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Master Thesis in Electronic Engineering

Design of a Nanopower NMOS-Based LDO for Wearable Applications

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Abstract

The increasing demand for portable and wearable electronic devices, together with the rapid expansion of Internet of Things (IoT) applications, has accelerated the development of ultra-low-power integrated circuits capable of operating under severe energy constraints. In these systems, power consumption represents one of the most critical design challenges, not only for the functional blocks but also for the power management circuits responsible for generating and regulating the supply voltages required by the system. This thesis presents the design and analysis of a nano-power LDO regulator optimized for ultra-low-power applications. The proposed architecture investigates circuit design techniques aimed at minimizing quiescent current while maintaining adequate voltage regulation and dynamic performance over a wide range of operating conditions. The proposed LDO architecture is designed and evaluated through circuit-level simulations, with particular emphasis on key performance metrics such as output voltage regulation, dropout voltage, quiescent current, transient response, and stability.

Introduction

The widespread adoption of portable electronic devices has led to an increasing demand for highly efficient and energy-conscious solutions. The continuous evolution toward smaller, smarter, and more autonomous electronic systems has accelerated the development of energy-efficient integrated circuits capable of performing complex tasks while operating under severe energy constraints, making power consumption one of the most critical design parameters in modern electronic systems. In particular, ultra-low-power Internet of Things (IoT) applications require power management solutions capable of maximizing battery lifetime while ensuring reliable operations. Furthermore, many IoT nodes spend the majority of their operating lifetime in low-power standby conditions, during which the energy consumed by inactive circuits can significantly affect the overall system power autonomy. Therefore, reducing power consumption is not only a requirement for the functional blocks of the system but also for the power management circuits responsible for supplying them. To optimize energy usage, IoT devices typically alternate between two main operating conditions:

- **Low-power standby mode:** the device remains in a low-activity state, requiring extremely low power consumption to maximize battery lifetime.
- **Active mode:** the device performs its intended functions and therefore requires higher performance and sufficient power delivery to support the increased load demand.

Efficient management of these transitions is therefore essential for extending the operational lifetime of battery-powered systems and enable long-term autonomous operation. To address these challenges, Power Management Integrated Circuits (PMICs) have become fundamental components in modern electronic systems. Their main function is to efficiently regulate, convert, and distribute the available energy to the different functional blocks of the system while minimizing power losses. In this context, ultra-low-power Low-Dropout (LDO) voltage regulators represent key components, providing stable and efficient power delivery while supporting the stringent energy constraints of modern IoT devices.

Among the different power management solutions, DC-DC converters are widely employed to improve energy efficiency by adapting the input voltage to the required supply levels. Switching regulators, such as buck and boost converters, can achieve high power conversion efficiency, especially when large voltage differences and high load currents are involved. However, their operation relies on high-frequency switching elements, which introduce additional design challenges, including increased circuit complexity, larger silicon area, electromagnetic interference (EMI), and output voltage ripple. These limitations make switching converters less suitable for applications requiring low-noise operation and extremely low power consumption. In contrast, Low-Dropout (LDO) voltage regulators offer a simpler and more compact solution for low-power applications.
The main benefits of LDO-based voltage regulation can be summarized as follows:

- **Low circuit complexity:** LDO regulators require a reduced number of active components compared with switching converters, resulting in simpler architectures and easier integration in CMOS technologies.
- **Small silicon area:** The absence of inductors and transformers allows LDOs to be implemented using only on-chip components, making them suitable for highly integrated systems.
- **Low output noise:** Since LDOs operate without high-frequency switching activity, they generate significantly lower output voltage ripple and electromagnetic interference (EMI), which is particularly important for analog, RF, and sensor applications.
- **Fast transient response:** LDOs can rapidly compensate for variations in load current, providing a stable supply voltage during transitions between different operating conditions.
- **High power supply rejection ratio (PSRR):** LDOs can effectively attenuate disturbances present on the input supply, improving the quality of the regulated output voltage.
- **Low Dropout Voltage:** LDOs can maintain regulation with a very small voltage difference between the input and output voltage and this maximizes efficiency is systems where the input and output voltages are very close.

LDOs are widely adopted in systems where energy efficiency and supply integrity are critical, such as IoT nodes, biomedical devices, and sensor interfaces. Despite these advantages, the design of ultra-low-power LDO regulators introduces significant challenges, as reducing the power consumption of the regulator itself often compromises other performance parameters,

such as stability, transient response, and regulation accuracy. Since modern electronic systems integrate several functional blocks that require different supply voltage levels and power quality requirements, it is important, especially for analog and RF circuits, to have a clean and stable voltage sources to preserve performance. Therefore, efficient voltage regulation is essential to guarantee reliable operation of the entire system.
In addition, battery-operated systems introduce further constraints due to the variability of the available input voltage and variability of load current. As the battery voltage decreases during discharge and the load current changes according to the operating state of the device, the unregulated supply provided to the LDO can experience significant fluctuations. Consequently, the regulator must guarantee accurate output voltage regulation under a wide range of input and load conditions. Achieving this level of robustness while maintaining nano-power consumption represents a critical challenge in the design of ultra-low-power LDOs.
In Chapter 1 of this work, the theoretical background of DC-DC converters is presented, with particular emphasis on linear regulators and switched-capacitor converters. Chapter 2 presents the proposed LDO architecture and provides an overview of the main design motivations and challenges addressed throughout this work. Chapter 3 describes the design of the individual building blocks and presents the transistor-level implementation of the proposed circuit, along with simulation results demonstrating the operation of the main blocks. In Chapter 4, the results obtained from the overall system simulations are reported, summarized in a table, and presented in the conclusions.

Chapter 1

DC-DC Converters Theory

In battery-powered electronic systems, such as portable devices and Internet of Things (IoT) applications, power converters play a fundamental role in ensuring reliable and efficient system operation. Batteries do not provide a constant output voltage; instead, their terminal voltage varies with the state of charge, discharge conditions, and instantaneous load current. Consequently, the voltage supplied by the battery cannot be directly used to power most electronic circuits. DC-DC converters are therefore employed to convert the unregulated battery voltage into one or more regulated supply voltages that satisfy the requirements of the different functional blocks while maximizing power conversion efficiency.
DC-DC converters can be categorized into three primary types based on their components:

- **Linear Regulators:** These circuits can only step down the voltage, making them suitable for applications where a lower voltage is required as portable electronics and wearables. They are compact, require minimal external components, and produce low noise. However, their efficiency is generally low.
- **Switched Capacitor Converters:** These converters utilize a switching mechanism to adjust the voltage by charging and discharging capacitors. Although they require more area than linear regulators, they offer improved efficiency and are used in applications where space is constrained but higher efficiency is necessary.
- **Inductive-Based Switching Converters:** These converters use inductors to regulate the output voltage by resisting rapid changes in current. They can step up, step down, or invert the input voltage and are capable of achieving very high efficiency. However, the need for substantial inductance often necessitates the use of bulky external components, makes them less suitable for wearables and IoT systems.

1.1 Analysis of Linear Regulators

Linear voltage regulators are widely used in electronic systems to provide a stable and regulated output voltage from a higher, unregulated DC input supply. Unlike switching converters, linear regulators operate by continuously controlling the conduction of a pass element, typically a MOSFET or bipolar transistor, connected in series with the load. By varying the resistance of the pass device, the regulator compensates for changes in the input voltage and load current, thereby maintaining a constant output voltage.

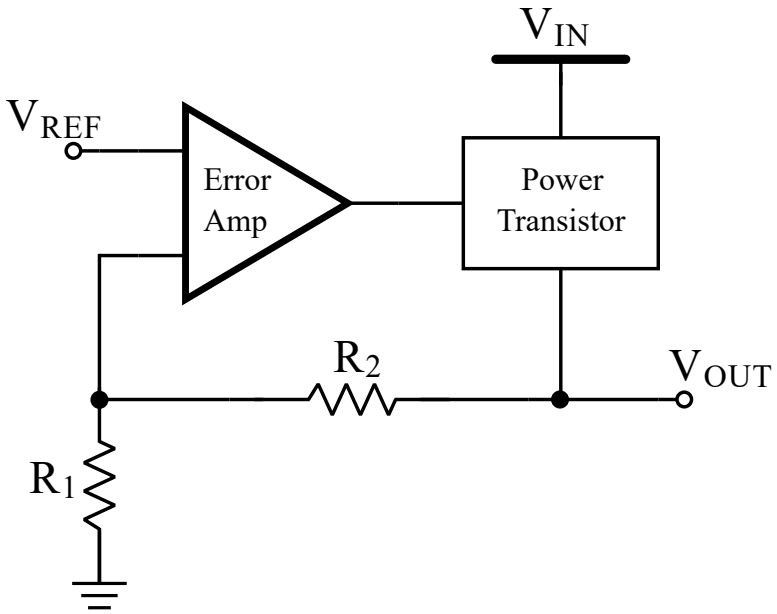


Figure 1.1: Schematic of general Linear Regulator.

The basic block diagram shown in Fig. 1.1, consists of a pass device placed between the input voltage (V_{IN}) and the regulated output voltage (V_{OUT}), a precision reference voltage (often derived from a bandgap circuit), and a resistor divider network formed by external or internal resistors. The operation is based on a negative feedback loop. The output voltage is sensed through a resistive feedback network and compared with a precise reference voltage by an error amplifier. The resulting error signal controls the pass transistor, continuously adjusting its conduction to minimize the difference between the desired and the actual output voltage. This closed-loop regulation enables the output voltage to remain nearly constant despite variations in the supply voltage or load current. Since the pass transistor operates in the linear region, and behaves as a variable resistance, the differential voltage between the input and output is dissipated as heat. Consequently, the power dissipation of a linear regulator can be expressed as:

$$P_{diss,linear} = I_{LOAD}(V_{IN} - V_{OUT}) \tag{1.1}$$

Where I_{LOAD} is the output load current, V_{IN} is the input unregulated voltage and V_{OUT} is the output regulated voltage.
The linear regulator mostly dissipates in the output stage (MOSFET or bipolar transistor) since the error amplifier and the resistive feedback branch are biased with a current generally negligible when compared to the output current. Instead, in a switched converter , in first approximation, the power dissipation depends on the power MOSFETs on-resistance, R_{ON}. The power dissipation can be roughly expressed as follows:

$$P_{diss,switched} = I_{LOAD}^2 R_{ON} \tag{1.2}$$

A switched converter has an efficiency advantage with respect to a linear regulator when:

$$P_{diss,switched} = I_{LOAD}^2 R_{ON} << I_{LOAD}(V_{IN} - V_{OUT}) = P_{diss,linear} \tag{1.3}$$

$$I_{LOAD} R_{ON} << (V_{IN} - V_{OUT}) \tag{1.4}$$

The linear regulator solution becomes interesting for light load (since the bias current required for a linear regulator is in general lower when compared to a switched-mode converter and for low drop ($V_{IN} - V_{OUT}$) applications.

1.2 Low Dropout Regulators

A particular class of linear regulators is represented by Low-Dropout (LDO) regulators, which are specifically designed to maintain output voltage regulation even when the difference between the input and output voltages is very small. This capability significantly improves efficiency in battery-powered applications, where the available supply voltage decreases as the battery discharges. Owing to these characteristics, LDO regulators have become one of the most widely adopted voltage regulation solutions for modern portable and ultra-low-power electronic systems. One of the most important performance metrics of an LDO regulator, particularly in nano-power applications, is its power efficiency. Since these regulators are intended for battery-powered systems operating under stringent energy constraints, maximizing efficiency is essential to extend battery lifetime. For an LDO, the power efficiency is primarily determined by:

$$\eta = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{IN}}} \tag{1.5}$$

where P_{IN} is the input power and P_{OUT} is the output power.

P_{IN} is defined as:

$$P_{IN} = V_{IN}(I_{IN} + I_q) \tag{1.6}$$

where I_q is the quiescent current consumed by the LDO. Under heavy-load conditions, the quiescent current is tipically much smaller than the input current I_{IN}. Consequently the input power can be approximated as:

$$P_{IN} \approx V_{IN} I_{IN} \tag{1.7}$$

P_{OUT} is defined as:

$$P_{OUT} = V_{OUT} I_{OUT} \tag{1.8}$$

Where V_{OUT} is the regulated output voltage, and I_{OUT} is the load current. The power efficiency can be rewrite as follows:

$$\eta = \frac{V_{\mathrm{OUT}} I_{\mathrm{OUT}}}{V_{\mathrm{IN}} I_{\mathrm{IN}}} \tag{1.9}$$

In the case of series regulator, like Low Dropout Regulator:

$$I_{IN} = I_{OUT} \tag{1.10}$$

and the efficiency can be rewritten as:

$$\eta \approx \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} \tag{1.11}$$

This expression shows that, as a first-order approximation, the efficiency of an LDO is primarily determined by the ratio between the output voltage and the input voltage. Consequently, high efficiency can be achieved by minimizing the dropout voltage (V_{DO}), i.e., the voltage difference between the input and output terminals. A smaller dropout voltage allows the output voltage to more closely track the input voltage, thereby reducing power dissipation across the pass transistor and improving the overall power conversion efficiency.
In general DC-DC switching regulators outperform linear regulators:

- Step-up (Boost), switching regulator has no linear counterpart
- Far better power efficiency at medium and high load current
- Far better power efficiency at high $V_{IN} - V_{OUT}$ drops

Linear regulators outperform DC-DC switching regulators:

- Less external components (lower BoM and area/volume occupation)
- Comparable or better efficiency for very light loads and low $V_{IN} - V_{OUT}$

- Far less noisy: no ripple affects the regulated output voltage
- Smaller pin count

The defining parameter of a low dropout regulator is its dropout voltage (V_{DO}), the minimum voltage differential between input and output required to maintain regulation. Once the input voltage approaches V_{OUT} , the pass device can no longer remain in its linear region, and regulation is lost.
For a MOSFET-based pass element, the dropout voltage is approximately:

$$V_{DO} = R_{DS(on)} I_{OUT} \tag{1.12}$$

Where a smaller $R_{DS(on)}$ yields a lower dropout at a given output current. LDOs generaly have V_{DO} values under 1 V; devices requiring less than 1 V input-output differential are called low-dropout regulators.

1.2.1 LDOs Building Blocks

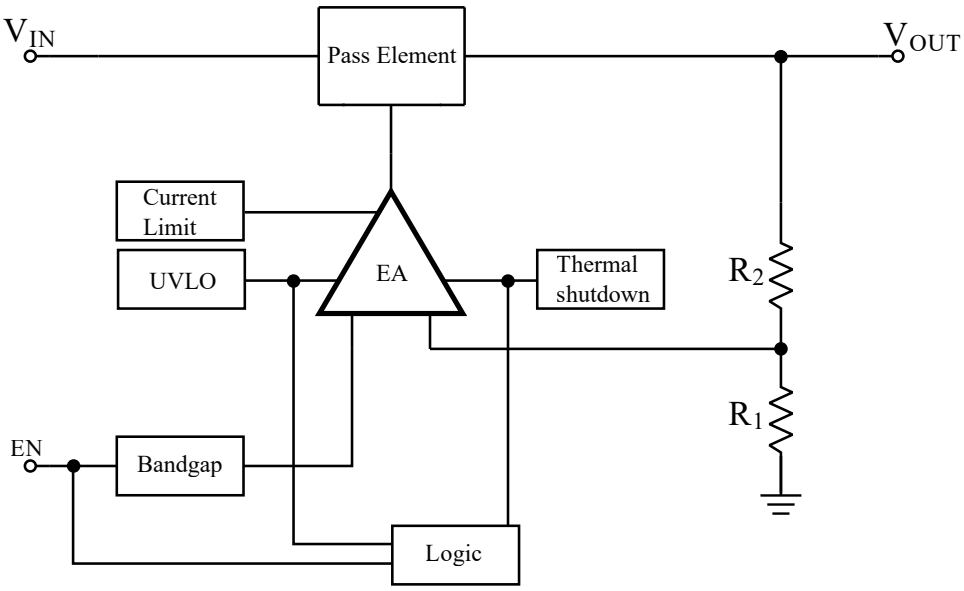


Figure 1.2: LDOs basic building blocks.

The essential blocks for an LDO are shown in Fig. 1.2 and they are:

- **Bandgap reference circuit:** Generates an on-chip temperature-independent reference voltage used by the error amplifier as the regulation reference. Since the reference voltage directly affects the output accuracy, its noise and stability have a significant impact on the overall performance of the LDO.

- **Error Amplifier:** its main function is to compare the feedback voltage with the reference voltage and amplify their difference. The resulting error signal drives the control terminal of the pass transistor, regulating the current delivered to the load and maintaining a constant output voltage. Ideally, the error amplifier should provide high DC gain to minimize the output voltage error, sufficient bandwidth to ensure fast response to load variations, and adequate phase margin to guarantee loop stability.
- **Pass Element:** is the main regulating device of the LDO and controls the amount of current delivered from the input supply to the load. It is typically implemented using a MOS transistor, usually a PMOS or NMOS device, or a bipolar transistor connected between the input voltage and the output node. The gate terminal of the pass transistor is controlled by the error amplifier, which continuously adjusts its conduction level according to the difference between the reference voltage and the feedback voltage.
- **Feedback network:** is responsible for sensing the output voltage and providing a scaled version of it to the error amplifier. It is typically implemented using a resistive voltage divider connected between the output node and ground.

In addition to the voltage regulation loop, practical LDO implementations often integrate several auxiliary circuits that enhance reliability, safety, and robustness. These include:

- **Thermal shutdown:** protects the regulator against excessive junction temperature by disabling the LDO when the temperature exceeds a predefined threshold. Once the device has sufficiently cooled down, normal operation can be restored, depending on the adopted protection strategy.
- **Overcurrent protection:** is a safety mechanism that limits the output current under overload or short-circuit conditions by sensing the load current, preventing excessive power dissipation and protecting both the LDO pass transistor and the load from permanent damage.
- **Under Voltage Lock Out (UVLO):** is a protection mechanism that continuously monitors the input supply voltage and disables the LDO when the input falls below a predefined threshold. This prevents the regulator from operating under insufficient supply conditions, where proper voltage regulation, loop stability, and reference generation cannot be guaranteed. UVLO typically incorporates hysteresis to prevent repeated switching near the threshold voltage, thereby ensuring reliable startup and shutdown behavior.

- **Logic block:** The logic block is a digital control unit that supervises the operation of the LDO by coordinating the enable signal and the outputs of the protection circuits, such as Undervoltage Lockout (UVLO), Overcurrent Protection, and Thermal Shutdown. Based on these inputs, it generates the internal control signals required to enable or disable the bias circuitry and the pass transistor, ensuring safe, reliable, and energy-efficient operation under both normal and fault conditions.

1.2.2 LDOs key parameters

The performance of an LDO regulator is characterized by several electrical parameters that define its operating range, regulation capability, and suitability for a specific application. These parameters are particularly important in low-power and battery-operated systems, where efficiency, accuracy, and robustness must be simultaneously achieved. The main performance metrics used to evaluate an LDO regulator are the following:

- **Input voltage range:** it defines the interval of input supply voltages over which the LDO is guaranteed to operate correctly while maintaining its specified performance. In the event of an undervoltage condition, LDOs equipped with an Under-Voltage Lockout (UVLO) circuit disable the regulator and shutdown the output to prevent improper operation of the following circuits and avoid possible system failures or instability.

- **Output voltage accuracy:** it represents the deviation of the regulated output voltage from its nominal value under specified operating conditions. It is a measure of the capability of the LDO to provide an output voltage close to the desired value.

- **Line regulation:** it represents the variation of the output voltage caused by changes in the input voltage while the output current is kept constant. It is a measure of the ability of the LDO to maintain a regulated output voltage despite variations in the input supply voltage.

- **Load regulation:** it represents the variation of the output voltage caused by changes in the output current while the input voltage is kept constant. It is a measure of the ability of the LDO to maintain a regulated output voltage despite variations in the load current.

- **Dropout voltage:** is defined as the minimum voltage difference between the input and output voltages required to maintain output voltage regulation. In MOS-based LDOs, the dropout voltage is specified

when the pass transistor operates in the linear region. In this condition, the dropout voltage mainly depends on the on-resistance of the pass transistor and the output current.

- **Load transient response:** it represents the variation of the output voltage, typically expressed in terms of undershoot and overshoot, caused by a sudden change in the load current. It evaluates the capability of the LDO to quickly restore the output voltage after a load transient event.
- **Output voltage noise:** it represents the magnitude of the noise generated at the output terminal of the LDO. It is typically defined as the total noise contribution from all internal circuit blocks integrated over a specified frequency range.
- **Quiescent currents and standby currents:** They are critical parameters in battery-operated systems because they directly affect the overall energy consumption and battery lifetime. The quiescent current represents the current consumed by the internal circuitry of the LDO during normal operation, excluding the load current, while the standby current refers to the current consumed when the regulator is disabled or operating in a low-power mode. In conventional LDOs, these currents are typically in the microampere range, while ultra-low-power LDOs aim to reduce them to the nanoampere range.

1.2.3 Pass Transistor topologies

The pass transistor is one of the most critical building blocks of an LDO regulator, as it directly controls the current delivered from the input supply to the load. Consequently, its characteristics strongly influence several key performance parameters, including dropout voltage, load current capability, transient response, loop stability, power efficiency, and power supply rejection ratio (PSRR). The selection of the pass device therefore represents one of the primary design choices in LDO architectures.
In CMOS implementations, the pass element is typically realized using either a PMOS or an NMOS transistor. Although both devices perform the same voltage regulation function, their operating principles and electrical characteristics differ significantly, resulting in different advantages and limitations.

PMOS Pass Transistor

In PMOS-based LDO regulators, the pass transistor is connected between the input supply and the output node, with its source tied to the input voltage. The gate voltage is controlled by the error amplifier to regulate

the current supplied to the load. PMOS transistor is configured as common source amplifier. The minimum voltage difference between input and output terminals is the minimum voltage required to keep MOSFET in saturation region, which is tipically around 50 mV to 200 mV. PMOS-based LDO regulators have power efficiency comparable with switching regulators due to their extremely low dropout voltage, and they do not require any additional voltage bias.

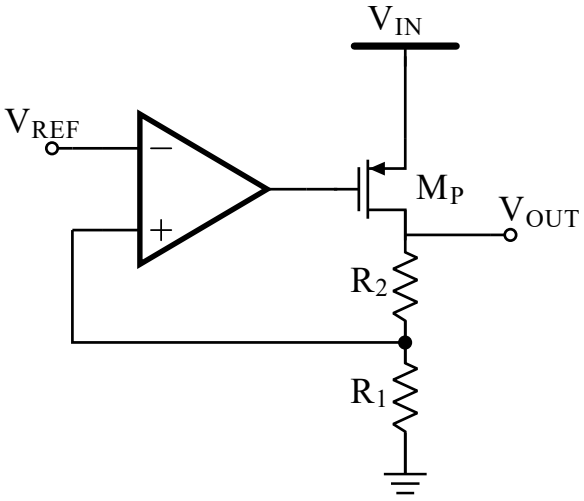


Figure 1.3: Schematic of PMOS-based LDO.

However one of the main challenges associated with PMOS-based LDO regulators is ensuring loop stability. Due to the relatively large gate capacitance of the PMOS pass transistor, a low-frequency pole is introduced at the gate node. At the same time, another dominant pole is typically present at the output node, where the load resistance and output capacitance determine the pole location. If these two poles are located close to each other in the frequency domain, the resulting phase shift can significantly reduce the phase margin of the feedback loop, potentially leading to oscillations or unstable operation. Consequently, appropriate frequency compensation techniques are required to guarantee stable operation over the entire range of input voltages and load currents.
The main advantages and disadvantages of this architecture can be summarized as follows:
Advantages:

- **Low dropout voltage**
- **No charge pump required**
- **Simpler architecture**

Disadvantages:

- **Larger transistor size**
- **Larger gate capacitance makes the compensation more challenging**
- **Slower transient response**

NMOS Pass Transistor

In NMOS-based LDO regulators, the pass transistor is also connected between the input and output nodes, but its gate voltage must be driven above the input supply voltage to ensure sufficient gate overdrive (V_{gs}-V_{th}). Consequently, an auxiliary voltage-boosting circuit, such as a charge pump, is generally required.

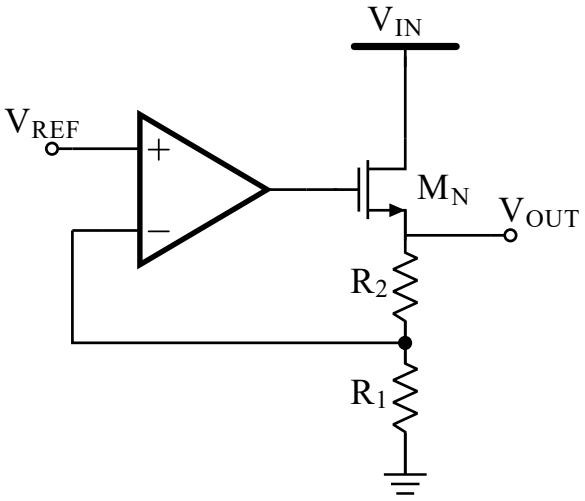


Figure 1.4: Schematic of NMOS-based LDO.

In this configuration the NMOS pass device acts like a common drain amplifier, this makes the difference between input and output voltage large than PMOS case. However the higher electron mobility on NMOS transistor compared to the hole mobility of PMOS transistor significantly reduces the size of pass transistor. Moreover output impedance is lower and hence regulation will be better.
The main advantages and disadvantages of this architecture can be summarized as follows:
Advantages:

- **Smaller transistor size**
- **Faster transient response**
- **Stability easier to achieve**

Disadvantages:

- **Boosted voltage is required**
- **Large dropout voltage**
- **Higher circuit complexity**

Although PMOS pass transistors are widely adopted in commercial LDO regulators due to their simple gate-drive requirements and low dropout operation, NMOS-based architectures represent an attractive alternative for applications requiring improved driving capability and higher transconductance. Owing to the higher electron mobility, an NMOS pass transistor can provide a larger transconductance for the same device area, resulting in improved current driving capability and potentially enhanced transient performance. For these reasons, the proposed LDO adopts an NMOS pass transistor, providing an alternative architecture to the PMOS-based solutions commonly found in commercial products.

1.3 Analysis of Switched Capacitor Converters

As discussed in the previous section, the proposed LDO employs an NMOS transistor as the pass element. Unlike a PMOS pass transistor, an NMOS device used in a high-side configuration requires its gate voltage to be higher than the input supply voltage in order to maintain sufficient gate-to-source overdrive and operate in the desired region. As the input voltage decreases or the load current increases, the required gate voltage may exceed the available supply voltage. Consequently, the gate cannot be driven directly by the error amplifier, and an auxiliary voltage-boosting circuit becomes necessary.
To overcome this limitation, a charge pump is employed to generate a boosted voltage higher than the input supply. This boosted voltage is used to drive the gate of the NMOS pass transistor, ensuring sufficient gate overdrive over the entire operating range of the regulator.
The following sections describe the operating principle of Switched Capacitor Converters (SCCs), introduce the simplest voltage-boosting circuit topology, and present the analysis of their equivalent circuit.

1.3.1 Basic operating principle

A switched-capacitor circuit is a discrete-time circuit that operates by transferring electric charge through one or more capacitors using periodically controlled switches. The switching sequence is driven by two or more well-defined, non-overlapping clock phases, which precisely control the charging

and discharging processes of the capacitors. As a result, the amount of transferred charge is accurately determined. By repeatedly transferring charge between different circuit nodes, switched-capacitor circuits can generate output voltages that differ from the available supply voltage. This operating principle forms the basis of switched-capacitor charge pumps, which are widely employed in integrated circuits to generate voltages higher or lower than the input supply without requiring inductors.
One of the principal advantages of switched-capacitor converters is that they do not require magnetic components, such as inductors or transformers, for energy transfer. Consequently, they can be fully integrated using standard CMOS technologies, resulting in a compact solution with reduced silicon area. Furthermore, the absence of magnetic elements significantly mitigates electromagnetic interference (EMI), making switched-capacitor converters particularly attractive for low-noise and highly integrated applications.
Charge pump circuits operate by exploiting one of the fundamental properties of capacitors: the voltage across a capacitor cannot change instantaneously. This behavior follows directly from the capacitor current-voltage relationship:

$$i_C(t) = C\frac{dv_C(t)}{dt} \tag{1.13}$$

where $i_C(t)$ is the current flowing through the capacitor, $v_C(t)$ is the voltage across the capacitor, and C is the capacitance.
An instantaneous change in the capacitor voltage would require an infinite current, which is physically impossible. Consequently, the voltage across a capacitor is a continuous quantity and cannot undergo abrupt transitions. Switched-capacitors circuits exploit this property by periodically reconfiguring the connections of one or more capacitors through clock-controlled switches. During one clock phase, a capacitor is charged to a known voltage, while during the following phase it is reconnected to a different node, transferring the stored charge and effectively shifting the voltage level. By repeating this process over successive clock cycles, charge pumps are able to generate output voltages higher or lower than the available supply voltage.

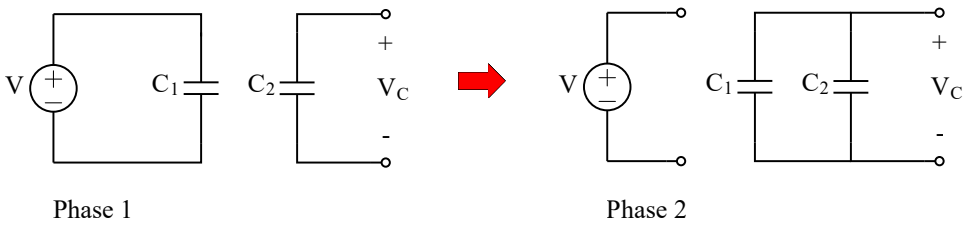


Figure 1.5: Basic principle operation of switched capacitor converters

In Fig. 1.5, during Phase 1 the capacitor C_2 is completely discharged and the voltage across its terminals is:

$$V_{C2,1} = 0 \tag{1.14}$$

The energy across the capacitor C_1 is defined as:

$$E_1 = \frac{1}{2}CV^2 \tag{1.15}$$

During phase 2, C_1 is attached in parallel with C_2; in this new configuration the voltage across C_2 is defined as:

$$V_{C2,2} = \frac{V}{2} \tag{1.16}$$

The energy is defined as:

$$E_2 = \frac{1}{4}CV^2 \tag{1.17}$$

At the end of the cycle the voltage across the capacitors and energy are changed:

$$V_{C2,1} \neq V_{C2,2} \tag{1.18}$$

$$E_2 \leq E_1 \tag{1.19}$$

Whenever charge is redistributed between two capacitors initially charged to different voltages, a portion of the stored energy is irreversibly lost. Although an ideal capacitor is a lossless energy-storage element that can, in principle, return all the energy stored in its electric field, energy is required whenever charge is transferred from one node to another. Specifically, moving a charge (q) across a potential difference (ΔV) requires an energy equal to:

$$E = q\Delta V \tag{1.20}$$

Consequently, when two capacitors at different voltages are connected together, charge flows from the higher-potential capacitor to the lower-potential one until a common equilibrium voltage is reached. During this redistribution process, the total electric charge is conserved, whereas the total electrostatic energy stored in the capacitors decreases. The difference between the initial and final stored energy is dissipated in the conductive path connecting the capacitors, even when ideal capacitors are assumed. This unavoidable energy dissipation is known as the charge-sharing loss and can be expressed as:

$$\Delta E = C\Delta V_C^2 \tag{1.21}$$

The previous analysis shows that the charge-sharing loss is directly related to the voltage difference between the capacitors involved in the charge-transfer process. In particular, since the energy loss is proportional to the square of the voltage difference (ΔV_C^2), large voltage transitions between two nodes result in significant energy dissipation. Therefore, instead of transferring the entire voltage difference in a single charge-sharing event, the voltage conversion can be divided into multiple smaller voltage steps. By reducing the voltage difference experienced during each charge-transfer operation, the associated charge-sharing losses are minimized, improving the overall efficiency of the switched-capacitor converter.

$$\Delta E = \sum_{i=1}^{M} C\frac{\Delta V_C^2}{M^2} = C\frac{\Delta V_C^2}{M} \tag{1.22}$$

Where M is the number of consecutive steps, and if the number of steps tends to infinite:

$$M \to \infty \tag{1.23}$$

$$\Delta E \to 0 \tag{1.24}$$

1.3.2 Voltage Doubler

To introduce the operating principle of switched-capacitor converters (SCCs), the voltage doubler is considered as a simple and intuitive example. SCCs exploit the charge transfer and redistribution between capacitors, controlled by switches operating according to periodic clock signals. The voltage doubler represents one of the simplest SCC topologies and allows an output voltage ideally equal to twice the input voltage.

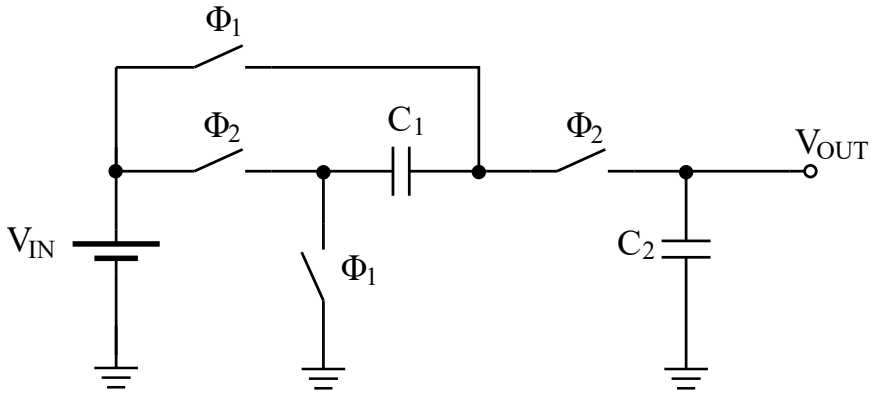


Figure 1.6: Schematic of SCC Voltage Doubler

Fig. 1.6 shows the schematic of the voltage doubler, consisting of two capacitors and four switches controlled by two complementary clock signals,

Φ_1 and Φ_2. These non-overlapping phases define the two operating states of the converter, each having the same duration. During the first phase, the switches controlled by Φ_1 are closed, while the remaining switches are open as shown in Fig. 1.7.

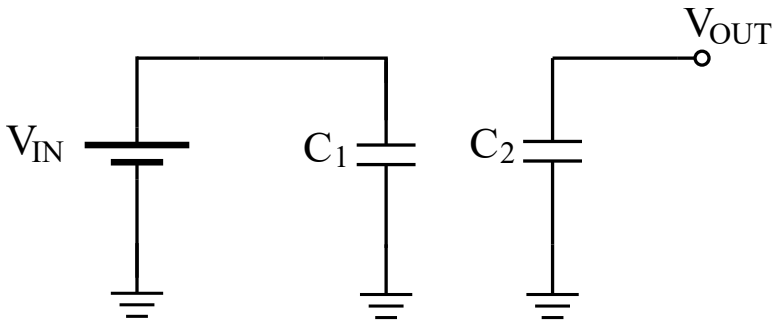


Figure 1.7: Voltage Doubler Phase 1

In this configuration, the capacitor C_1 is connected across the input supply and is therefore charged to the input voltage:

$$V_{C1} = V_{IN} \tag{1.25}$$

During the second phase, the switches controlled by Φ_1 are opened and the switches controlled by Φ_2 are closed as shown in Fig. 1.8.

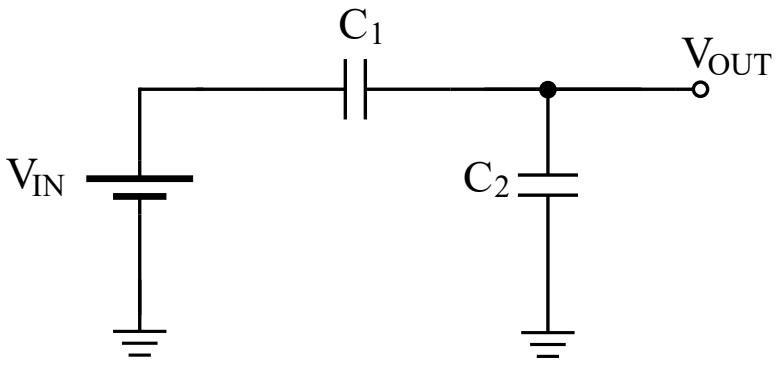


Figure 1.8: Voltage Doubler Phase 2

Since C_1 has previously been charged to V_{IN}, the voltage at the output node ideally becomes:

$$V_{OUT} = V_{IN} + V_{C1} = 2V_{IN} \tag{1.26}$$

Therefore, under ideal conditions and neglecting conduction losses, charge redistribution, and parasitic effects, the voltage conversion ratio M of the voltage doubler is:

$$M = \frac{V_{OUT}}{V_{IN}} = 2 \tag{1.27}$$

This simple example highlights the fundamental operating principle of SCCs: capacitors are periodically charged and reconfigured through switches so that their stored voltage can be transferred or stacked to obtain the desired voltage conversion. Several other SCC topologies can be employed to achieve different voltage conversion ratios, depending on the number and arrangement of capacitors, switches, and operating phases [1].

1.3.3 Equivalent Model

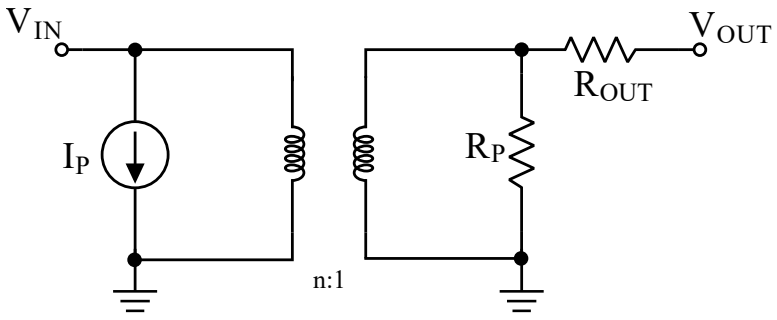


Figure 1.9: Equivalent model of switched-capacitor converter

The equivalent model of a switched-capacitor converter (SCC) consists of several elements that account for the main sources of power loss in the circuit. The output resistance R_{OUT} models the losses associated with charge redistribution and switch conduction losses. Its value depends on several parameters, including the SCC topology, the capacitance value, the size and on-resistance of the switching devices, and the operating switching frequency. Since these losses are caused by the current flowing through the equivalent output resistance, their impact increases with the load current, and the losses can be defined as:

$$P_I = R_{OUT} I_{OUT}^2 \tag{1.28}$$

The equivalent resistance R_{P} represents the losses introduced by parasitic capacitances, which arise from non-ideal effects in the capacitors, switches, and interconnections. These parasitic elements reduce the efficiency by causing additional charge transfer during each switching cycle. The relative losses are defined as:

$$P_J = \frac{V_{OUT}^2}{R_P} \tag{1.29}$$

The current source I_{P} models the power losses associated with the gate capacitances of the switching transistors. During operation, the charging and discharging of the gate capacitances require energy from the clock generation circuitry, resulting in an additional dynamic power consumption component. The relative losses are defined as:

$$P_{GATE} = V_{IN} I_P \tag{1.30}$$

The efficiency of a switched-capacitor converter (SCC) can be defined as:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_I + P_J + P_{GATE}} = \frac{1}{1 + R_{OUT}\frac{I_{OUT}}{V_{OUT}} + \frac{V_{OUT}}{I_{OUT}R_P} + \frac{I_P}{nI_{OUT}}} \tag{1.31}$$

Under light load conditions:

$$I_{OUT} \to 0 \tag{1.32}$$

The efficiency can be rewritten as follows:

$$\eta = \frac{I_{OUT}}{I_{OUT} + \frac{V_{OUT}}{R_P} + \frac{I_P}{n}} \tag{1.33}$$

Under heavy load conditions:

$$I_{OUT} \to \infty \tag{1.34}$$

The efficiency can be rewritten as follows:

$$\eta = \frac{1}{1 + R_{OUT}\frac{I_{OUT}}{V_{OUT}}} \tag{1.35}$$

The equivalent output resistance R_{OUT} represents the lumped contribution of the main losses associated with the charge pump operation, including charge-transfer losses and conduction losses through the switching devices. It determines the voltage drop between the ideal output voltage and the actual output voltage under load conditions. There are 2 main components:

- **Slow Switching Limit (SSL):** represents the asymptotic behaviour of a switched-capacitor converter when the switching frequency is sufficiently low. In this operating regime, the output voltage drop is mainly determined by the amount of charge that must be transferred from the flying capacitors to the load during each switching cycle.
- **Fast Switching Limit (FSL):** represents the asymptotic behaviour of a switched-capacitor converter when the switching frequency becomes sufficiently high. In this operating regime, the flying capacitors experience only small voltage variations during each switching

cycle, since the time available for charge redistribution is significantly reduced. Consequently, the charge-sharing losses become negligible compared with the resistive losses associated with the current flow through the converter. The dominant contribution to the equivalent output resistance is determined by the finite resistance of the current path, including the on-resistance of the switching devices, the equivalent series resistance (ESR) of the capacitors, and the parasitic resistances introduced by interconnections and routing.

The transition between the Slow-Switching Limit and the Fast-Switching Limit is associated to characteristic time constant of the switched-capacitor network.

$$\tau = R_{\text{eq}} C_{\text{eq}} \tag{1.36}$$

Where R_{eq} and C_{eq} represent the equivalent resistance and capacitance seen by the charging path. The converter operates in Slow-Switching Limit (SSL) when:

$$f_{\text{sw}} << \frac{1}{R_{\text{eq}} C_{\text{eq}}} \tag{1.37}$$

In this condition, the capacitors have enough time to fully charge and discharge during each phase, and charge-sharing losses dominate. Conversely, the Fast-Switching Limit occurs when:

$$f_{\text{sw}} >> \frac{1}{R_{\text{eq}} C_{\text{eq}}} \tag{1.38}$$

Where the capacitors experience only small voltage variations during each switching cycle and conduction losses dominate the output impedance. Total R_{OUT} can be empirically approximated as:

$$R_{\text{OUT}} = \sqrt{R_{\text{SSL}}^2 + R_{\text{FSL}}^2} \tag{1.39}$$

To minimize the equivalent output resistance R_{OUT}, the switched-capacitor converter should operate as close as possible to the Fast-Switching Limit (FSL). Increasing the switching frequency reduces the contribution of charge-sharing losses, since the capacitors experience smaller voltage variations during each switching cycle. Similarly, increasing the flying capacitor value reduces the amount of voltage ripple associated with each charge-transfer event, thereby lowering the SSL contribution to the output resistance.
However, increasing the switching frequency and capacitance, introduces additional design trade-offs. A higher switching frequency increases the dynamic power consumption associated with charging and discharging the gate capacitances of the switching devices, while larger capacitors increase the

silicon area and parasitic capacitances. Therefore, the optimal design requires a compromise between minimizing the SSL contribution and limiting the additional losses associated with FSL operation.

Chapter 2

Proposed Low Dropout Architecture

The objective of this work is the design of a nano-power LDO regulator employing an NMOS transistor as the pass element. Compared with the conventional PMOS-based architecture, the use of an NMOS pass transistor offers several advantages, including improved current-driving capability, enhanced transient response, PSRR, and output noise performance. The main limitation of an NMOS-based LDO arises from the gate-drive requirements of the pass transistor. Since the NMOS is used as a high-side pass device, its gate voltage must be higher than the available input supply voltage to provide sufficient gate-to-source overdrive and ensure proper operation over the entire operating range. As a consequence, the gate cannot be driven directly by the error amplifier, making an auxiliary voltage-boosting circuit necessary. To overcome this limitation, a switched-capacitor charge pump is integrated into the proposed architecture. The charge pump generates a boosted voltage from the available input supply, providing the gate voltage required to properly drive the NMOS pass transistor. However, because the charge pump operates continuously, its power consumption contributes directly to the overall quiescent current of the regulator. Consequently, its design represents a critical aspect of the proposed architecture.
To minimize this overhead, special attention has been devoted to the implementation of the charge pump control circuitry. A low-power digital logic architecture has been developed to generate the required clock signals while minimizing both dynamic and static power consumption. The resulting solution enables the advantages of an NMOS-based LDO to be achieved without compromising the ultra-low-power requirements of the overall regulator.
The block diagram of the proposed LDO architecture illustrated in Fig. 2.1, consists of several key functional blocks, including the power stage, the error amplifier, an output buffer, and the feedback network. Each block has been carefully designed and optimized to satisfy the stringent power requirements

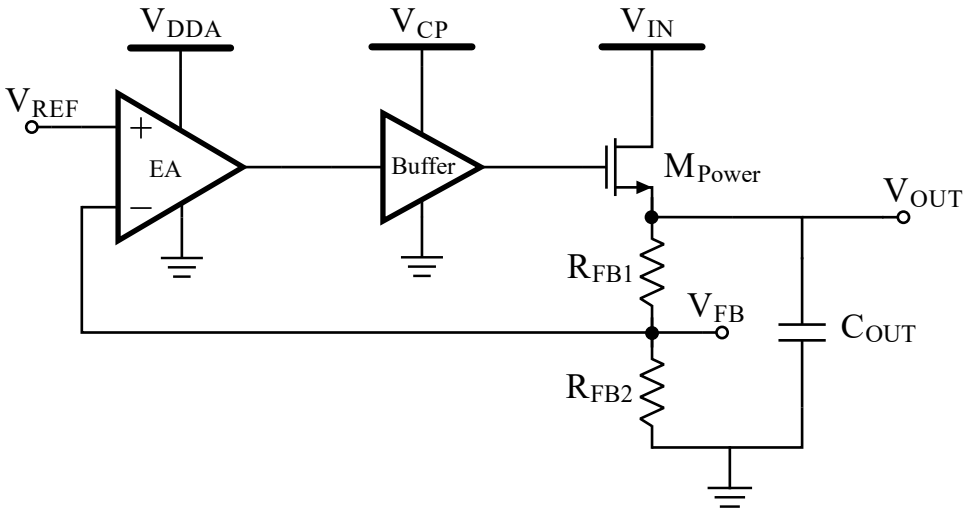


Figure 2.1: Block Diagram of proposed LDO.

of ultra-low-power applications, especially under light-load conditions, where the quiescent current of the regulator dominates the total energy consumption, while ensuring reliable operation of the regulator. Consequently, the design of each circuit block has been optimized to reduce both static and dynamic power dissipation without compromising the overall performance of the LDO.

2.1 Design Specifications and Objectives

Several design specifications and requirements are defined for this work, including the input voltage range, output voltage accuracy, load current range, maximum load current, and quiescent current limit. Particular emphasis is placed on achieving ultra-low quiescent current, especially under light-load conditions.

Quantity	**Symbol**	**MIN**	**MAX**
Input Voltage	V_{IN}	1.7 V	5.5 V
Output Voltage	V_{OUT}	1.7 V	1.8 V
Output Voltage Accuracy	err% V	-2%	+2%
Analog Voltage	V_{DDA}	1.7 V	3 V
Load Current	I_{LOAD}	0 A	100 mA
Quiescent Current	$I_{q,LDO}$	-	200 nA

Table 2.1: Design Specifications

Table 2.1 summarizes the main specifications and design constraints of the proposed LDO. Particular attention was devoted to the analog supply volt-

age V_{DDA}, which is provided by another LDO block and follows the variation of the input voltage V_{IN}. V_{DDA} is limited to a maximum value of 3 V. When V_{IN} falls below 3 V, V_{DDA} follows it until the minimum allowable input voltage of 1.7 V is reached. Fig. 2.2 shows the schematic of the V_{DDA} generation circuit and an overview of the complete system.

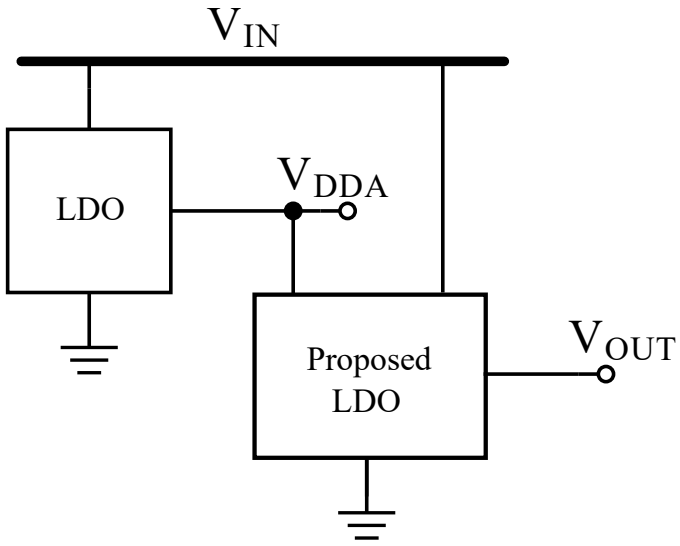


Figure 2.2: Overview of the complete scheme.

Particular attention was devoted to the minimum allowable input voltage of the system, $V_{IN} = 1.7$ V, which is lower than the nominal regulated output voltage of 1.8 V. Under this condition, the LDO enters the dropout region and can no longer maintain the nominal output voltage. Consequently, the output voltage is expected to follow the input voltage as closely as possible.

2.2 Principal blocks

The proposed architecture consists of an NMOS pass transistor connected between the input and output voltages, an Error Amplifier (EA) biased by the available supply voltage V_{DDA}, which is derived from the input voltage, a buffer biased by the boosted voltage V_{CP} generated by a charge pump, and a resistive feedback network that senses the output voltage and generates its scaled version, V_{FB}. One of the fundamental building blocks is the boosted-voltage generation circuit, which provides the voltage required to properly bias the gate of the NMOS pass transistor. This ensures a sufficient gate overdrive voltage to drive the output load across the entire operating range. Several voltage boosting techniques can be adopted to generate a voltage higher than the available supply voltage. Among them, switched-capacitor converters (SCCs) represent one of the most suitable solutions for low-power

applications requiring limited silicon area. This allows the generation of a boosted voltage starting from a lower input voltage while maintaining a compact implementation and low power consumption.

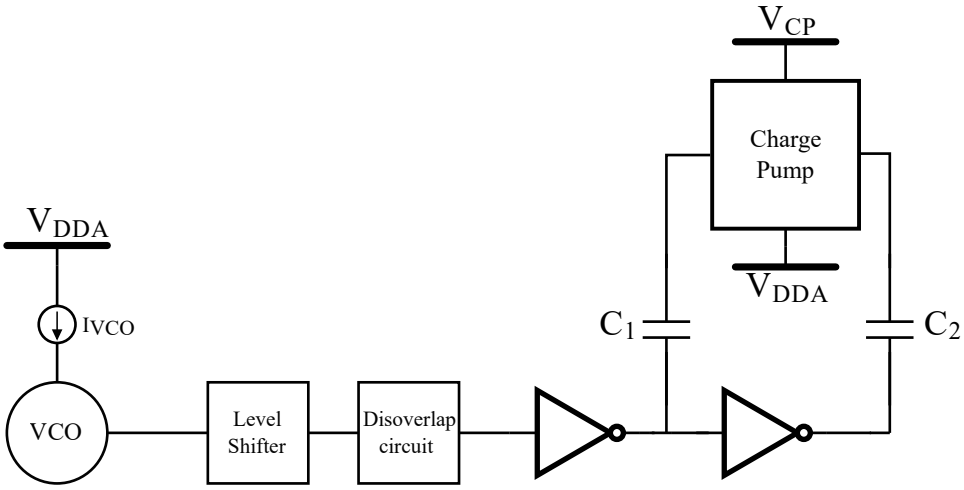


Figure 2.3: Block Diagram of Charge Pump voltage generation.

Fig. 2.3 shows the block diagram of the proposed boosting-voltage circuit. The architecture employs a current-starved voltage-controlled oscillator (VCO) to generate the clock signal required by the switched-capacitor charge pump. The oscillation frequency of the VCO is determined by its bias current I_{VCO} , allowing the switching frequency to be controlled depending on load current, while maintaining extremely low power consumption when required. However, the waveform produced by the VCO does not exhibit sufficiently fast transitions or rail-to-rail voltage levels to directly drive the charge pump. To overcome this limitation, a dedicated clock generation stage is introduced between the VCO and the charge pump. Its purpose is to convert the VCO output into well-defined digital clock signals suitable for efficiently driving the switched-capacitor converter. The architecture is composed by several logic blocks. This stage consists of a level shifter followed by a non-overlapping clock generation circuit. The level shifter acts as a waveform-conditioning block, restoring the signal amplitude and producing sharp rising and falling edges that enable reliable operation of the subsequent digital circuitry. The conditioned clock signal is then processed by the non-overlapping clock generation circuit, which generates two complementary, non-overlapping clock phases required for the operation of the cross-coupled charge pump. Introducing a dead time between the two phases prevents cross-conduction in the clock drivers, reducing unnecessary power dissipation and improving the overall efficiency of the charge pump, particularly under light-load conditions. The generated non-overlapping clock phases are finally buffered by dedicated inverter stages, which provide the

current-driving capability required to switch the charge pump capacitors. Consequently, the generated non-overlapping clock signals allow the charge pump to operate efficiently, producing a boosted output voltage greater than the available input supply. This boosted voltage is used to drive the gate of the NMOS pass transistor.
Another fundamental block of the proposed architecture is the error amplifier (EA), which forms the core of the feedback control loop. Its primary function is to compare the reference voltage, generated by the bandgap reference, with the feedback voltage derived from the output node. Based on the resulting error signal, the amplifier generates the control voltage that drives the gate of the NMOS pass transistor, thereby regulating the output voltage and maintaining it at the desired value.
Since the proposed LDO targets ultra-low-power applications, the error amplifier must exhibit extremely low power consumption under light-load conditions. At the same time, it must provide sufficiently high DC gain to ensure accurate output voltage regulation and minimize steady-state regulation errors. Achieving these conflicting objectives represents one of the main challenges in the design of nano-power LDO regulators.
To properly drive the NMOS pass transistor, an additional buffer stage is introduced between the error amplifier output and the gate terminal of the pass device. The buffer is biased by the boosted voltage generated by the charge pump, allowing the gate voltage of the NMOS transistor to reach values higher than the available input supply voltage.
This configuration ensures sufficient gate-to-source overdrive, particularly in low dropout conditions, where the input voltage approaches the regulated output voltage. In this operating region, the available voltage headroom is significantly reduced, making it essential to provide an adequate gate drive voltage to maintain the required control capability of the pass transistor and preserve the regulation performance of the LDO.

2.2.1 Power Pass Transistor

Another fundamental block of the LDO is the pass transistor, which acts as the power device responsible for regulating the current delivered from the input supply to the load. Controlled by the error amplifier, the pass transistor continuously adjusts its conduction to maintain a constant output voltage despite variations in the input supply voltage and load current. Therefore, it must be capable of supplying the required load current while ensuring accurate voltage regulation and stable operation over the entire operating range. The performance of the pass transistor is strongly influenced by both the selected device technology and its dimensions that determine its transconductance, parasitic capacitances, and current-driving capability. A sufficiently large device provides a lower effective conduction resistance, enabling the LDO to deliver high load currents while maintaining a low

dropout voltage. However, increasing the device dimensions also increases the gate capacitance, which may degrade the loop bandwidth, complicate frequency compensation, and increase the power required to drive the gate. Consequently, the sizing of the pass transistor represents a critical design trade-off between current-driving capability, dropout voltage, dynamic performance and stability.
The pass device adopted in this work is an Extended-Drain NFET transistor implemented in the 55 nm CMOS technology provided by GlobalFoundries. The dimensions of the power MOSFET are selected to satisfy the design specifications under the worst-case operating conditions, ensuring reliable voltage regulation throughout the entire operating range.
The worst-case condition corresponds to the minimum input supply voltage, V_{IN} = 1.9 V while maintaining the regulated output voltage at V_{OUT} = 1.8 V and supplying the maximum load current of I_{LOAD} = 10 mA. Under these conditions, only a limited voltage headroom is available across the pass device, making this operating point the most demanding in terms of current-driving capability. The dimensions of the NMOS pass transistor are therefore determined by analyzing the regulator under these worst-case conditions. The device is sized to provide the required load current while maintaining sufficient gate-to-source overdrive to guarantee proper regulation at the specified dropout voltage. At the same time, the transistor dimensions are chosen to achieve an appropriate trade-off among current-driving capability, parasitic capacitances and silicon area.
The adopted power MOSFET size is W = 10 mm, implemented using 100 fingers with W_{finger} = 100 μm each one with a channel lenght of L_{min} = 167 nm. With this sizing, the pass transistor is capable of delivering the maximum specified load current while maintaining sufficient voltage headroom to operate in saturation under the worst-case design condition.

I_{LOAD}	V_{Gate}	V_{Dsat}
4 mA	2.62 V	79 mV
6 mA	2.646 V	84 mV
8 mA	2.666 V	90 mV
10 mA	2.681 V	95 mV
12 mA	2.695 V	99 mV
14 mA	2.706 V	104 mV
16 mA	2.716 V	108 mV
18 mA	2.726 V	112 mV
20 mA	2.734 V	116 mV

Table 2.2: Dependency of V_{Dsat} on load current I_{LOAD}.

The analysis reported in 2.2 shows that the required saturation voltage of the power pass transistor remains lower than the available dropout voltage

for load currents up to approximately $I_{LOAD} = 12$ mA. Therefore, under the specified operating conditions, the selected transistor dimensions satisfy the dropout requirement and guarantee proper regulation of the output voltage. However, the large device area introduces significant parasitic capacitances, particularly at the gate terminal, which affect the stability and transient response of the LDO. Therefore, the gate-driving capability provided by the buffer and charge pump must be carefully designed to ensure adequate control of the pass transistor.

2.2.2 PSRR analysis of different Pass Devices in LDO Architectures

The Power Supply Rejection Ratio (PSRR) is a key performance parameter of an LDO regulator, as it quantifies the ability of the circuit to suppress disturbances and ripple components present on the input supply voltage over a wide frequency range. It is typically evaluated by comparing the amplitude of the input supply ripple coupled to the output node, and it is defined as:

$$PSRR = 20 \log \left(\frac{V_{\text{IN,ripple}}(f)}{V_{\text{OUT,ripple}}(f)} \right) \tag{2.1}$$

A high PSRR indicates that variations in the input supply are effectively attenuated, resulting in a cleaner and more stable output voltage. This parameter becomes particularly critical in low-power applications, where supply noise can significantly affect the performance of sensitive analog circuits. Considering the specifications of the proposed nano-power LDO, achieving high PSRR performance represents one of the main design objectives.
In order to understand the impact of the pass transistor choice on PSRR, the main noise coupling paths of PMOS- and NMOS-based LDO architectures are analyzed.
As illustrated in Fig. 2.4 several coupling paths allow disturbances present on the input supply to propagate to the regulated output voltage. The first path corresponds to the feedback loop of the LDO, which actively suppresses low-frequency supply variations through the regulation action of the error amplifier. The second path is associated with the finite output conductance of the pass transistor, providing a direct coupling mechanism between the input and output nodes. The third path originates from the finite Power Supply Rejection Ratio (PSRR) of the error amplifier, allowing a fraction of the input supply ripple to be transferred to the gate of the pass device. Finally, the fourth path is due to the finite PSRR of the bandgap reference, whose supply sensitivity can also contribute to output voltage disturbances. The relative importance of these coupling mechanisms strongly depends on the architecture of the LDO, and in particular on the type of pass transistor

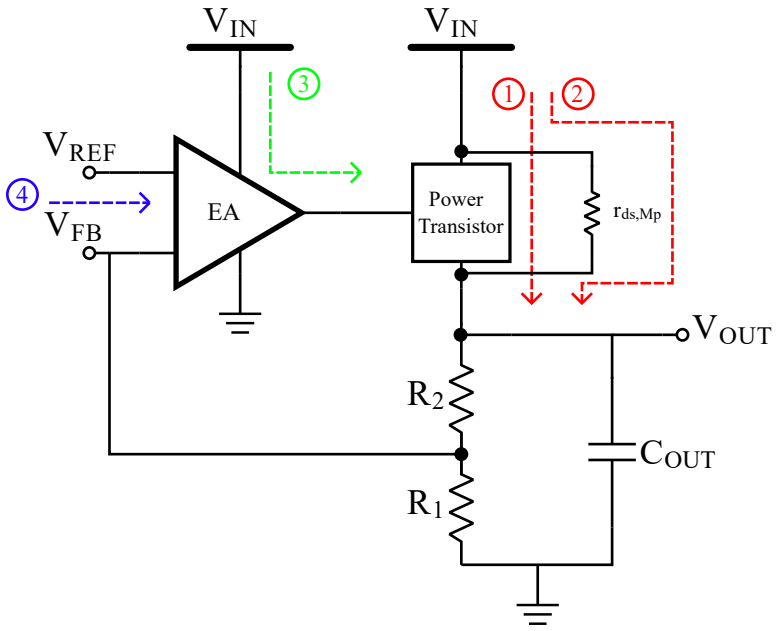


Figure 2.4: Input to output ripple paths in LDOs.

employed. PMOS and NMOS-based regulators exhibit different ripple propagation paths and small-signal characteristics, leading to different PSRR performance over the frequency spectrum.

PSRR analysis of PMOS Pass transistor

The PSRR of an LDO exhibits different characteristics depending on the operating frequency. At low frequencies, the rejection capability is primarily determined by the loop gain of the voltage regulator. In this frequency range, the error amplifier provides a high open-loop gain, allowing the feedback loop to effectively suppress disturbances originating from the input supply. Consequently, the low-frequency PSRR is mainly dictated by the loop gain and the intrinsic PSRR of the error amplifier. As the frequency increases, the gain of the error amplifier progressively decreases, reducing the effectiveness of the feedback loop. In the mid-frequency range, supply disturbances begin to propagate through the parasitic capacitances associated with the pass transistor and the compensation network, causing a gradual degradation of the PSRR. At high frequencies, the loop gain becomes negligible and the feedback loop can no longer attenuate input supply ripple. Under these conditions, the PSRR is dominated by the direct feedthrough mechanisms of the pass transistor and by the parasitic capacitances between its terminals. More in details in a PMOS-based LDO architecture, the source of the pass transistor is connected directly to the input supply voltage, V_{IN}. At low frequencies, this does not significantly affect the regulator perfor-

mances because the high loop gain allows the feedback loop to effectively reject supply voltage variations. As the frequency increases, however, the loop gain progressively decreases, reducing the ability of the control loop to suppress disturbances. Consequently, input ripple can propagate to the output through the pass transistor via its finite output resistance and intrinsic parasitic capacitances. Compared to an NMOS device, a PMOS transistor exhibits a lower transconductance g_{m}:

$$g_{\mathrm{m}} = \sqrt{2\mu C_{\mathrm{OX}} \frac{W}{L} I_{\mathrm{LOAD}}} \tag{2.2}$$

Furthermore the transconductance g_{m} is proportional to the drain current and to the carrier mobility of the device. Consequently, for the same bias current and identical device dimensions, a PMOS transistor exhibits a lower g_{m} than an NMOS transistor because hole mobility is significantly lower than electron mobility.

$$\mu_{\mathrm{n}} \approx 3\mu_{\mathrm{p}} \tag{2.3}$$

The pass transistor operates as a common-source stage, providing a voltage gain approximately proportional to:

$$A_{\mathrm{v}} \propto g_{\mathrm{m,pass-MOS}}(r_{\mathrm{o}} // R_{\mathrm{L}}) \tag{2.4}$$

Where r_{o} is the output impedance of Pass Transistor and R_{L} is the load impedance.
Consequently, the transconductance of the pass device directly contributes to the overall loop gain. Since a PMOS transistor exhibits a lower transconductance than an equivalent NMOS transistor under the same bias conditions, the regulator generally achieves a lower loop gain and a reduced bandwidth, resulting in poorer PSRR performance.
Furthermore, to provide the same current-driving capability, a PMOS transistor typically requires a considerably larger channel width than an equivalent NMOS transistor. This larger device area increases the gate and junction parasitic capacitances, including C_{gs}, C_{gd}, and drain-to-bulk capacitances. These parasitic capacitances create additional high-frequency feedthrough paths from the input supply to the output, further degrading the high-frequency PSRR.

PSRR analysis of NMOS Pass transistor

In contrast, the pass transistor of an NMOS-based LDO operates as a source follower (common-drain stage), whose small-signal voltage gain is ideally close to unity. Therefore, the pass device does not provide significant voltage amplification, and its transconductance does not directly determine the loop gain as in the PMOS case. Instead, the transconductance mainly affects

the source follower accuracy, the output impedance of the pass device, and the location of the output pole, thereby influencing the loop bandwidth, stability, and ultimately the PSRR performance.

$$A_{\mathrm{v}} \approx \frac{g_{\mathrm{m,pass-MOS}}(r_{\mathrm{o}}//R_{\mathrm{L}})}{1 + g_{\mathrm{m,pass-MOS}}(r_{\mathrm{o}}//R_{\mathrm{L}})} \tag{2.5}$$

And if:

$$g_{\mathrm{m,pass-MOS}}(r_{\mathrm{o}}//R_{\mathrm{L}}) >> 1 \tag{2.6}$$

$$A_{\mathrm{v}} \approx 1 \tag{2.7}$$

Therefore, unlike the PMOS common-source configuration, the pass transistor does not provide a significant voltage gain contribution to the overall loop gain. However, a high transconductance is still desirable because it allows the source follower gain to approach unity, improving the accuracy of the voltage transfer from the gate to the output node.
Furthermore, the transconductance of the NMOS pass device directly affects the output impedance seen at the LDO output node. Since the source of the NMOS transistor is connected to the output, the small-signal output resistance, for sufficiently large g_{m} is approximately determined by:

$$R_{\mathrm{OUT}} \approx \frac{1}{g_{\mathrm{m,pass-MOS}}} \tag{2.8}$$

Therefore, increasing the pass transistor transconductance reduces the output impedance and moves the output pole towards higher frequencies:

$$f_{\mathrm{p,OUT}} = \frac{1}{2\pi R_{\mathrm{OUT}} C_{\mathrm{OUT}}} \tag{2.9}$$

leading to an increased loop bandwidth and improved transient response. Consequently, although g_{m} does not directly provide voltage gain in an NMOS pass stage, maximizing the pass transistor transconductance is beneficial for achieving high bandwidth, improved regulation accuracy, and enhanced PSRR performance.
Based on the previous considerations, the choice of an NMOS pass transistor instead of a PMOS device was made through preliminary analyses that considered the design specifications and the main objectives of this work. The first advantage of an NMOS pass transistor is its higher current-driving capability, which represents a critical requirement for the proposed LDO, as the regulator must guarantee proper voltage regulation over a wide load current range, up to 100 mA. Furthermore, the higher current capability of the NMOS device allows a reduction in the required transistor size compared with a PMOS implementation providing the same output current capability.

This results in a lower silicon area occupation, which is a significant advantage in integrated circuit design. Another important aspect is the improved PSRR performance achievable with the NMOS architecture, particularly at medium and high frequencies, thanks to the source-follower configuration of the pass device and the reduced coupling between the input supply and the output node. In contrast, conventional PMOS-based LDOs often require additional PSRR enhancement techniques, such as ripple cancellation or feed-forward compensation, which introduce extra circuitry and may increase the overall quiescent current. Despite the several advantages offered by the NMOS pass transistor, this architecture introduces an additional design challenge related to the generation of the gate driving voltage. For this reason, a switched-capacitor charge pump is integrated into the proposed LDO architecture.

Chapter 3

Transistor-Level Implementation

3.1 Power Stage

The sizing of the power pass transistor in an LDO is a critical design aspect, as it directly determines the load-driving capability of the regulator, the achievable dropout voltage, and consequently the overall efficiency of the system. The width of the pass device must be carefully optimized to provide the required output current while minimizing the voltage drop across the transistor in low-dropout conditions. However, increasing the transistor size also introduces larger parasitic capacitances and higher area occupation, requiring a proper trade-off between performance, power consumption, and silicon area. The sizing methodology and the selection of the NMOS pass transistor are discussed in detail in Chapter 2, including the motivations behind the chosen device dimensions and architecture. Another fundamental aspect of an adaptive LDO architecture is the implementation of an accurate load current sensing technique. This function is required to adapt the biasing conditions of the regulator according to the load demand, improving performance while maintaining low quiescent current. However, current sensing in an NMOS-based LDO can be more challenging compared with conventional PMOS implementations due to the different connection of the pass device

3.1.1 Current Sensing of NMOS Power Stage

Current sensing represents a fundamental aspect of an adaptive LDO architecture, since it provides information about the load current level and enables the dynamic optimization of the regulator operation. By accurately detecting the load demand, the bias conditions of the internal blocks can be adapted to provide the required regulation performance over the entire op-

erating range. In particular, current sensing allows the regulator to increase the available driving capability and loop bandwidth during high-load conditions, where fast transient response and high current capability are required. Conversely, during idle and light-load operation, the internal bias currents can be reduced to minimize the quiescent current consumption while still maintaining output voltage regulation. This aspect is especially critical in the proposed nano-power LDO, where minimizing the current consumption in idle mode is one of the primary design objectives.

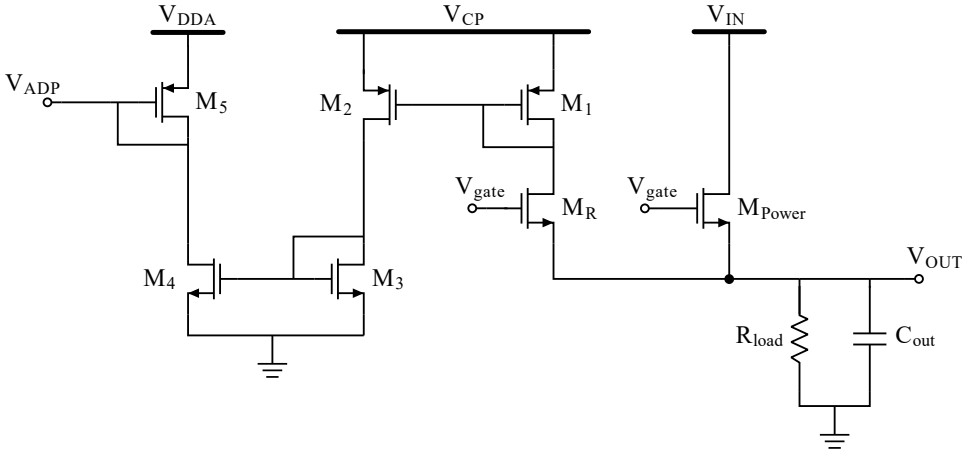


Figure 3.1: First implementation of Current Sensing circuit.

The first implemented current sensing technique is illustrated in Fig. 3.1. It is based on a replica transistor approach, where a scaled-down copy of the power MOS transistor is employed to estimate the load current. The replica transistor M_{R} is connected with its gate and source terminals in common with the power MOS transistor M_{Power}, ensuring that, under first-order approximation, both devices experience the same gate-source voltage and consequently the same overdrive voltage:

$$V_{OV,R} \approx V_{OV,Power} \tag{3.1}$$

By properly selecting the scaling factor (k), the current flowing through the replica device is a scaled version of the current flowing through the power transistor:

$$I_{Replica} = \frac{I_{Load}}{k} \tag{3.2}$$

The sensed current is then mirrored through transistor M_1 and subsequently mirrored again to generate the required bias current for the adaptive circuitry. This second mirroring stage also performs a voltage domain conversion, transferring the sensed information from the charge pump voltage

domain V_{CP} to the supply voltage domain V_{DDA}, where part of the adaptive block circuitry is implemented.

Limitations of Current Sensing

However this replica-based current sensing technique presents several limitations:

1. The first drawback is related to the drain voltage mismatch between the replica transistor and the power transistor. Since the drain terminals of the two devices are not maintained at the same voltage, the two transistors experience different channel-length modulation effects (3.3). As a consequence, the sensed current is affected by an error that reduces the accuracy of the load current estimation.

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{TH})(1 + \lambda V_{DS}) \tag{3.3}$$

2. A second limitation is related to the biasing requirements of the sensing branch. In order to correctly mirror the replica current through M_1, a sufficiently high source-gate voltage must be provided. For this purpose the replica branch must be biased in the boosted voltage V_{CP} domain.

3. Since the sensing branch operates in the charge pump voltage domain, the boosted voltage V_{CP} generated by the charge pump is required to sustain the replica current. This introduces an additional load for the charge pump, increasing its current consumption. This aspect becomes particularly critical under heavy-load conditions, where a larger sensed current is required. In this operating condition, the charge pump must provide a higher current to the sensing circuitry, which can reduce the generated boosted voltage level. The reduction of V_{CP} can affect the switching conditions of the charge pump devices, requiring a higher switching activity to compensate for the increased current demand and further increasing the power consumption.

4. Another critical issue occurs during no-load and light-load operation, especially when the input voltage approaches the regulated output voltage. In this condition, the pass transistor enters the low-dropout region and becomes less sensitive to variations of the gate voltage. Therefore, the loop tends to increase the gate voltage in an attempt to restore the output voltage. However, the replica transistor may not experience the same operating condition as the power transistor. While the power MOS can operate in the linear region close to dropout, the replica device may remain in saturation, where the drain current

strongly depends on the gate-source voltage. As a result, an increase in the gate voltage can cause a significant increase in the replica current, generating an unnecessary current consumption during light-load conditions.

Proposed Current Sensing circuit

Considering the limitations of the previously discussed approach, a different current sensing technique is investigated. The proposed current sensing circuit is illustrated in Fig. 3.2.

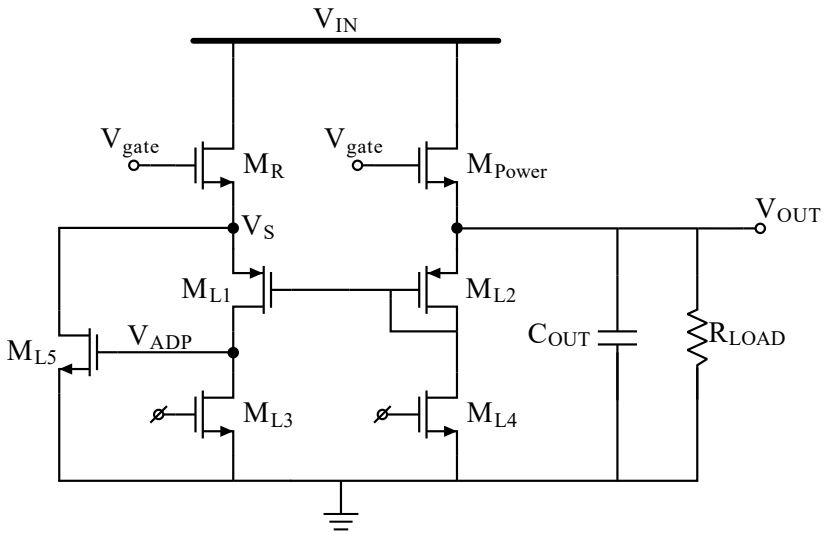


Figure 3.2: Proposed Current Sensing circuit.

The proposed configuration overcomes the limitations previously discussed. More specifically, the new current sensing circuit employs an internal voltage feedback loop composed of M_{L1}, M_{L2}, M_{L3} and M_{L5}, which forces the source voltage of the replica transistor M_{R} to be equal to the source voltage of the power transistor M_{Power}, corresponding to the LDO output voltage. Furthermore, the drain terminals of both the power transistor and the replica transistor are connected to the input voltage, while their gate terminals are connected together. As a consequence, the two transistors operate with the same terminal voltages, ensuring a better matching of their operating conditions. This significantly improves the accuracy of the sensed current, since the channel-length modulation effect is minimized due to the equal drain-source voltages. The gates of M_{L3} and M_{L4} are biased with a fixed voltage, which forces a reference current of 5 nA to flow in the loop. This ensures the correct biasing point of the entire replica structure even under no load conditions, while minimizing the quiescent current in this operating condition. An additional important advantage of this architecture is the

improved behavior during dropout operation. Since the replica transistor experiences the same voltage conditions as the power transistor, it enters the same operating region. Therefore, when the power transistor enters the triode region close to dropout and becomes less sensitive to gate voltage variations, the replica transistor exhibits the same behavior and does not increase its current consumption due to further gate voltage variations. This avoids the excessive sensing current observed in the previous approach and preserves the low-power operation of the LDO.
The replica current is converted into the control voltage V_{ADP} , which carries the information about the load current level. This voltage is then used to control the current mirrors that generate the adaptive bias currents for the various functional blocks of the LDO. As the load current increases, V_{ADP} varies accordingly, increasing the mirrored currents supplied to the adaptive circuitry. Conversely, under light-load conditions, V_{ADP} decreases, reducing the bias currents and minimizing the overall quiescent current consumption. In this way, the proposed adaptive biasing scheme automatically adjusts the current delivered to each internal block according to the operating conditions, ensuring the required performance under heavy-load conditions while preserving ultra-low power consumption during idle operation.

3.1.2 Replica MOS

The replica transistor is sized such that the sensed current represents only a small fraction of the load current. This scaling factor is carefully selected to minimize the power consumed by the sensing circuitry, which is particularly important under light-load and no-load operating conditions. The replica transistor is implemented as a series array of Extended-Drain NFET devices identical to those used for the power pass transistor, whose dimensions are selected to achieve the desired scaling factor with respect to the power pass transistor.
The dimensions of the replica branch are selected to achieve a current scaling factor of k = 22.500 with respect to the power pass transistor respecting the equation (3.5)

$$\frac{W_P}{L_P} = k\frac{W_R}{L_R} \tag{3.4}$$

$$k = \frac{W_P L_R}{W_R L_P} \tag{3.5}$$

3.2 Error Amplifier

A fundamental block of the proposed LDO is the error amplifier (EA), whose primary function is to compare the feedback voltage with a stable reference

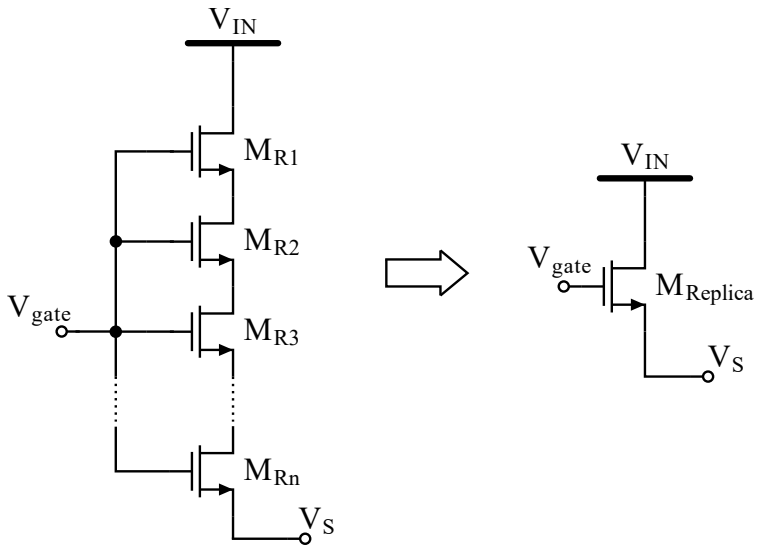


Figure 3.3: Replica MOS Structure.

voltage provided by an external bandgap reference. The error amplifier detects the difference between these two signals and amplifies it to generate the control signal that drives the subsequent stages of the regulator, thereby ensuring accurate output voltage regulation through the feedback loop. The performance of the error amplifier has a direct impact on the overall behavior of the LDO. A high DC gain is required to minimize the steady-state regulation error and achieve high output voltage accuracy. At the same time, a wide bandwidth is desirable to enable the feedback loop to respond rapidly to variations in the input voltage and load current, improving both the transient response and the power supply rejection ratio (PSRR). Another fundamental design aspect of the error amplifier is its power consumption, especially under light-load and no-load operating conditions. Since the LDO must maintain output voltage regulation even when the load current is extremely low, the error amplifier must operate with a very limited bias current to minimize the overall quiescent current consumption. However, reducing the bias current directly affects the available transconductance and consequently the DC gain and bandwidth of the amplifier. Therefore, the main design challenge is to achieve an ultra-low-power error amplifier while maintaining sufficient gain accuracy and loop performance over the entire load current range, including no-load conditions.
The first implementation of the error amplifier is based on a PMOS differential pair version of adaptive-core error amplifier architecture, proposed in [2], and illustrated in Fig. 3.4.
The proposed architecture is implemented with two biasing circuits: a fixed bias branch and an adaptive bias branch. This approach allows the error

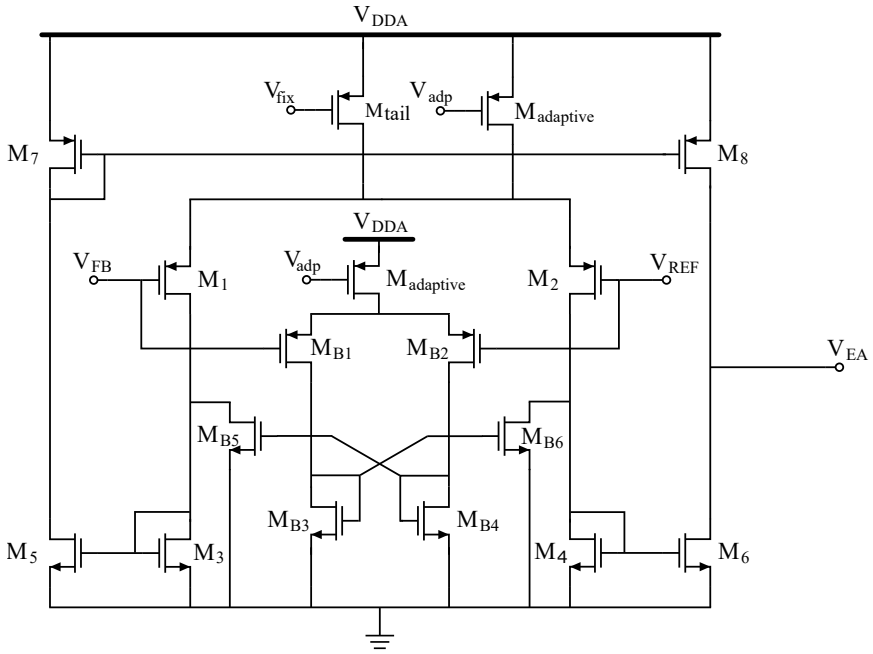


Figure 3.4: Error Amplifier with adaptive core.

amplifier to operate in two different modes depending on the load current condition.

1. **Light-Load operating condition:** Under light-load or no-load conditions, only the fixed bias circuit is active. This branch provides a minimum bias current in the nanoampere range, ensuring the correct biasing of the internal nodes of the error amplifier. In this operating condition, the adaptive transconductance core is turned off. In this way, even with zero output current, the error amplifier is still able to generate the required amplified error signal to properly drive the subsequent stages of the LDO feedback loop.

2. **Heavy-Load operating condition:** When the load current increases, the adaptive bias network detects the higher current demand and increases the bias current supplied to the error amplifier. The increased bias current activates the adaptive g_{m} core and improves the transconductance of the amplifier devices, allowing the transistors to remain in the desired operating region and improving the overall gain and bandwidth of the feedback loop.

This adaptive behavior provides the required regulation capability and transient performance under high-load conditions while avoiding unnecessary power consumption during light-load operation.

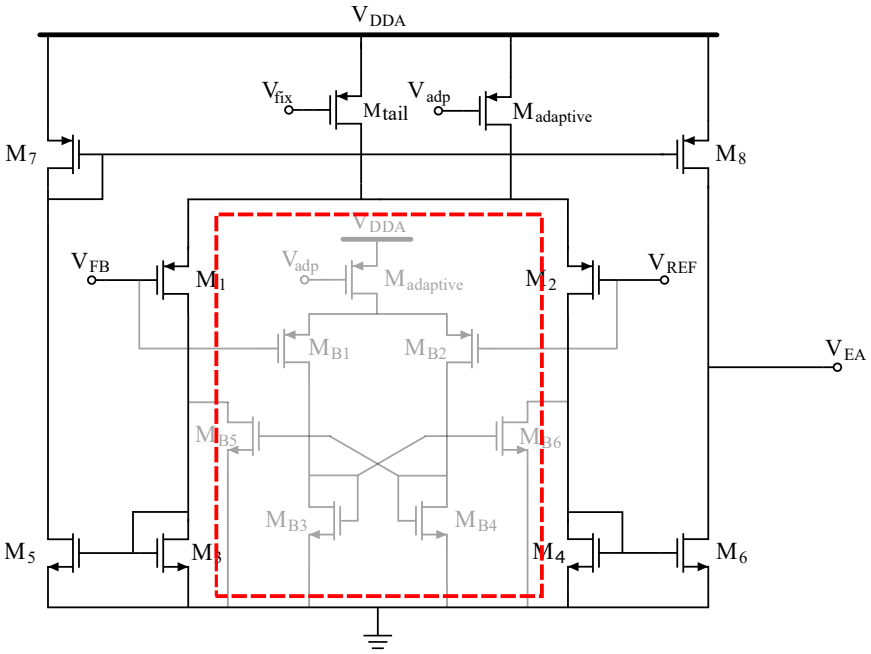


Figure 3.5: Error Amplifier in Light-Load condition.

A limitation encountered in this architecture is the presence of a non-dominant pole introduced by the internal nodes of the current mirror stage, mainly due to the parasitic capacitances associated with transistors M_4-M_6 and M_3-M_5. This pole is located at a relatively low frequency, which can negatively affect the stability of the error amplifier. This issue becomes particularly critical under heavy-load conditions, where the adaptive biasing increases the amplifier transconductance g_{m} and consequently extends the loop bandwidth. As the unity-gain frequency moves closer to the non-dominant pole, the phase margin can be significantly degraded, requiring more complex compensation techniques to ensure stable operation. Therefore, although increasing the bias current improves the intrinsic speed of the error amplifier, the achievable bandwidth can be limited by the position of the non-dominant poles and by the additional compensation requirements needed to guarantee sufficient stability.

The proposed error amplifier, illustrated in Fig. 3.6, represents an improved version of the previously discussed architecture and is designed to overcome the limitations associated with the low-frequency non-dominant pole. The new configuration retains the g_{m} boosting mechanism, while introducing a folded structure in the output stage instead of the topology adopted in the previous implementation. This architectural modification reduces the parasitic capacitance associated with the critical internal nodes, particularly the gate capacitance introduced by the devices of the previous current-mirror structure. As a result, the corresponding non-dominant pole is shifted to a

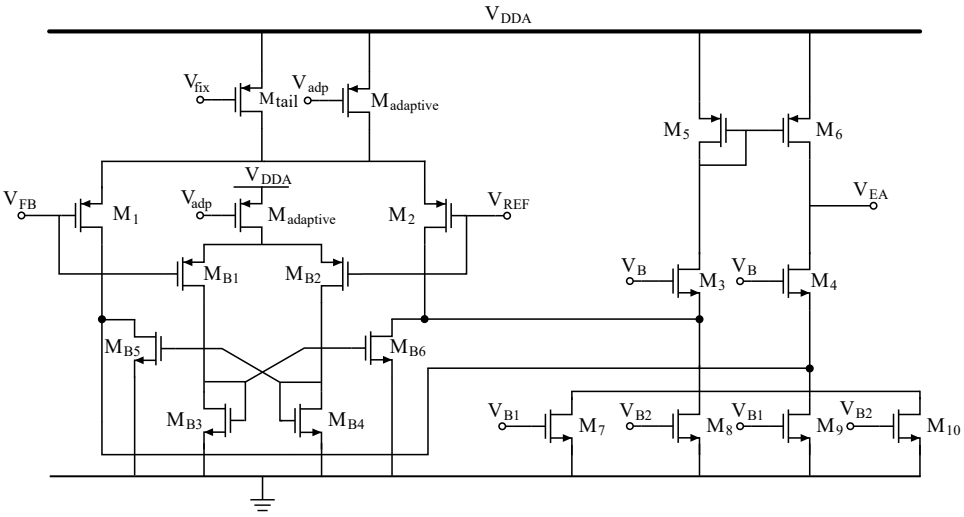


Figure 3.6: Proposed Folded Error Amplifier with gm boosting.

higher frequency, reducing its interaction with the unity-gain frequency and simplifying the frequency-compensation requirements. The reduced parasitic loading also allows the error amplifier to achieve a higher bandwidth while maintaining adequate stability over the different load-current conditions. Therefore, the proposed architecture provides an improved trade-off between transconductance, bandwidth and stability compared with the previous implementation. The main drawback of the proposed architecture is the increased complexity of the biasing circuitry required to properly bias the cascode devices. In particular, the folded structure requires additional bias voltages to ensure the correct operating conditions of the transistors, resulting in a more complex bias network and an associated increase in power consumption. For this reason, a novel biasing strategy for the error amplifier is investigated, with particular emphasis on reducing the bias current under light-load conditions while maintaining accettable performances.
The biasing network of the error amplifier presented in Fig. 3.7, is composed of two main parts: a fixed-bias branch and an adaptive-bias branch. The fixed-bias branch is always active, including under no-load conditions, in order to maintain the error amplifier correctly biased and ensure continuous regulation of the output voltage even when the load current is zero. Conversely, the adaptive-bias branch adjusts the bias current of the error amplifier according to the load current, increasing the available current under heavy-load conditions to improve the amplifier gain and bandwidth. The fixed-bias branch is therefore a fundamental component for achieving low-power operation, since its bias current determines the minimum current consumed by the error amplifier during no-load and light-load conditions. In the initial implementation, the fixed-bias branch was designed to provide

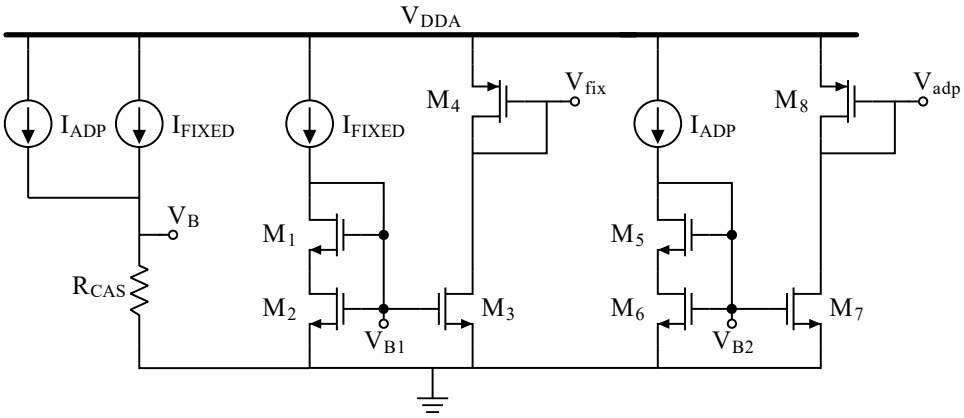


Figure 3.7: Bias network of proposed Error Amplifier.

a constant current of 10 nA. This low bias current is used to generate the required bias voltages for the different nodes of the error amplifier while maintaining a very low power consumption. However, in order to further reduce the power consumption of the error amplifier, a different biasing approach was adopted in the final implementation.

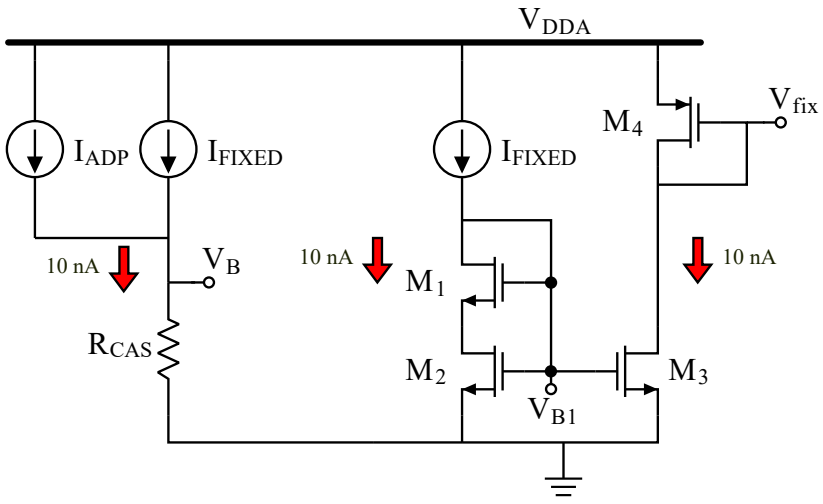


Figure 3.8: Fixed bias network of proposed Error Amplifier.

In the initial implementation, the no-load operating condition resulted in a fixed current consumption of approximately 30 nA for the biasing network, in addition to approximately 5 nA consumed by the error amplifier itself. Therefore, the total current associated with the error amplifier reached approximately 40 nA even in the absence of load current. Considering the stringent quiescent-current requirements of the proposed LDO, this consumption was considered excessive. To further reduce the current consumption under

no-load and light-load conditions, a duty-cycled bias current technique is therefore adopted in the final implementation. This technique consists of using a switch controlled by a low-duty-cycle periodic signal to activate the bias current only for a fraction of the operating time. Consequently, the average current consumption of the bias circuit is reduced approximately in proportion to the duty cycle, as shown in (3.6), while the required biasing functionality is maintained during the active portion of each cycle.

$$I_{q,EA,AVG} = DI_{q,ON,EA} \tag{3.6}$$

$I_{\mathrm{q,EA,AVG}}$ is the total averaged current consumption of Error Amplifier and bias network, D is the duty cycle of control signal and $I_{\mathrm{q,ON,AVG}}$ is the current consumed while the bias circuit is active.

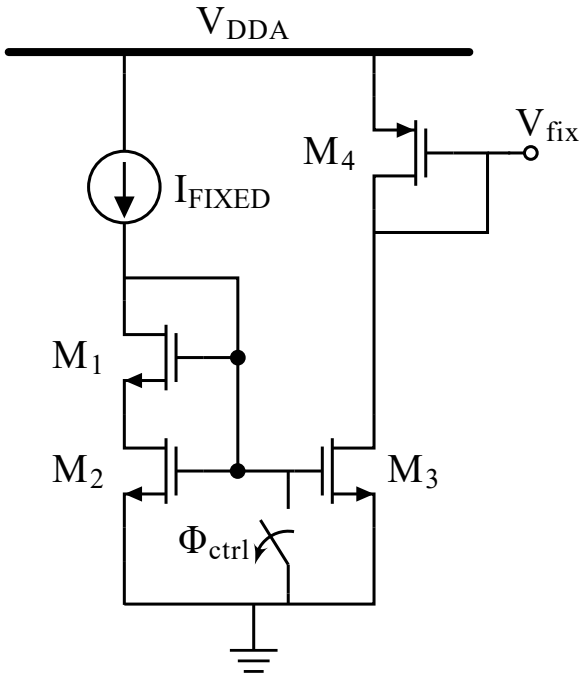


Figure 3.9: Duty-cycled fixed bias network of proposed Error Amplifier.

The control signal Φ_{ctrl} is generated from the clock signals produced by the charge pump driver block. An additional inverter is employed to generate the control signal, which is then used as the input of a counter. The counter generates a periodic control signal with a reduced duty cycle, enabling the bias current to be activated only for a limited fraction of each cycle.
An 8-stage counter is implemented to generate the control signal. As a result, the bias current is active for approximately (1/8) of the total period, corresponding to a duty cycle of (D=1/16=6.25 %). Assuming that the instantaneous current consumption during the active phase remains approximately unchanged, the average current consumed by the bias circuit is

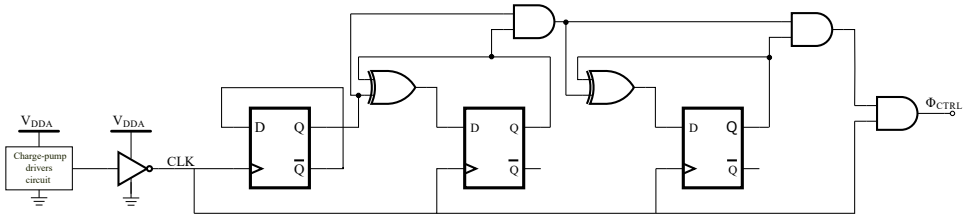


Figure 3.10: Control signal generation.

reduced by a factor of 16. Resulting in a total current consumption of 2.5 nA for the entire Error Amplifier structure.

$$I_{q,EA,AVG} = DI_{q,ON,EA} = \frac{6.25}{100} \times 40nA \approx 2.5nA \tag{3.7}$$

3.3 Boosted Voltage Generation

In order to properly operate the NMOS device in the linear region and guarantee the required current capability, the gate voltage must be higher than the output voltage by at least the required gate-source voltage:

$$V_{\text{Gate}} \geq V_{\text{OUT}} + V_{\text{GS}} \tag{3.8}$$

This condition becomes particularly critical in low dropout operation, where the input voltage is very close to the regulated output voltage. In this condition, the available voltage headroom is not sufficient to directly drive the gate of the NMOS pass transistor from the supply voltage. Therefore, an additional voltage boosting circuit is required to generate a gate voltage higher than V_{IN}.

3.3.1 Cross-coupled Charge Pump

The selected topology for the proposed design is a cross-coupled charge pump. This architecture provides several advantages, particularly for low-voltage and low-power applications. The circuit operates through two complementary clock phases with opposite voltage levels, which alternately control the charging and discharging phases of the flying capacitors. Thanks to the cross-coupled configuration, the MOS transistors are driven as active switches.

As shown in Fig. 3.11, the operation of the cross-coupled charge pump can be described as follows. The circuit is driven by two non-overlapping clock phases, Φ_{A} and Φ_{B} which swing between GND and V_{DDA}. During the phase in which Φ_{A} is low and Φ_{B} is high, node V_1 is pulled down towards V_{DDA}, while node V_2 is boosted to the charge pump output voltage V_{CP}. In this condition, M_{N1} and M_{P2} are turned on, whereas M_{N2} and M_{P1} are

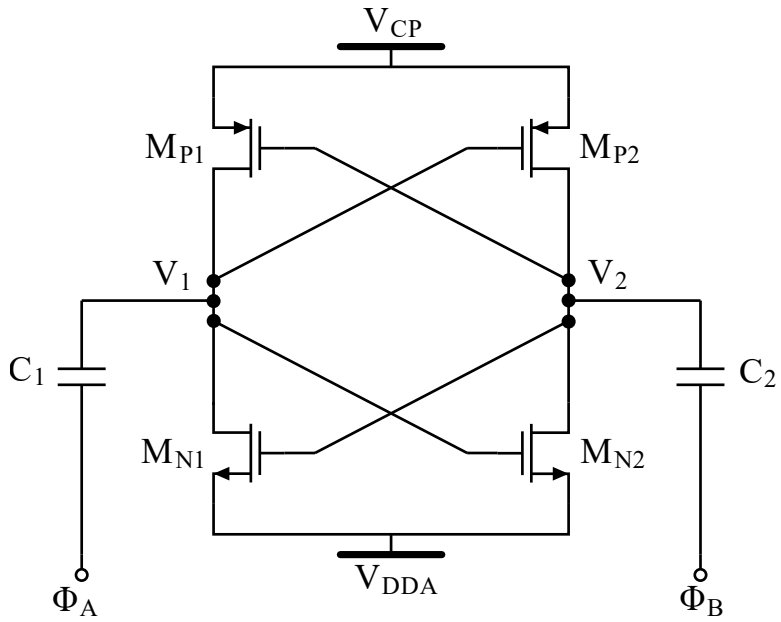


Figure 3.11: Cross Coupled Charge Pump.

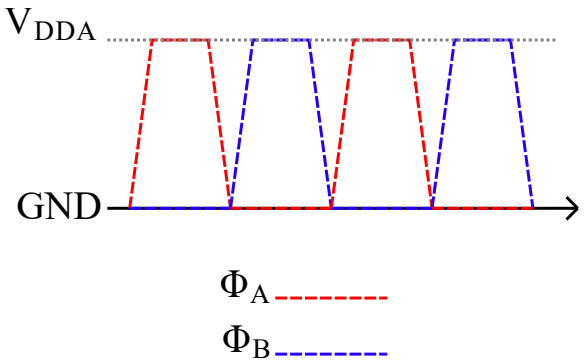


Figure 3.12: Disoverlapped Control Signals.

turned off. Consequently, the output node is connected to V_2 through the conducting M_{P2} transistor, transferring the boosted voltage to the output. At the same time, the top plate of capacitor C_1 is charged to V_{DDA} through the conducting transistor M_{N1}.

During the complementary phase, when Φ_A is high and Φ_B is low, the circuit operation is reversed. M_{N2} and M_{P1} are turned on, while M_{N1} and M_{P2} are turned off. The top plate of capacitor C_2 is charged to V_{DDA} through M_{N2}, and the output node is connected to the boosted node V_1 through the conducting M_{P1} transistor.

The voltage boosting capability of the switched-capacitor charge pump relies on the fundamental property of capacitors that their voltage cannot change

instantaneously. In fact, the voltage across a capacitor is related to the stored charge according to:

$$V_{\mathrm{c}} = \frac{Q}{C} \tag{3.9}$$

and the capacitor current relationship is defined as:

$$i_{\mathrm{c}} = C\frac{dV_{\mathrm{c}}}{dt} \tag{3.10}$$

Equation (3.10) states that any instantaneous variation of the capacitor voltage would require an infinite current. Therefore, when the clock signals change the connection of the capacitor terminals, the charge stored on the flying capacitors is preserved, causing the capacitor voltage to be transferred and added to the supply voltage. This charge transfer mechanism allows the generation of a voltage higher than the input supply voltage.
During each phase one capacitor is charged while the other transfers its stored energy to the output node. By alternately transferring charge between the flying capacitors and the output node, the output voltage is progressively increased until it reaches the boosted voltage V_{CP}.

3.4 Clock Generation Circuit for Charge Pump Driving

3.4.1 Voltage-Controlled Oscillator

To efficiently drive the switched-capacitor charge pump, sharp clock signals with fast rise and fall times are required in order to minimize switching losses and maximize the voltage conversion efficiency. For this reason, a dedicated clock generation and conditioning circuit is implemented.

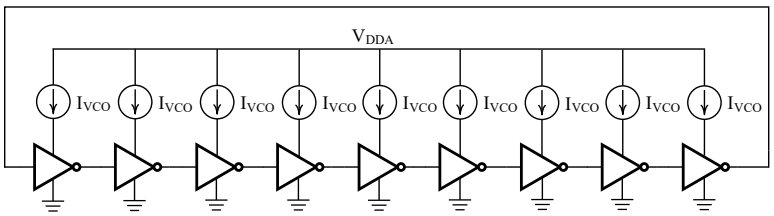


Figure 3.13: Current-starved Voltage-Controlled Oscillator.

The proposed circuit employs a current-starved Voltage-Controlled Oscillator as the clock generator. In a current-starved architecture, the oscillation frequency is determined by the bias current supplied to the delay stages. This topology is particularly suitable for ultra-low-power applications because the oscillation frequency can be accurately controlled while maintaining a very low static current consumption. Since the proposed LDO

is required to regulate the output voltage over a wide load current range, including the no-load condition, minimizing the quiescent current is one of the primary design objectives. Therefore, the bias current of the VCO is made dependent on the load current. At light loads, the VCO operates at a lower frequency, reducing the power consumed by both the oscillator and the charge pump. As the load current increases, the oscillation frequency is increased to provide sufficient charge transfer and maintain the boosted gate voltage required to properly drive the NMOS pass transistor under all operating conditions. The proposed VCO shown in Fig. 3.13, consists of a nine-stage inverter ring oscillator. Under no-load and light-load conditions, each delay stage is biased by a fixed current of 1 nA, resulting in extremely low power consumption during the idle operating mode. To ensure adequate charge pump performance over the entire load current range, an adaptive bias current generator is also implemented. As the load current increases, the adaptive circuit injects additional current into each delay stage, thereby increasing the oscillation frequency of the VCO. Consequently, the charge pump is able to deliver a higher output current, maintaining the boosted gate voltage required to properly drive the NMOS pass transistor under heavier load conditions.

The oscillation frequency f_{osc} of a current-starved ring oscillator is determined by the propagation delay of each inverter stage. Considering an N-stage ring oscillator, the oscillation frequency can be approximated as:

$$f_{\text{osc}} = \frac{1}{2Nt_{\text{p}}} \tag{3.11}$$

where N is the number of inverter stages and t_{p} is the propagation delay of a single stage. Since each inverter is current-limited, the propagation delay can be approximated as:

$$t_{\text{p}} \approx \frac{C_{\text{L}}\Delta V}{I_{\text{D}}} \tag{3.12}$$

where C_{L} is the effective load capacitance of each stage, ΔV is the output voltage swing, and I_{D} is the bias current supplied by the current-starving transistors. Substituiting (3.12) into (3.11) yields

$$f_{\text{osc}} \approx \frac{I_{\text{D}}}{2NC_{\text{L}}\Delta V} \tag{3.13}$$

Equation (3.13) shows that the oscillation frequency is approximately proportional to the bias current:

$$f_{\text{osc}} \propto I_{\text{D}} \tag{3.14}$$

Therefore, increasing the VCO bias current I_{VCO} reduces the propagation delay of each inverter stage and consequently increases the oscillation frequency. In the proposed architecture, the bias current is composed of a fixed

component of 1 nA I_{VCOfix} per stage and an adaptive component I_{VCOadp} that increases with the load current. As a result:

$$I_{\mathrm{VCO}} = I_{\mathrm{VCOfix}} + I_{\mathrm{VCOadp}} \tag{3.15}$$

3.4.2 4 Phases Level Shifter

Unfortunately, the proposed VCO does not provide a full-swing square waveform at its output. Therefore, its output signal cannot be directly used to drive the charge pump switches efficiently. The slow transition edges generated by the VCO may lead to incomplete switching of the charge pump transistors, increasing conduction losses and potentially causing unwanted simultaneous conduction between complementary devices. These effects can significantly degrade the charge pump efficiency and introduce additional power consumption. For this reason, an additional level-shifting and waveform-conditioning stage is implemented. The level shifter converts the VCO output signal into a sharp full-swing digital waveform, providing adequate voltage levels and driving capability for the subsequent circuitry.
The design of the level shifter also requires careful consideration of possible short-circuit or cross-conduction losses. This aspect becomes particularly critical when the input signal generated by the VCO exhibits slow transition edges rather than an ideal square waveform. During these transitions, the pull-up and pull-down devices of the level shifter may operate simultaneously in the conduction region, creating a direct current path between the supply rails and increasing power consumption. To mitigate this effect, a four-phase level shifter architecture is implemented. This approach ensures a controlled sequential switching operation of the MOS transistors, avoiding the simultaneous activation of complementary devices in the same branch.
As illustrated in Fig. 3.14 the proposed level shifter is controlled by four clock phases and implements a sequential turn-on and turn-off operation of the MOS transistors. The main objective of this approach is to guarantee a break-before-make operation, preventing the simultaneous conduction of the pull-up and pull-down networks.
The implementation of this structure requires multiple clock phases generated by the VCO as shown in Fig. 3.15, to properly control the turn-on and turn-off of the MOS transistors.
To generate the required control phases for the level shifter, different VCO phases must be appropriately combined. The required logical operations are implemented through AND-like structures using series-connected MOS transistors, where each transistor is controlled by a different VCO phase. By appropriately selecting the phases to be combined, the required control signals for the level-shifter stages are generated. The selected VCO phases and the corresponding combined signals are shown in Fig. 3.16.

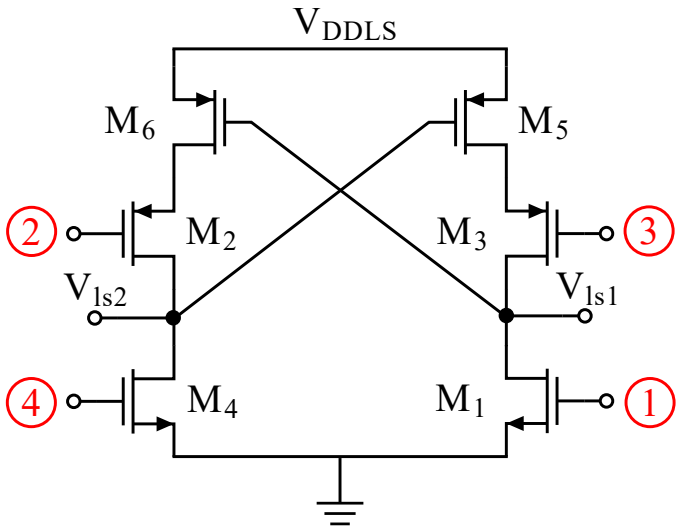


Figure 3.14: Proposed 4-Phase Level Shifter.

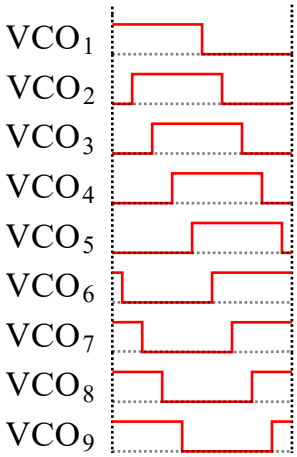


Figure 3.15: Phases of 9-stage VCO

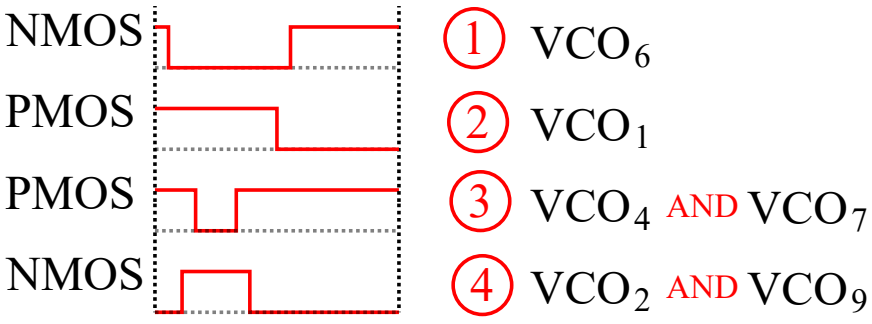


Figure 3.16: Combined VCO phases

During the first transition, M_1 (NMOS) is turned off first, together with M_2 (PMOS). As a result, the pull-down path on the right branch is disabled, allowing the pull-up transistor M_3 to be activated. A similar sequence occurs in the left branch, where the pull-up transistor M_2 is turned off before the pull-down transistor M_4 is activated. During the following transition, M_4 and M_3 are turned off first to prevent cross-conduction. Only after these devices have been completely turned off, M_1 and M_2 are turned on. By introducing a controlled delay between the turn-off of one device and the turn-on of its complementary device, the proposed four-phase control scheme ensures that the pull-up and pull-down branches are never simultaneously active.

The implemented level shifter is not primarily intended to perform a conventional voltage translation from a low-voltage input swing to a rail-to-rail output swing. Instead, its main purpose is to reshape and regenerate the waveform generated by the VCO, providing a sharper digital-like signal suitable for driving the subsequent blocks. For this reason, achieving a complete voltage swing between GND and V_{DDA} is not a strict requirement at this stage, since the final full-swing control signals required to drive the charge pump switches are generated by the following conditioning stages.

A critical aspect of this implementation is related to the variation of the VCO output voltage swing. Since the VCO is based on an adaptive current-starved architecture, the oscillation frequency and the output waveform amplitude can vary depending on the bias current. In particular, at different load current conditions, the VCO output voltage may not reach the same voltage levels, potentially affecting the correct switching operation of the level shifter. To overcome this limitation, an adaptive voltage control mechanism is introduced. In particular, the gate voltage driving the PMOS pull-up devices must be sufficiently high to completely turn them off when required. Otherwise, incomplete switching could occur, creating an unwanted current path between the supply rails and increasing power consumption.

As illustated in figure Fig. 3.17, the adaptive voltage mechanism is composed of a diode and a capacitor, which together form a voltage rectifier (or peak detector). The circuit receives one of the VCO output signals and rectifies the oscillating waveform, ideally generating a DC voltage level (V_{DDLS}) approximately equal to the maximum amplitude reached by the VCO output. The generated voltage is then applied to the gate of a native MOS transistor. A native MOS device is characterized by a very low threshold voltage compared with standard MOS transistors, allowing it to operate with a reduced gate-source voltage.

$$V_{\mathrm{GS,native}} \approx 0 \tag{3.16}$$

This feature enables the transistor to provide the required bias current for the level shifter while maintaining proper operation even when the avail-

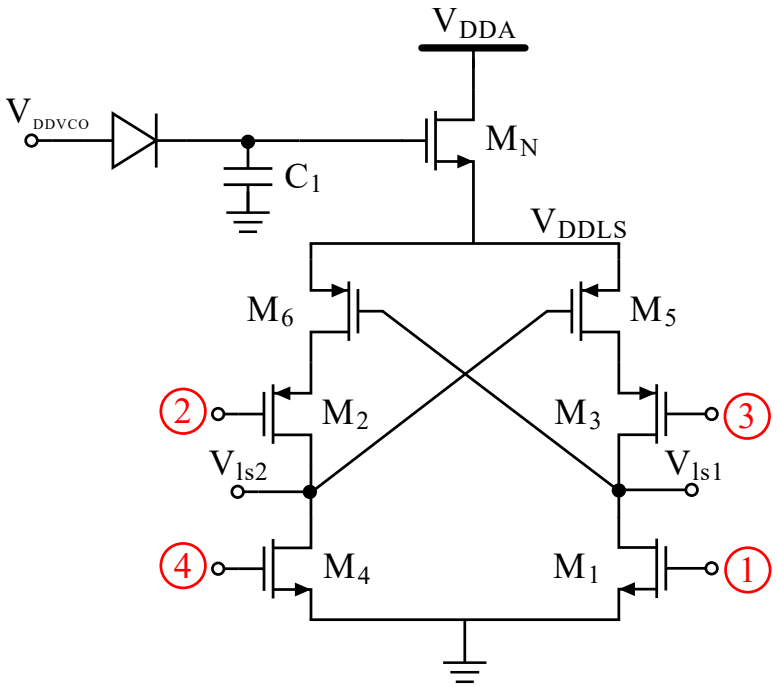


Figure 3.17: Proposed 4-Phase Level Shifter with adaptibe voltage mechanism.

able control voltage is limited. By exploiting the rectified voltage generated from the VCO output, the adaptive mechanism automatically adjusts the bias conditions of the level shifter according to the actual waveform amplitude. This ensures reliable switching operation over the entire range of oscillation frequencies and load conditions, preventing incomplete transistor turn-off and minimizing unwanted conduction paths. The complete circuit implementation is shown in Fig. 3.18.
By combining all these techniques, the proposed level shifter achieves a current consumption under no-load conditions of approximately:

$$I_{\text{Level-Shifter}} \approx 2.3nA \tag{3.17}$$

3.4.3 Non-Overlapping Clock Generation for Charge Pump Control

Disoverlap circuit

To efficiently control the charge pump, high-quality clock signals with sharp transition edges and adequate voltage swing are required. The output signals generated by the level shifter cannot directly drive the charge pump switches because they do not provide a complete rail-to-rail voltage swing

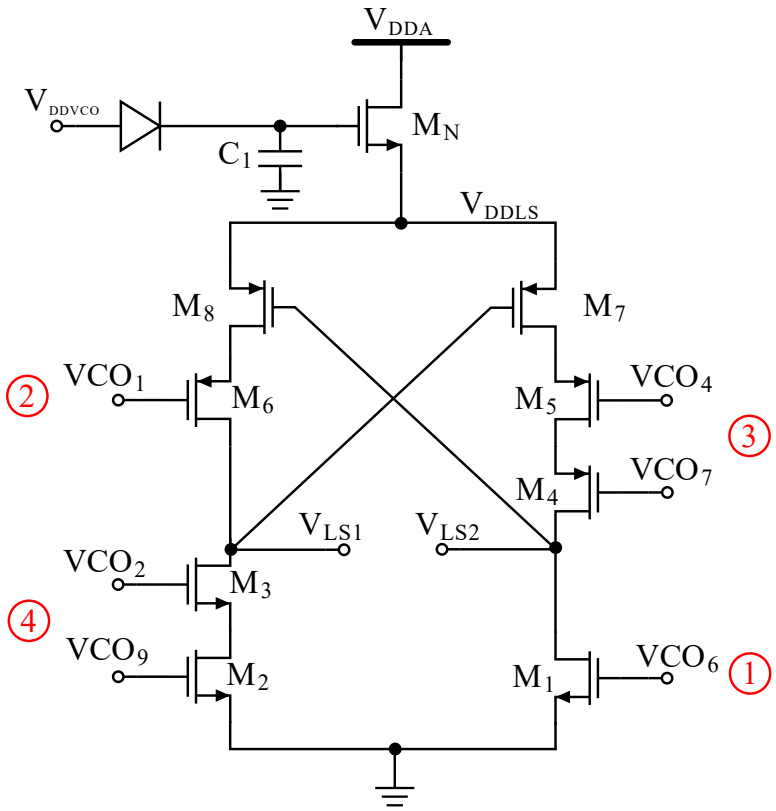


Figure 3.18: Implementation of proposed Level Shifter.

and still exhibit limited transition speed due to the non-ideal waveform generated by the VCO, that would result in incomplete switching of the charge pump transistors, increasing switching losses and potentially introducing undesired conduction paths. For this reason, an additional conditioning stage is required. This stage includes a non-overlapping clock generation circuit, which guarantees the correct timing relationship between complementary control signals, and dedicated drivers.

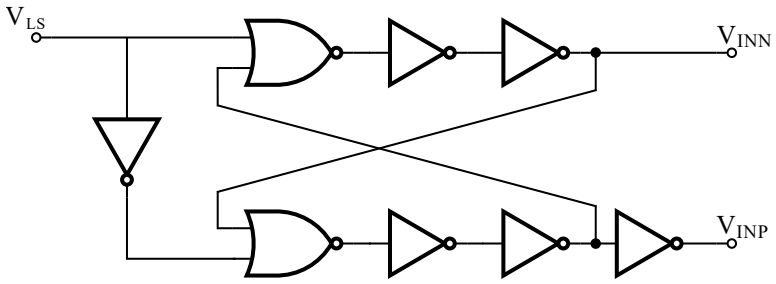


Figure 3.19: Disoverlap Circuit.

Figure Fig. 3.19 shows the proposed non-overlapping clock generation circuit, which produces two clock signals with a controlled dead time between their transitions. These non-overlapping waveforms are used to drive the subsequent inverter stages, preventing simultaneous conduction of the pull-up PMOS and pull-down NMOS transistors, which represents one of the major sources of dynamic power dissipation in CMOS switching circuits. This timing relationship guarantees that one switching network is completely turned off before the complementary one is activated, thereby eliminating short-circuit current paths during signal transitions. The input signal of the circuit is one of the two output signals generated by the level shifter. As in the previously described conditioning stages, an insufficient overdrive voltage across the PMOS devices of the logic ports may prevent them from being fully turned off. This can lead to unwanted cross-conduction currents, thereby increasing the quiescent power consumption of the circuit.

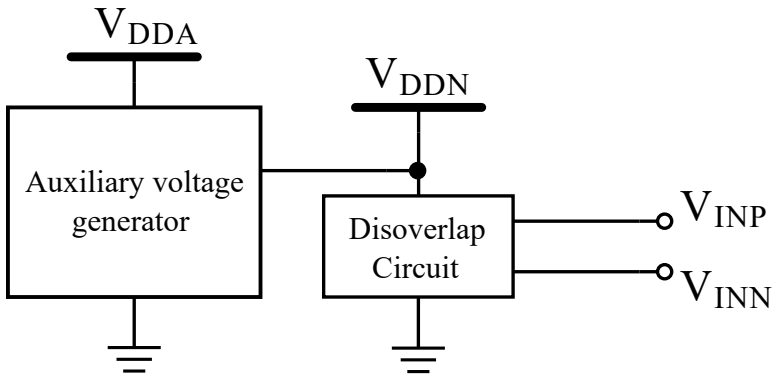


Figure 3.20: Disoverlap circuit with auxiliary voltage block diagram.

As illustrated in Fig. 3.21, to overcome this issue, an auxiliary bias voltage is generated using a constant current source of 5 nA and two diode-connected devices. The resulting voltage is approximately equal to two diode voltage drops. The generated auxiliary bias voltage is then applied to the gate of a native NMOS transistor. Owing to its very low threshold voltage, the native device operates as a voltage buffer with enhanced current driving capability, reproducing the generated bias voltage at its output while providing sufficient current to drive the subsequent non-overlapping circuit.

$$V_{\mathrm{AUX}} \approx V_{\mathrm{DDN}} \tag{3.18}$$

This auxiliary voltage is always lower than the voltage swing of the control signal, ensuring sufficient overdrive to completely turn off the PMOS transistors during the transition intervals, even when the input waveform exhibits reduced voltage swing. Consequently, unwanted conduction paths are avoided, allowing the non-overlapping logic to operate with very low power consumption while maintaining reliable switching behavior across the

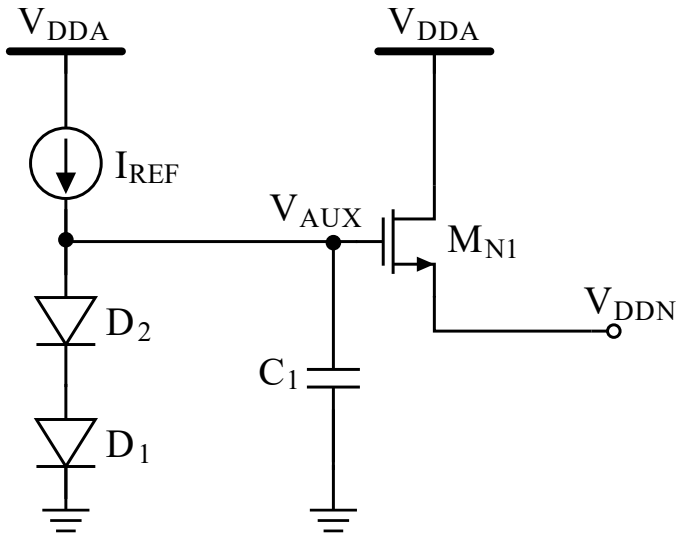


Figure 3.21: Auxiliary voltage generation circuit.

entire operating range. The resulting total current consumption of the logic is approximately:

$$I_{\text{Logic}} \approx 10nA \tag{3.19}$$

Charge-Pump Drivers

The final stage of the clock generation chain consists of the output drivers, whose purpose is to generate full-swing control signals for the charge pump. To achieve this objective, CMOS inverters are employed. A critical issue arises because the inputs of these inverters are the outputs of the non-overlapping circuit, whose voltage swing is limited by the auxiliary bias voltage previously introduced. Consequently, if these signals were applied directly to the gate of the pull-up PMOS transistor, the gate voltage would never reach a sufficiently high level to completely turn the device off. As a result, the source-to-gate voltage, $V_{\text{SG,p}}$ would remain greater than the threshold voltage $V_{\text{TH,p}}$, causing the PMOS transistor to remain partially conductive. Under these conditions, when the pull-down NMOS transistor turns on, both transistors may conduct simultaneously, creating an undesired short-circuit current path between the supply rails. To overcome this limitation, the solution shown in Fig. 3.22 is adopted.
In the proposed solution, two diode-connected MOS transistors are employed together with the coupling capacitor C_{C}. The output signal of the non-overlapping circuit is AC-coupled through C_{C}, while the diode-connected devices establish the DC bias level of the PMOS gate. As a result, the gate voltage of the pull-up PMOS swings between V_{DDA} and approximately

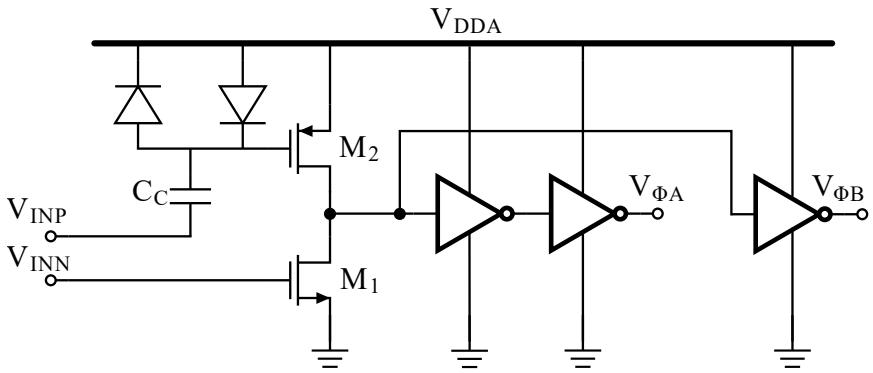


Figure 3.22: Charge Pump drivers circuit.

one diode voltage drop below V_{DDA}. This voltage excursion is sufficient to ensure both a strong turn-on and a complete turn-off of the PMOS transistor during each switching cycle. Consequently, simultaneous conduction of the pull-up PMOS and pull-down NMOS transistors is effectively prevented. This simple yet effective solution significantly reduces cross-conduction current during the switching transitions, thereby minimizing the dynamic power consumption of the driver stage, especially in light load condition. The subsequent inverter stages generate two complementary full-swing clock signals with sharp transition edges, providing the control signals required to efficiently drive the charge pump. In this way, the charge pump can be properly controlled to generate the required boosted output voltage over the entire load-current range. Table 3.1 summarizes the relationship between the load current and the VCO oscillation frequency and, consequently, the switching frequency of the control signals driving the charge pump. As the load current increases, the VCO frequency is increased accordingly, providing the charge pump with a higher switching frequency to sustain the required boosted voltage under heavier load conditions.

3.5 Voltage Buffer

The buffer at the output of the error amplifier is a fundamental block for properly driving the NMOS pass transistor. Since the gate voltage of the NMOS must be raised above the available input supply voltage to provide sufficient gate-to-source overdrive, the buffer is biased using the boosted voltage V_{CP} generated by the charge pump. This allows the gate voltage of the pass transistor to exceed the input voltage V_{IN} when required. This feature is particularly important under low-dropout conditions, where the input voltage approaches the regulated output voltage and the available voltage headroom across the pass transistor is significantly reduced.
The proposed buffer is illustrated in Fig. 3.23 and is implemented using a

I_{LOAD}	f_{osc}
0 A	17.2 KHz
100 μA	19 KHz
10 mA	340 KHz
20 mA	728 KHz
30 mA	1.2 MHz
40 mA	1.51 MHz
50 mA	1.91 MHz
60 mA	2.3 MHz
70 mA	2.72 MHz
80 mA	3.12 MHz
90 mA	3.54 MHz
100 mA	3.96 MHz

Table 3.1: Dependency of f_{sw} on load current I_{LOAD}.

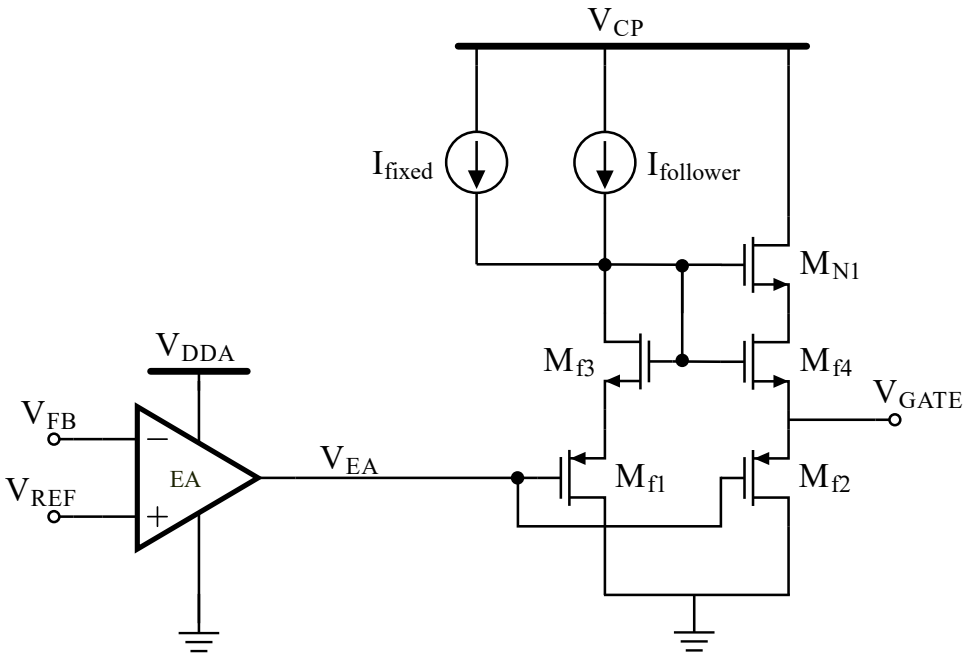


Figure 3.23: Proposed push-pull Buffer topology.

push-pull topology based on complementary NMOS and PMOS transistors. In this configuration, one transistor actively sources current to increase the output voltage, while the complementary device sinks current to decrease it. This configuration provides low output impedance and high current-driving capability, making it suitable for driving the large gate capacitance of the NMOS pass transistor. The buffer operates approximately as a voltage

follower, providing a voltage gain close to unity, while presenting a high input impedance and a low output impedance. This allows the control voltage generated by the error amplifier to be efficiently transferred to the gate of the pass transistor. The biasing network consists of two current sources: a 10 nA fixed bias current I_{fixed}, which maintains the internal nodes correctly biased and ensures proper operation even under no-load conditions, and an adaptive bias current I_{follower} controlled according to the load current. As the load current increases, the adaptive bias current is increased, providing higher current-driving capability and improving the dynamic response of the buffer. Conversely, under light-load conditions, the adaptive current is reduced to minimize the overall power consumption.
More specifically, the proposed buffer consists of a source-follower stage implemented by M_{f1} and M_{f2} whose gates are directly connected to the error amplifier output V_{EA}. This stage transfers the control voltage generated by the error amplifier to the subsequent output stage while providing the required current drive. The output push-pull stage is implemented by M_{f3} and M_{f4}. Proper voltage matching between these two devices is required to ensure the correct operation of the output stage. In particular, the biasing circuit is designed to maintain approximately equal gate-to-source voltages:

$$V_{GS,f3} = V_{GS,f4} \tag{3.20}$$

So that the two complementary devices are correctly biased and the buffer can generate the desired output voltage. Proper matching also helps minimize the static current flowing through the push-pull stage.
To minimize the static power consumption of the buffer, particularly under no-load conditions, the current flowing through the first branch (M_{f1}-M_{f3}) must be accurately matched to the current flowing through the push-pull branch (M_{f2}-M_{f1}). To achieve this condition, a native NMOS transistor M_{N1} is introduced to equalize the drain voltages of M_{f3} and M_{f4}. Since the native NMOS exhibits a gate-source voltage close to zero, it can be used to establish the required voltage relationship between the two branches, in particular the proposed biasing configuration ensures approximately:

$$V_{D,f3} \approx V_{D,f4} \tag{3.21}$$

allowing M_{f3} and M_{f4} to operate under closely matched terminal-voltage conditions. Together with the matching of their gate-source voltages, since the sizes of the two transistors are the same.

$$V_{GS,f3} \approx V_{GS,f4} \tag{3.22}$$

This improves the accuracy of the current mirroring between the two branches and minimizes the residual static current flowing through the push-pull stage under no load condition.

3.6 Stability and Compensation

This section analyzes the stability of the overall LDO feedback loop. Since the operating conditions of the proposed adaptive LDO vary significantly with the load current, the positions of the poles and zeros can change accordingly. Therefore, a stability analysis is performed over the entire load-current range to identify the main contributions to the loop transfer function and evaluate their impact on the phase margin and bandwidth. Based on this analysis, an appropriate compensation network is designed to ensure stable operation under all relevant operating conditions while maintaining the required bandwidth and transient performance of the LDO.

3.6.1 Stability analysis

To properly analyze the loop stability, two main operating conditions must be considered: the light-load and heavy-load regimes. The significant variation in the bias currents and transistor operating points between these two regimes results in substantial changes in the locations of the poles and zeros of the loop transfer function. Consequently, a compensation network designed for a single operating condition may not guarantee sufficient stability over the entire load-current range. The compensation strategy must therefore account for the variation of the loop dynamics with the load current and provide adequate phase margin and stability in both light-load and heavy-load conditions.

Small signal analysis

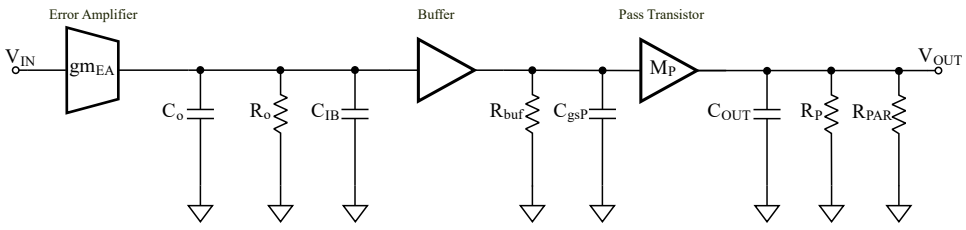


Figure 3.24: Small signal equivalent circuit.

Figure Fig. 3.24 illustrates the small-signal equivalent circuit of the LDO feedback loop. The main parasitic and small-signal elements are described as follows: C_{O} represents the output capacitance of the error amplifier, while C_{IB} is the input capacitance of the buffer. R_{O} denotes the output resistance of the error amplifier, and R_{buf} represents the output resistance of the buffer. The input capacitance of the NMOS pass transistor is mainly represented by its gate-source capacitance C_{gsP}. At the LDO output C_{OUT} represents the output capacitance, while R_{P} denotes the output resistance of the pass

transistor. Finally, R_{PAR} represents the equivalent impedance associated with the feedback network.
The principal poles and zeros are:

- $$\omega_{P0} = \frac{1}{R_O(C_O + C_{IB})} \tag{3.23}$$
- $$\omega_{P1} = \frac{1}{C_{OUT}(R_P||R_{PAR})} \tag{3.24}$$
- $$\omega_{P2} = \frac{1}{C_{gsP}R_{buf}} \tag{3.25}$$
- $$\omega_{zESR} = \frac{1}{C_{OUT}ESR} \tag{3.26}$$

Where ω_{P0} is the pole associated to the output of Error Amplifier, ω_{P1} is the pole associated to the LDO's output node. ω_{P2} is the pole associated to the input capacitance of NMOS Pass Transistor and ω_{zESR} is the zero associated to the ESR parasitic resistance of output capacitance C_{OUT}.
Under light-load conditions, the dominant pole is located at the output node of the error amplifier ω_{P0}. The output resistance at this node is mainly determined by the parallel combination of the drain-source resistances of the transistors connected to the node. Since the error amplifier operates with very low bias currents in this operating regime, transistors operate in the subthreshold region, resulting in a relatively high small-signal output resistance. Consequently, the large output resistance, together with the parasitic capacitance at the error amplifier output, generates a low-frequency pole that becomes the dominant pole of the overall loop. In first approximation, its frequency location can be expressed as:

$$f_{P0} = \frac{1}{2\pi R_O(C_O + C_{IB})} \tag{3.27}$$

$$R_O = (r_{ds}||r_{ds}) \tag{3.28}$$

The first non-dominant pole is associated with the output node of the LDO. This pole is mainly determined by the output resistance of the pass transistor and the total output capacitance. Its approximate location can therefore be expressed as:

$$f_{P1} = \frac{1}{2\pi C_{OUT}(R_P||R_{PAR})} \tag{3.29}$$

Where the LDO's output node impedance is dominated by the output impedance of NMOS Pass transistor:

$$R_P = \frac{1}{g_{m,Mp}} \tag{3.30}$$

$$f_{P1} \approx \frac{g_{m,Mp}}{2\pi C_{OUT}} \tag{3.31}$$

Since the output resistance of the pass transistor depends on the load current and its operating region, the location of this pole varies significantly with the operating condition of the LDO.
The second non-dominant pole is associated with the output node of the buffer. This pole is mainly determined by the buffer output resistance R_{buf} and the input capacitance of the NMOS pass transistor C_{gsP}. Under light-load conditions, the output impedance of the buffer is mainly determined by the transconductance of its output devices. Since the buffer is biased with a very low current in this operating regime, its g_{m} is relatively small, resulting in a high output resistance, approximately:

$$R_{buf} \approx \frac{1}{g_{m,buf}} \tag{3.32}$$

Consequently, the pole associated with the buffer output node is approximated as:

$$f_{P2} \approx \frac{g_{m,buf}}{2\pi C_{gsP}} \tag{3.33}$$

Although the low bias current under light-load conditions results in a relatively low g_{m}, the buffer transistors are sized with a large width to maintain a sufficiently high transconductance. This design choice ensures that the pole associated with the buffer output node remains at a relatively high frequency and therefore does not become the dominant pole of the loop also in light load condition.
The last contribution to the loop transfer function is given by the zero associated with the ESR of the output capacitor C_{OUT}. The ESR is estimated to be approximately $10\,\mathrm{m\Omega}$. Therefore, the corresponding ESR zero is located at a relatively high frequency and does not significantly affect the loop dynamics within the frequency range of interest. The zero frequency can be approximated as:

$$f_{zESR} \approx \frac{1}{2\pi ESR C_{OUT}} \tag{3.34}$$

For the considered ESR value, the zero is located at approximately:

$$f_{zESR} \approx 16MHz \tag{3.35}$$

Since this frequency is significantly higher than the relevant pole frequencies of the LDO loop, the ESR zero can be considered negligible in the stability

analysis over the operating conditions of interest. The main issue under light-load conditions is the proximity between the dominant pole associated with the output node of the error amplifier and the non-dominant pole associated with the LDO output node. Since these two poles are located within a similar frequency range, they can introduce a significant phase shift before the loop reaches its unity-gain frequency, potentially reducing the phase margin and compromising the stability of the overall feedback loop. Therefore, an appropriate compensation strategy is required to sufficiently separate the two poles and ensure an adequate phase margin under light-load conditions.
Under heavy-load conditions, the dominant pole ω_{P0} remains associated with the output node of the error amplifier. In this operating regime, the output impedance of the error amplifier is mainly determined by the drain-source output resistances r_{ds} of the transistors connected to the output node, which operate in saturation. The first non-dominant pole ω_{P1} is still associated with the LDO output node and is mainly determined by the output impedance of the NMOS pass transistor and the output capacitance C_{OUT}. The second non-dominant pole ω_{P2} is associated with the output node of the buffer. Under heavy-load conditions, the adaptive biasing increases the buffer current and consequently its transconductance g_m. The resulting reduction in the buffer output impedance shifts ω_{P2} toward higher frequencies. Therefore, unlike the light-load condition, where the error-amplifier output pole and the LDO output pole can become relatively close in frequency, under heavy-load conditions the increased bias currents modify the pole locations and improve the frequency separation between the relevant poles. This analysis shows that, under light-load conditions, a dedicated compensation network is required to ensure adequate loop stability by properly modifying the relative positions of the dominant and non-dominant poles. As the load current increases, the pole locations change due to the adaptive biasing of the different blocks. Above a certain load-current level, the compensation is no longer primarily required to guarantee stability, but rather becomes a means of extending the loop bandwidth by introducing an appropriate zero in the transfer function.

3.6.2 Compensation network

As discussed in the previous subsection 3.6.1, a compensation network is required to ensure the stability of the overall feedback loop over the entire load-current range. Since the positions of the relevant poles vary significantly with the operating condition, a fixed compensation zero would not provide optimal phase compensation across the entire load range. For this reason, a zero-tracking compensation technique is adopted. The proposed compensation network introduces a movable zero whose frequency is automatically adjusted according to the load current. As the operating condition

changes, the zero tracks the variation of the dominant and non-dominant poles, providing an adequate phase contribution over the entire load-current range. In this way, the phase margin is maintained above the required value, ensuring stable operation of the LDO under both light- and heavy-load conditions.
A critical issue arises under no-load and very light-load conditions, where the zero frequency must be located at a very low frequency range, approximately 15–25 Hz, to ensure adequate loop stability. Achieving such a low-frequency zero requires either a very large capacitance or a very high resistance in the zero-tracking compensation network. However, implementing a very large resistance using conventional on-chip techniques is challenging, while the use of a large capacitance introduces significant area overhead and increases the time required to charge and discharge the capacitor, affecting the response of the entire loop.
To overcome these limitations, a dedicated compensation technique is adopted. From the capacitance perspective, a fixed capacitor C_{Z} with a value of 5 pF is implemented. The required large equivalent resistance is instead obtained through a mixed approach. In particular, the resistance network is composed of two complementary elements:

1. a MOS transistor operating in the triode region
2. a switched-capacitor circuit that emulates a high-value resistive element

This approach allows the required low-frequency zero to be achieved without introducing an excessively large on-chip resistor or capacitor, thereby reducing the area overhead while maintaining the required tracking behavior.
As illustrated in Figure Fig. 3.25 , the equivalent impedance seen by the compensation capacitor is given by the shunt connection of the equivalent resistance of the MOS transistor operating in the triode region and the equivalent resistance generated by the switched-capacitor circuit. Therefore, the total equivalent resistance can be expressed as:

$$R_Z = R_{triode} // R_{sw} \tag{3.36}$$

The switched-capacitor circuit consists of a fixed capacitor C_{sw} and two NMOS transistors used as switches. The switching control signals Φ_1 and Φ_2 are generated using the same clock-generation circuitry previously described in Section 3.4 for the charge-pump control signals.
The switched-capacitor circuit is driven by two complementary non-overlapping clock signals with the same switching frequency. Under the assumption of ideal switches and non-overlapping operation, the circuit can be modeled as an equivalent resistive element. The corresponding equivalent resistance can be expressed as:

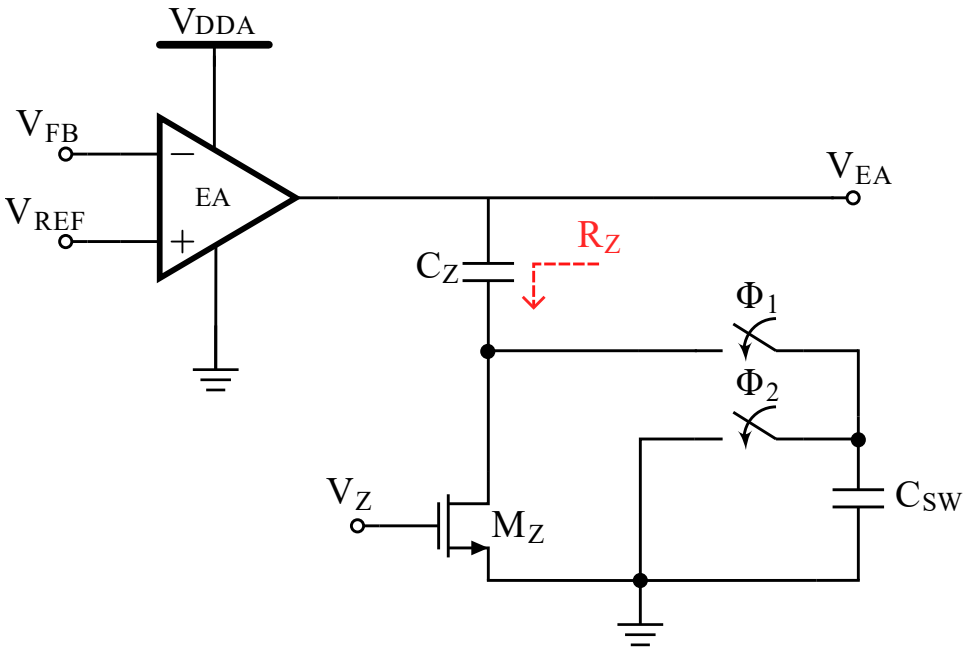


Figure 3.25: Proposed Zero-Tracking Compensation network.

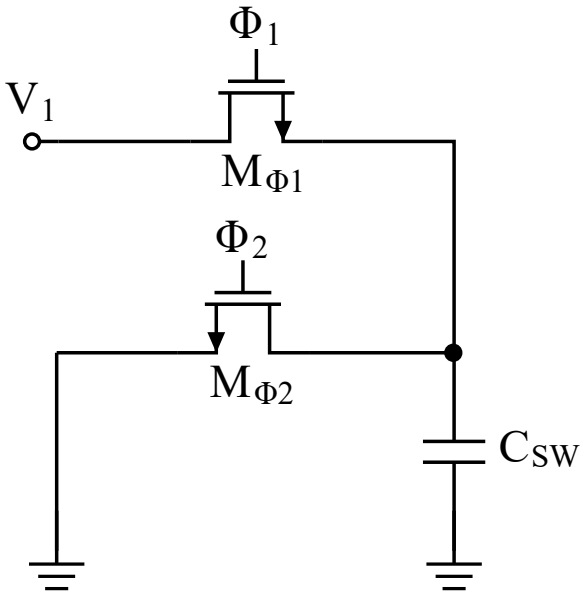


Figure 3.26: Switched-Capacitor resistor.

$$R_{SC} = \frac{1}{f_{sw} C_{sw}} \tag{3.37}$$

where f_{sw} is the switching frequency. Therefore, the equivalent resistance

can be controlled by adjusting the switching frequency, allowing the zero-tracking compensation network to modify the location of the compensation zero according to the load current.
The operating principle of the proposed compensation network can be described as follows. Under no-load and very light-load conditions, the switching frequency of the two control signals is relatively low. Consequently, the switched-capacitor circuit generates a very high equivalent resistance. At the same time, the gate of the triode MOS is driven by a very low control voltage, well below its threshold voltage, causing the MOS transistor to remain substantially turned off and therefore providing a very high equivalent resistance. Under these conditions, the switched-capacitor contribution is the dominant component determining the equivalent resistance of the compensation network. As the load current increases, the switching frequency also increases, consequently the equivalent resistance generated by the switched-capacitor circuit decreases. However, this resistance remains too high to provide the required zero frequency over the corresponding operating range. At the same time, the control voltage applied to the gate of the triode MOS increases with the load current. As the gate voltage increases, the equivalent resistance of the MOS operating in the triode region decreases according to:

$$R_{triode} \approx \frac{1}{\mu C_{OX} \frac{W}{L} (V_{GS} - V_{TH)}} \tag{3.38}$$

By appropriately sizing the width-to-length ratio (W/L) of the triode-operated MOS transistor, the required equivalent resistance can be obtained to achieve the desired zero location and ensure adequate loop stability. The combined effect of the two mechanisms therefore allows the total equivalent resistance to decrease progressively with increasing load current, enabling the compensation zero to track the required frequency and maintain adequate loop stability over the entire load-current range.

3.7 Feedback network

Another fundamental block for the correct operation of the LDO is the feedback network. In a conventional implementation, the feedback network consists of a resistive divider with a suitable resistance ratio, which scales the output voltage to a value compatible with the reference voltage generated by the bandgap circuit. In a nano-power LDO, however, the implementation of the feedback network is particularly challenging because of the stringent quiescent-current requirements. Even under no-load conditions, the resistive divider continuously draws a current from the output node. This current can be expressed as:

$$I_{FB} = \frac{V_{OUT}}{R_{FB1} + R_{FB2}} \tag{3.39}$$

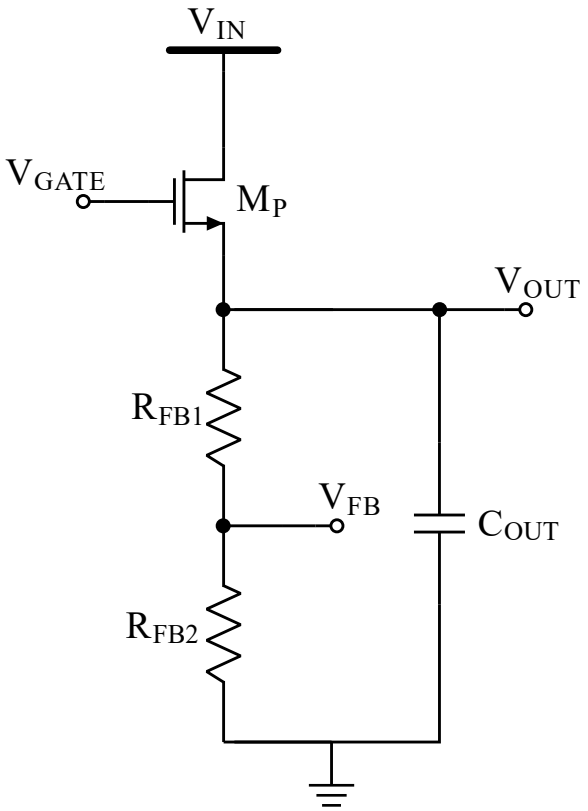


Figure 3.27: Conventional Resistive Feedback Network.

Therefore, to minimize the current consumption of the feedback network, very large resistance values are required. This introduces a significant design trade-off, since excessively large on-chip resistors can result in increased silicon area and may also introduce additional parasitic effects. For the proposed application, a maximum current consumption of approximately 20 nA is considered a suitable target. The required feedback voltage is V_{FB}= 600 mV, obtained from a regulated output voltage V_{OUT}= 1.8 V. Therefore, a resistive divider with a division ratio of 3 is required. To meet this stringent current-consumption requirement, two possible approaches are considered:

1. **Resistive Feedback:** a conventional resistive divider can be implemented using R_{FB1}= 60 MΩ and R_{FB2}= 30 MΩ. This configuration provides the required 600 mV feedback voltage while drawing approximately 20 nA from the output.

$$I_{FB} = \frac{V_{OUT}}{R_{FB1} + R_{FB2}} = \frac{1.8V}{90\mathrm{M}\Omega} = 20nA \tag{3.40}$$

2. **Sampled Feedback:** alternatively, a sampled-feedback technique can be investigated to further reduce the static current consumption of the

feedback network by avoiding a continuous DC current path between the output and ground.

The sampled feedback consists of a resistive divider controlled by two switches driven by a periodic control signal. The switches periodically enable and disable the feedback path, resulting in a duty-cycled operation. In this way, the average power consumption of the feedback network can be reduced proportionally to the duty cycle.

$$I_{q,AVG} = DI_{q,ON} \tag{3.41}$$

This technique is investigated to overcome the main limitations of conventional resistive feedback, particularly in nano-power LDOs. By exploiting the duty-cycled operation of the sampled feedback, lower resistance values can be employed while maintaining the same average power consumption. As a result, both the silicon area occupied by the feedback network and its associated parasitic capacitances can be significantly reduced.

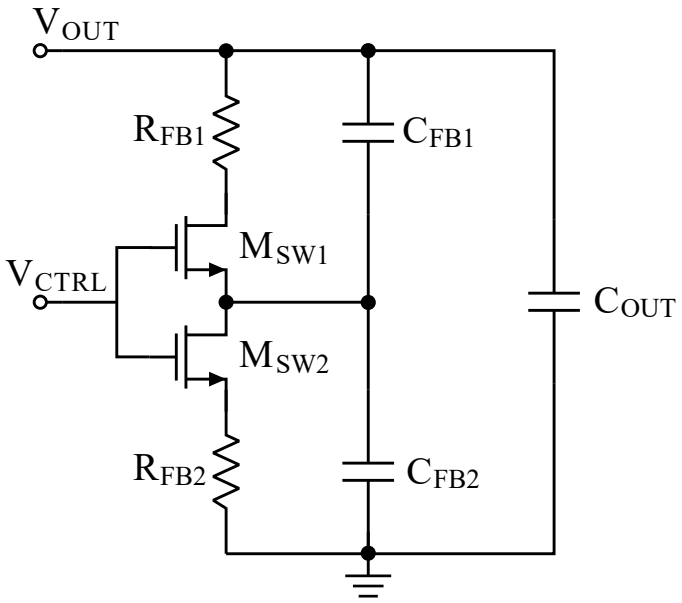


Figure 3.28: Sampled Resistive Feedback Network.

The implementation of this network is shown in Fig. 3.28. It consists of two feedback resistors R_{FB1}, R_{FB2} and two NMOS transistors used as switches, which are controlled by a signal V_{CTRL} with a reduced duty cycle. An important aspect to consider when implementing the feedback network using real resistors, is the parasitic capacitance associated with large resistance values.
These parasitic capacitances are mainly referred to ground and must be periodically charged and discharged, causing unwanted voltage variations at

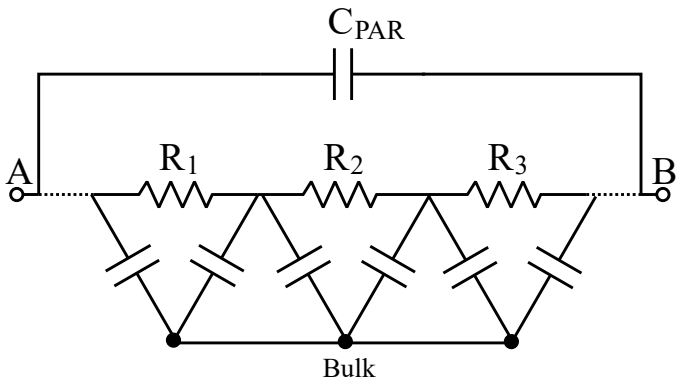


Figure 3.29: Equivalent model of real resistances.

the output node. To mitigate this effect, the resistance values are carefully selected to minimize the associated parasitic capacitances while maintaining the required low feedback current. However, a trade-off must be considered between minimizing the feedback current and limiting the effects of the parasitic capacitances. A divide-by-16 counter is employed to generate a control V_{CTRL} signal with a duty cycle D = 3.125 %. The counter is based on the same architecture used for the Error Amplifier described in Section 3.2, with an additional stage added to implement the divide-by-16 operation. The counter is driven by an external clock signal already available in the system, with a fixed frequency of 32 kHz. The resulting low-duty-cycle control signal is used to periodically activate the feedback network. With this control scheme, the sizing of the feedback resistors is determined by a trade-off between minimizing the feedback current consumption and limiting the degradation of the output voltage accuracy caused by parasitic capacitances associated with the resistors.

R_{FB1}	R_{FB2}	V_{OUT}	**err%**	$I_{feedback}$
6 MΩ	3 MΩ	1.74 V	3.33%	6 nA
3 MΩ	1.5 MΩ	1.786 V	0.77%	12.5 nA
2 MΩ	1 MΩ	1.794 V	0.33%	17.75 nA
1.5 MΩ	750 kΩ	1.7958 V	0.23%	25 nA
1 MΩ	500 kΩ	1.7973 V	0.15 %	38 nA

Table 3.2: Dependency of feedback network current consumption $I_{feedback}$ and output voltage accuracy on Feedback resistances variation.

Table 3.2 shows the variation in feedback-network current consumption and output-voltage accuracy as a function of the feedback resistances values. A suitable trade-off is achieved by selecting $R_{\mathrm{FB1}} = 2\mathrm{M}\Omega$ and $R_{\mathrm{FB2}} = 1\mathrm{M}\Omega$, resulting in an output-voltage error of 0.33 %. The current consumption of the feedback network can be expressed as:

$$I_{FB,ON} = \frac{V_{OUT}}{R_{FB1} + R_{FB2}} = \frac{1.8V}{3\text{M}\Omega} = 600nA \tag{3.42}$$

$$I_{FB,AVG} = DI_{FB,ON} = \frac{3.125}{100}600nA = 18.75nA \tag{3.43}$$

Chapter 4

Simulation Results

This chapter presents the simulation results and evaluates the overall performance of the proposed LDO. The analysis focuses on the main performance metrics and design objectives introduced in the previous chapters. Particular attention is given to the stability of the regulation loop over the entire load-current range, with emphasis on the ultra-low quiescent-current consumption under no-load and light-load conditions. Other key performance metrics are also investigated, including power efficiency, load-transient response, line-transient response, and power-supply rejection ratio (PSRR). The obtained results are finally compared with the target specifications to assess the overall performance of the proposed architecture.

4.1 Regulation Loop Performance

One of the most important aspects to evaluate is the stability of the regulation loop, together with its main frequency-domain parameters, including the phase margin, gain margin, bandwidth, and DC gain. As the load current varies, the operating point of the LDO changes, leading to variations in the small-signal parameters of the circuit and, consequently, in the frequency response of the regulation loop. Therefore, the stability of the LDO must be verified over the entire load current range to ensure reliable operation under all specified operating conditions.
Fig. 4.1 shows the loop response under the two extreme load current conditions. In both operating conditions, the phase margin remains above 45°, indicating that adequate stability margins are maintained and stable operation of the regulation loop is ensured. The stability analysis confirms that the compensation network operates effectively over the considered load-current range.
Fig. 4.2 shows additional plots corresponding to different load-current conditions. The stability analysis confirms that the compensation network operates effectively over the considered load current range.

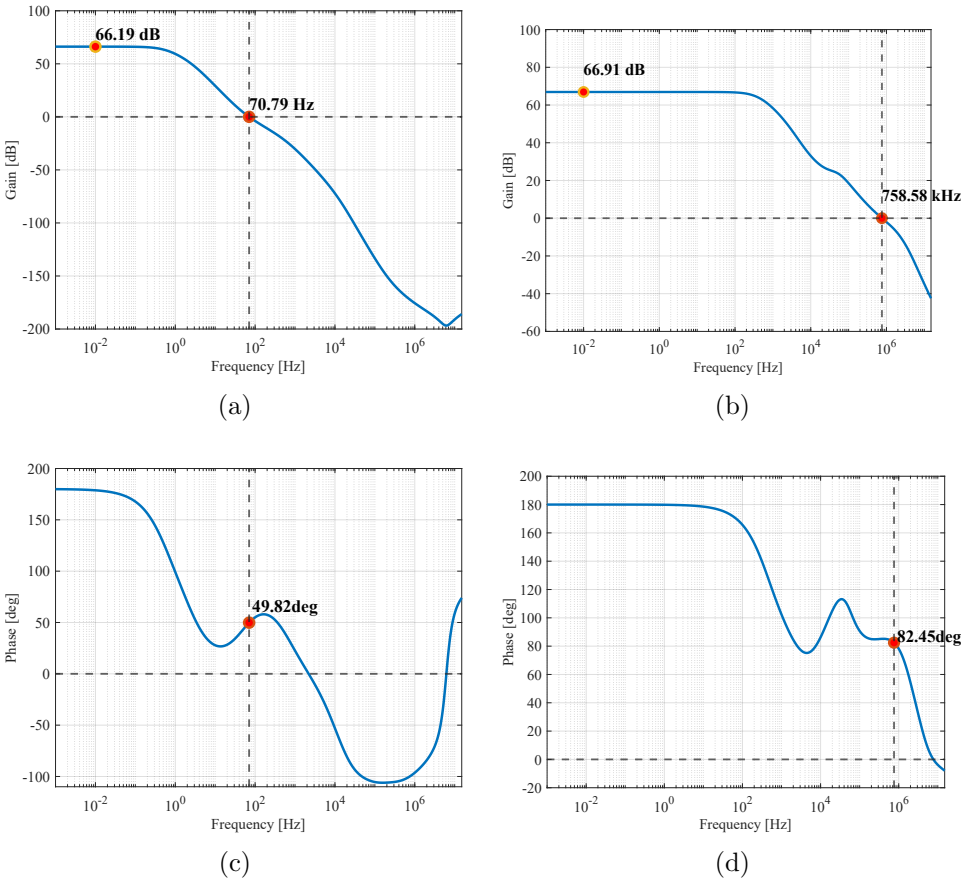


Figure 4.1: Simulations done with $V_{\mathrm{IN}} = 3.6$ V and $V_{\mathrm{OUT}} = 1.8$ V. (a) Loop Gain under no load condition, (b) Loop Gain under heavy load condition ($I_{\mathrm{LOAD}} = 100$ mA), (c) Loop Phase under no load condition, (d) Loop Phase under heavy load condition ($I_{\mathrm{LOAD}} = 100$ mA)

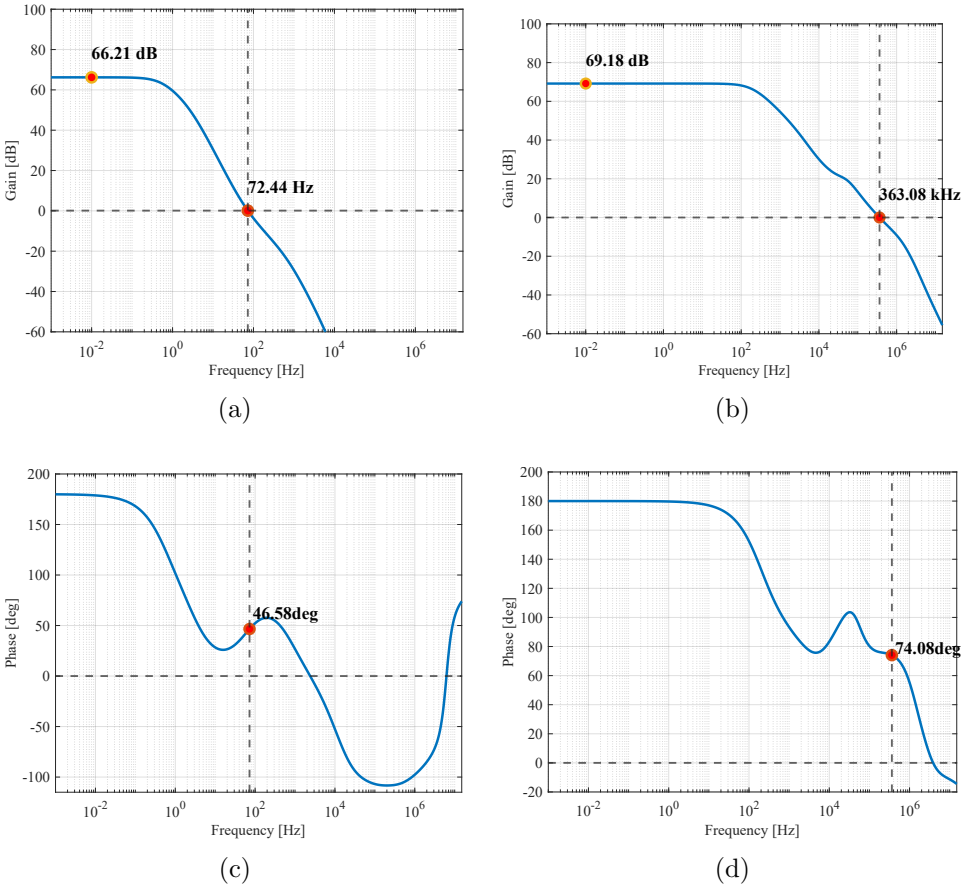


Figure 4.2: Simulations done with $V_{\mathrm{IN}} = 3.6$ V and $V_{\mathrm{OUT}} = 1.8$ V. (a) Loop Gain under light load condition ($I_{\mathrm{LOAD}} = 100$ nA) , (b) Loop Gain under heavy load condition ($I_{\mathrm{LOAD}} = 50$ mA), (c) Loop Phase under light load condition ($I_{\mathrm{LOAD}} = 100$ nA), (d) Loop Phase under heavy load condition ($I_{\mathrm{LOAD}} = 50$ mA)

I_{LOAD}	BW	Phase Margin	Gain Margin
0 A	70 Hz	50°	42.5 dB
100 nA	72 Hz	46°	43 dB
10 mA	74 kHz	57°	24 dB
50 mA	363 kHz	74°	29.5 dB
100 mA	759 kHz	82°	29 dB

Table 4.1: Stability parameters as a function of load current.

Table 4.1 summarizes the main regulation-loop performance parameters for different load-current conditions.
Fig. 4.3 shows the stability response of the system under the worst-case operating condition, with $V_{\mathrm{IN}} = 1.9$ V and a regulated output voltage of $V_{\mathrm{OUT}} = 1.8$ V. The plots demonstrate that the regulation loop remains stable even under this worst-case condition, with the phase margin remaining above 40° across the considered load-current range. In particular, stable operation is maintained, up to the maximum achievable load current $I_{\mathrm{LOAD}} = 10$ mA, under these conditions.

4.2 Sampled Feedback

As discussed in Chapter 3, a sampled feedback technique is employed to reduce the current consumption of the resistive feedback network without requiring excessively large feedback resistance values. The control signal is generated from a fixed 32 kHz clock and subsequently processed to reduce its duty cycle. By reducing the ON-time of the feedback network, the average current flowing through the resistive divider is significantly reduced.
As shown in Fig. 4.4, the periodic feedback control signal turns on the feedback network switches, allowing the output voltage to be periodically refreshed through a duty-cycled operation.

4.3 Load Transient Response

The load-transient performance of the proposed LDO is investigated through transient simulations over the specified load current range. Particular attention is given to the output voltage deviation produced by abrupt load current variations and to the subsequent recovery of the regulated output voltage. Both load increasing and load decreasing conditions are considered in order to evaluate the dynamic response of the regulation loop under different operating conditions. The main parameters extracted from the simulations are the output-voltage undershoot and overshoot, as well as the corresponding recovery time.

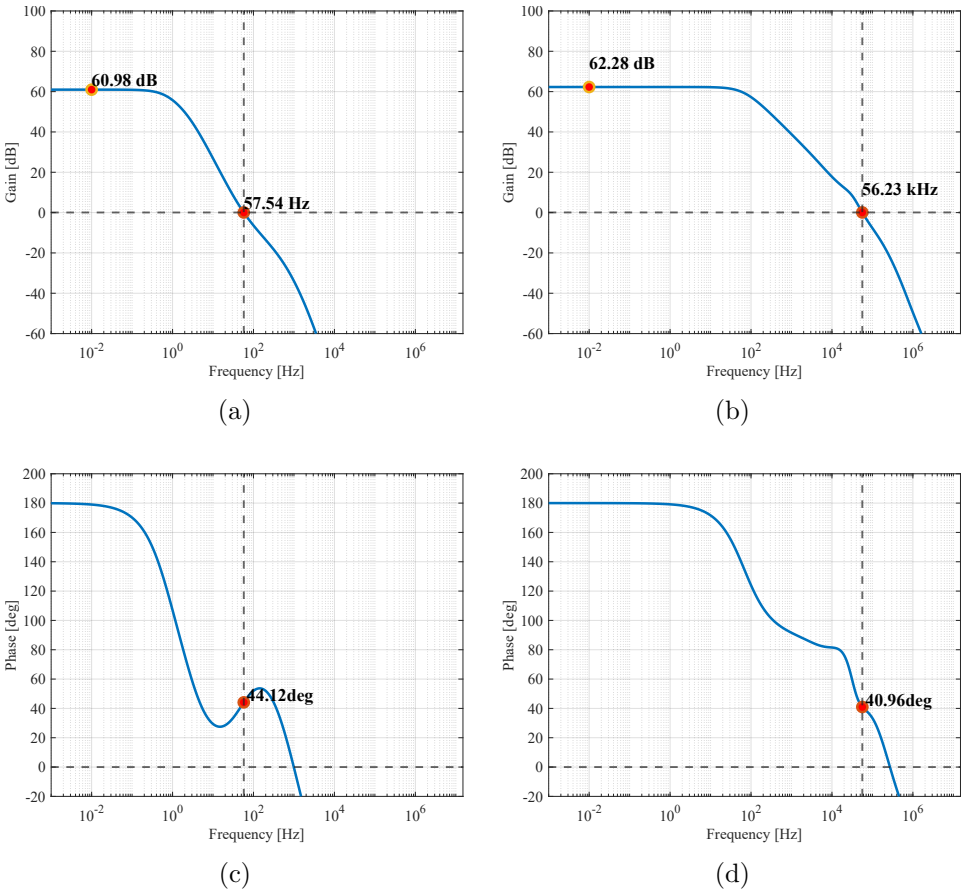


Figure 4.3: Simulations done in the worst case with $V_{\mathrm{IN}} = 1.9$ V and $V_{\mathrm{OUT}} = 1.8$ V. (a) Loop Gain under no load condition, (b) Loop Gain under heavy load condition ($I_{\mathrm{LOAD}} = 10$ mA), (c) Loop Phase under no load condition, (d) Loop Phase under heavy load condition ($I_{\mathrm{LOAD}} = 10$ mA)

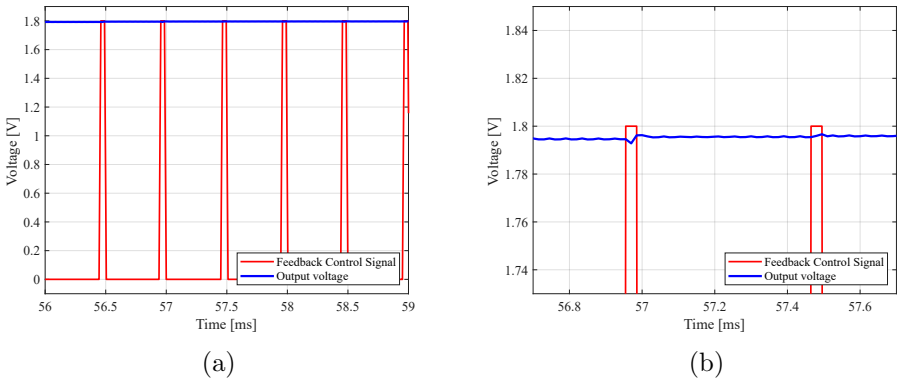


Figure 4.4: Simulated output voltage and sampled feedback control signal for the duty-cycled feedback network.

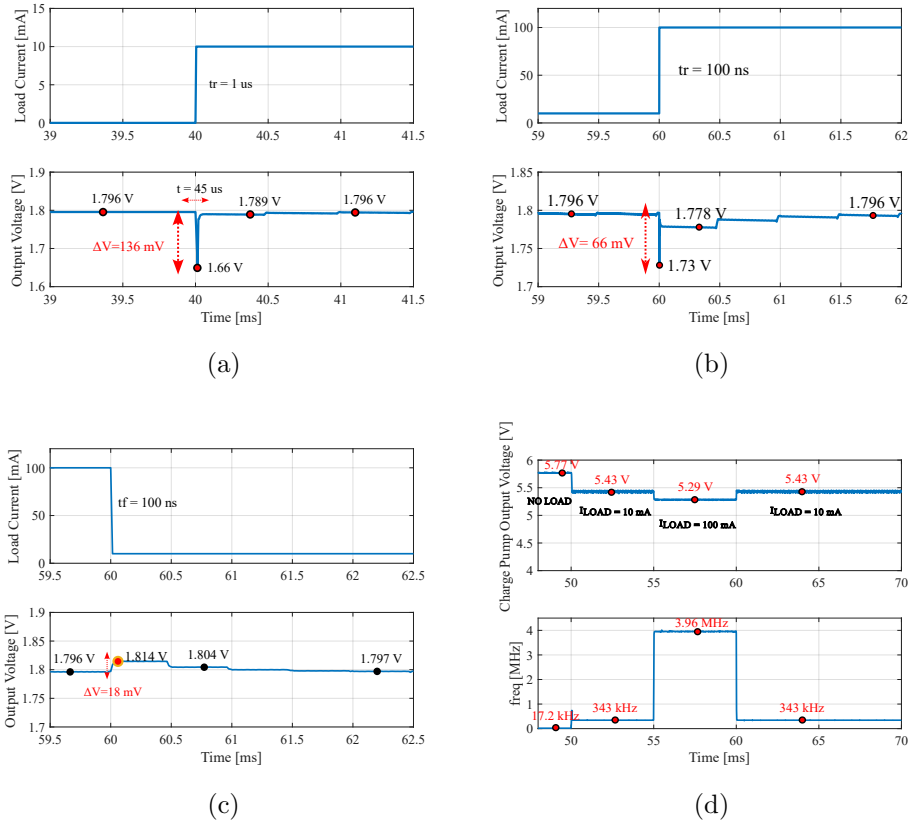
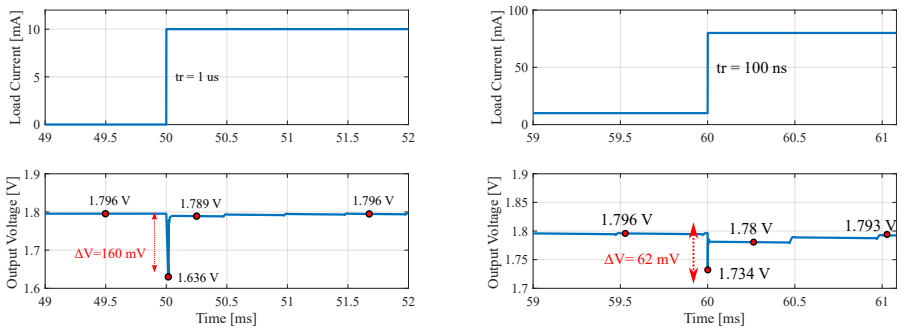


Figure 4.5: Simulations done in the typical case with $V_{\mathrm{IN}} = 3.6$ V and $V_{\mathrm{OUT}} = 1.8$ V. (a) Transient response with a current step from no load condition to 10 mA with $t_{\mathrm{rise}} = 1$ us , (b) Transient response with a current step of 90 mA from 10 mA to 100 mA with $t_{\mathrm{rise}} = 100$ ns , (c) Transient response with a current step of 90 mA from 100 mA to 10 mA with $t_{\mathrm{fall}} = 100$ ns (d) Voltage response of Charge Pump output voltage and switching frequency depending on load current condition

Fig. 4.5 shows the transient response of the system under a typical operating condition with $V_{\text{IN}} = 3.6$ V. An undershoot of $\Delta V = 136$ mV is observed for a 10 mA load current step, from no load condition to 10 mA. An undershoot of $\Delta V = 66$ mV is observed for a 90 mA load-current step, from 10 mA to 100 mA. Conversely, a 90 mA load current step from 100 mA to 10 mA produces an overshoot of $\Delta V = 18$ mV. These results demonstrate that the system maintains a stable output voltage even in the presence of steep and large load current transients.
As shown in Fig. 4.5d the VCO's oscillation frequency varies with the load current and, consequently, so does the switching frequency of the charge pump. In addition, the charge-pump output voltage adjusts according to the current it is required to deliver, operating within a range that ensures both system stability and proper operation.



(a) (b)

Figure 4.6: Simulations done with $V_{\text{IN}} = 2.4$ V and $V_{\text{OUT}} = 1.8$ V. (a) Transient response with a current step from no load condition to 10 mA with $t_{\text{rise}} = 1$ us , (b) Transient response with a current step of 70 mA from 10 mA to 80 mA with $t_{\text{rise}} = 100$ ns

Fig. 4.6 shows the transient response of the system under a low input voltage condition, representative of a partially discharged battery, where V_{IN} is reduced to 2.4 V. An undershoot of $\Delta V = 160$ mV is observed for a 10 mA load-current step, from no-load condition to 10 mA, with a recovery time of 50 us. For a larger load current step of 70 mA, from 10 mA to 80 mA, the output voltage exhibits an undershoot of $\Delta V = 62$ mV. These results demonstrate that the system remains operational and maintains regulation even under low input voltage conditions.
Fig. 4.7 shows the transient response of the system under the minimum input voltage condition, representative of an almost completely discharged battery, with V_{IN} reduced to 1.9 V. The simulations demonstrate that the output regulation is maintained even under this extreme operating condition and at the maximum specified load current of 10 mA.

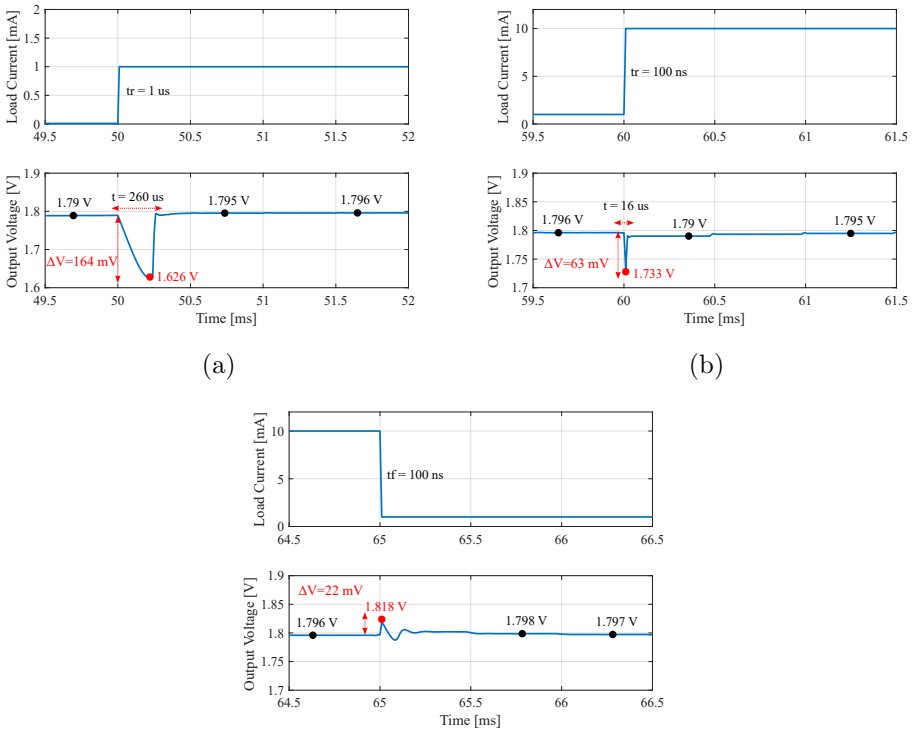


Figure 4.7: Simulations done with $V_{\text{IN}} = 1.9$ V and $V_{\text{OUT}} = 1.8$ V. (a) Transient response with a current step from no load condition to 1 mA with $t_{\text{rise}} = 1$ us , (b) Transient response with a current step of 9 mA from 1 mA to 10 mA with $t_{\text{rise}} = 100$ ns, (c) Transient response with a current step of 9 mA from 10 mA to 1 mA with $t_{\text{fall}} = 100$ ns

4.4 Line Transient Response

The line transient response is evaluated to assess the capability of the proposed LDO to maintain the regulated output voltage in the presence of variations in the input voltage. This analysis is particularly relevant for battery-powered applications, where V_{IN} progressively decreases during battery discharge. The following simulations evaluate the output voltage response under different input-voltage conditions, with particular attention to the resulting voltage deviation and recovery of the regulated output.

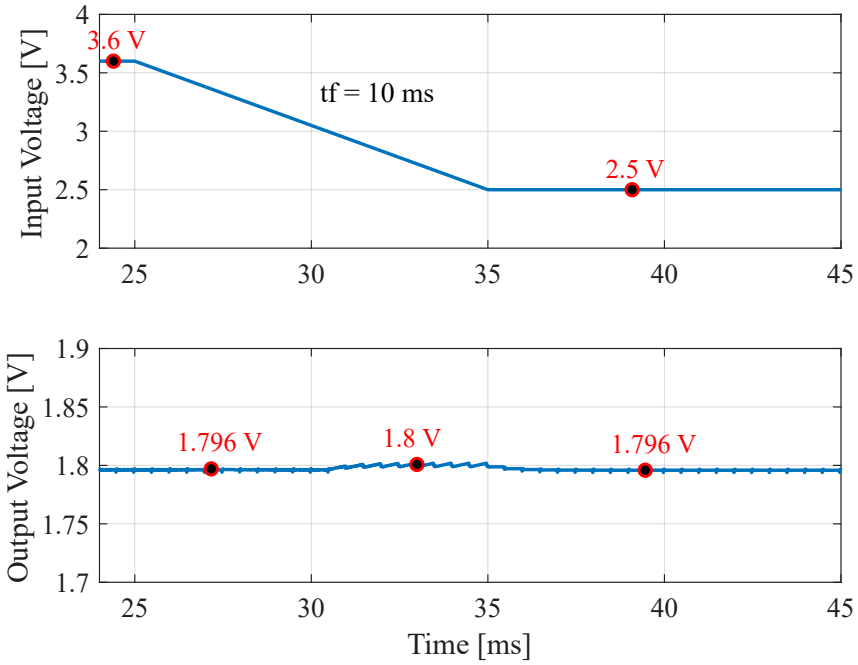


Figure 4.8: Line transient response with change in V_{IN} from 3.6 V to 2.5 V in 10 ms with constant load current I_{LOAD} = 100 mA.

Fig. 4.8 shows the line transient response to an input-voltage variation from 3.6 V to 2.5 V over 10 ms, with a constant load current I_{LOAD} = 100 mA. The results show that the output voltage remains regulated throughout the input voltage variation, demonstrating the capability of the proposed circuit to maintain regulation as the battery voltage decreases during discharge.
Fig. 4.9 shows that the charge-pump output voltage varies in response to changes in the input voltage, decreasing starting from V_{IN} = 3 V to V_{IN} = 2.5 V.
Fig. 4.10 shows the line transient response to an input voltage variation from 3.6 V to 2.8 V within 1 us, while maintaining a constant load current of 100 mA. The results show an output voltage overshoot of ΔV = 11 mV. This

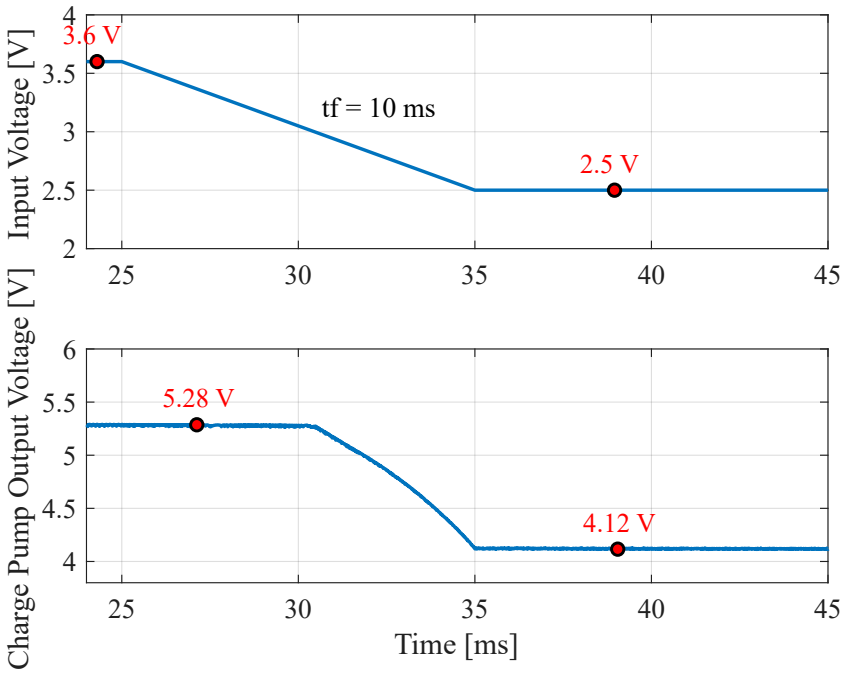


Figure 4.9: Charge Pump output voltage variation with input voltage variation $V_{IN}$from 3.6 V to 2.5 V in 10 ms with constant load current I_{LOAD} = 100 mA.

response demonstrates that the proposed circuit is capable of maintaining good output voltage regulation even in the presence of very fast input voltage variations, such as those that may occur during rapid battery discharge or supply fluctuations.
Fig. 4.11 shows results for an input voltage V_{IN} that is progressively reduced below the desired regulated output voltage. As the input voltage approaches and eventually falls below the target output voltage, the LDO enters in the dropout region and pass MOS can no longer maintain regulation and enters the triode (linear) region. Under these conditions, the output voltage follows the input voltage, resulting in the loss of regulation.

4.5 Current Efficiency

Current efficiency is one of the most important performance metrics of a voltage regulator, particularly in nano-power LDOs, where the quiescent current must be minimized to reduce the overall power consumption. This aspect becomes especially critical under light-load conditions, where the quiescent current can represent a significant fraction of the total current

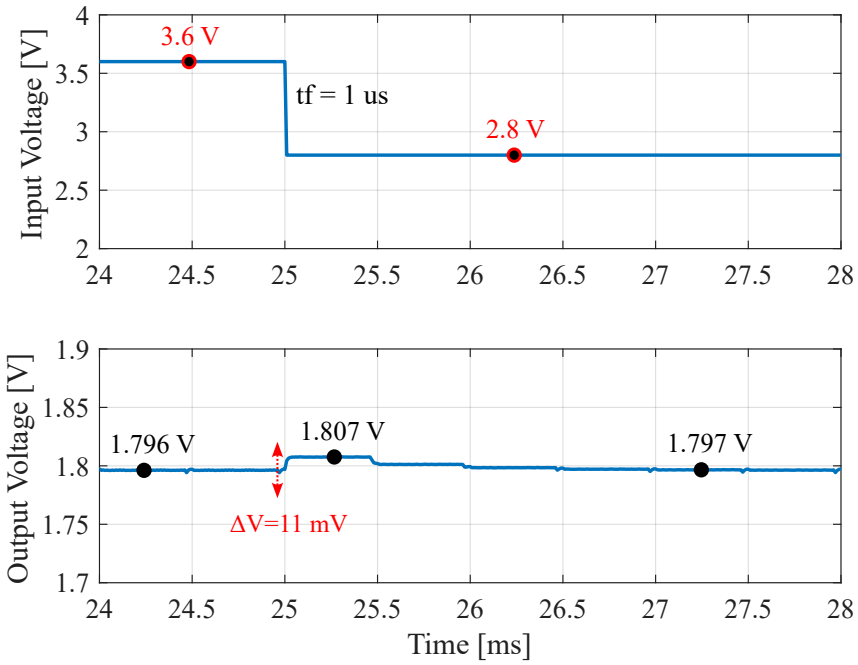


Figure 4.10: Line transient response with change in V_{IN} from 3.6 V to 2.8 V in 1 us with constant load current I_{LOAD} = 100 mA.

drawn from the input supply.

$$\eta_I = \frac{I_{Load}}{I_{Load} + I_q} 100\% \tag{4.1}$$

Fig. 4.12 shows the quiescent current as a function of the load current, together with the corresponding current efficiency at different load conditions.

4.6 PSRR

The Power Supply Rejection Ratio (PSRR) is a key performance metric of an LDO and represents its ability to suppress variations and noise from the input supply at the output. Since the PSRR is strongly frequency-dependent, its behavior is evaluated over a wide frequency range and under different load conditions.
Fig. 4.13 illustrates the PSRR performance across the entire load current range at different disturbance frequencies.
Table 4.2 summerize the PSRR performance of the proposed LDO at different disturbance frequencies over the entire load current range.

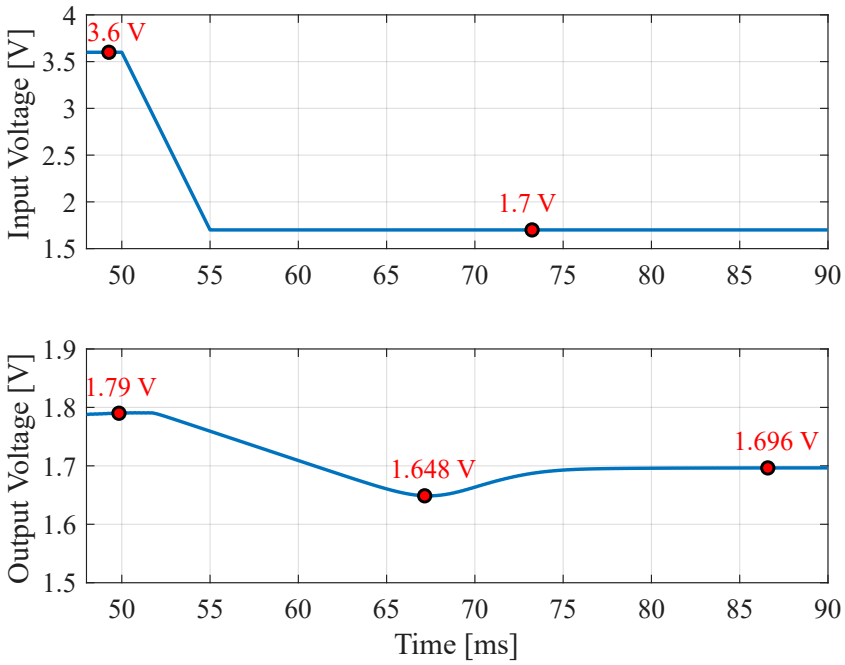
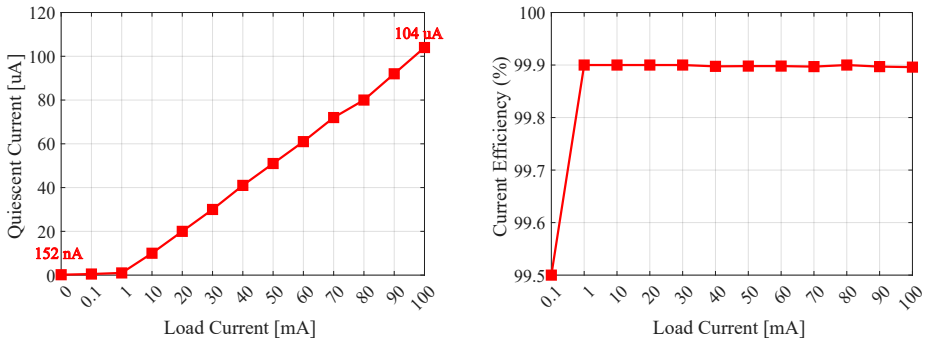


Figure 4.11: Line transient response with change in V_{IN} from 3.6 V to 1.7 V in 5 ms under no load coniditon

In the simulations, the supply disturbance is applied to the input voltage V_{IN}, which represents the battery voltage. The disturbance appearing on the analog supply voltage V_{DDA} is attenuated by the preceding LDO block, which generates V_{DDA} and follows the variations of V_{IN}. Therefore, the disturbance coupled through V_{DDA} is already filtered and attenuated by the preceding LDO, resulting in a lower contribution to the overall PSRR compared with the disturbance directly applied to V_{IN}. Consequently, the PSRR performance of the proposed LDO is mainly determined by the rejection of disturbances coupled through the input supply voltage V_{IN}.

4.7 Corner Simulations

Corner simulations were performed to provide an additional verification of the robustness of the proposed LDO against process and temperature variations. The analysis is intended as a supplementary assessment of the circuit behavior under non-nominal conditions, complementing the main simulation results presented in the previous sections. In these simulations, process variations affecting the MOS transistors, resistors, and capacitors are considered, as summarized in Table 4.3.



(a) (b)

Figure 4.12: Simulations done in typical conditions with $V_{\mathrm{IN}} = 3.6$ V and $V_{\mathrm{OUT}} = 1.8$ V. (a) Quiescent current vs Load current (b) Current Efficiency vs Load current

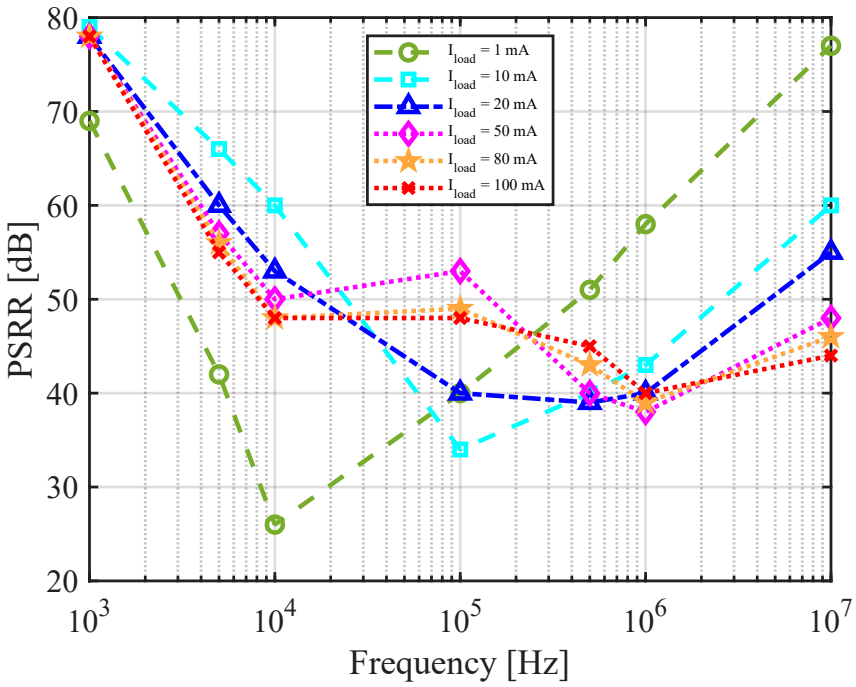


Figure 4.13: Simulated PSRR at different frequencies and load current conditions of the proposed LDO

Fig. 4.14 shows the transient response under corner simulations at the worst-case temperature of 120°C and -40°C, considering a 10 mA load current step, from a no load condition to I_{LOAD}= 10 mA, with a rise time of 1 us. Under the worst-case conditions, an output voltage undershoot of 184 mV is ob-

f_{supply}	I_{LOAD}	PSRR
1 kHz	1 mA	69 dB
	10 mA	79 dB
	20 mA	78 dB
	50 mA	78 dB
	80 mA	78 dB
	100 mA	78 dB
5 kHz	1 mA	42 dB
	10 mA	66 dB
	20 mA	60 dB
	50 mA	57 dB
	80 mA	56 dB
	100 mA	55 dB
1 MHz	1 mA	58 dB
	10 mA	43 dB
	20 mA	40 dB
	50 mA	38 dB
	80 mA	39 dB
	100 mA	40 dB
10 MHz	1 mA	77 dB
	10 mA	60 dB
	20 mA	55 dB
	50 mA	48 dB
	80 mA	46 dB
	100 mA	44 dB

Table 4.2: PSRR at Different Supply Disturbance Frequencies and Load Current

MOM Capacitors	Resistances	MOS
SS	SS	SS
-	-	SF
-	-	FS
FF	FF	FF

Table 4.3: Considered process variations in corners simulations.

served, compared with 136 mV under typical operating conditions. Fig. 4.15 shows the output voltage regulation at I_{LOAD}= 10 mA under typical operating conditions and at the worst-case corner, corresponding to a temperature of 120°C. The simulations show that the system maintains satisfactory regulation even under these extreme conditions, with an output voltage variation of only 14.78 mV, corresponding to an output accuracy within the specified

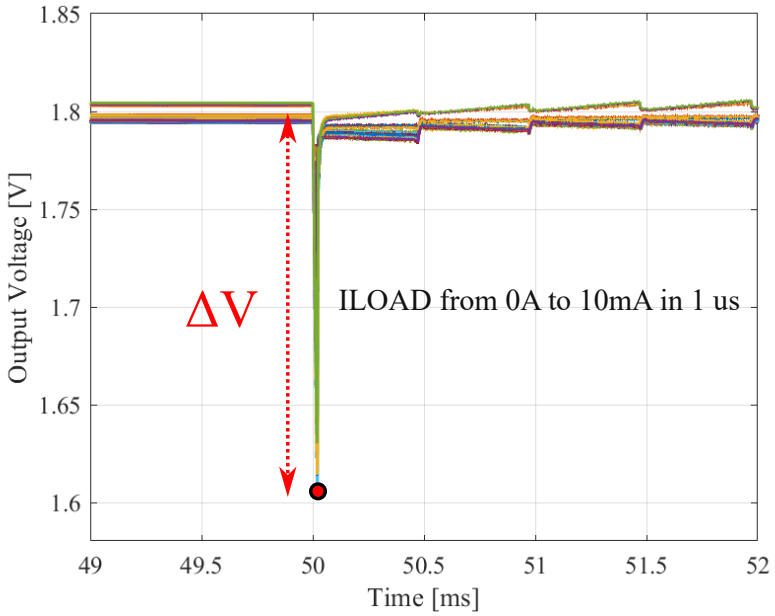


Figure 4.14: Corner simulations at 120°C and -40°C of Load transient response with current step from 0 A to 10 mA

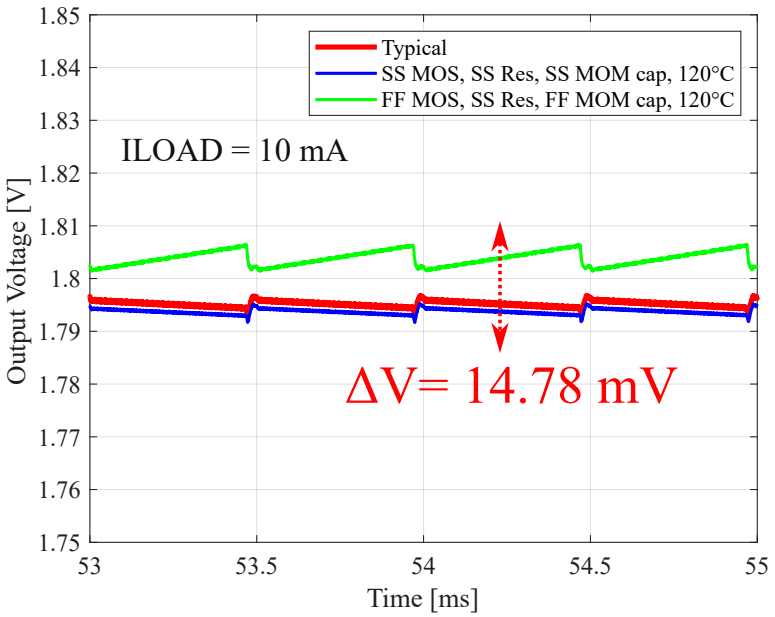


Figure 4.15: Worst case of V_{OUT} regulation with I_{LOAD}= 10 mA

target.

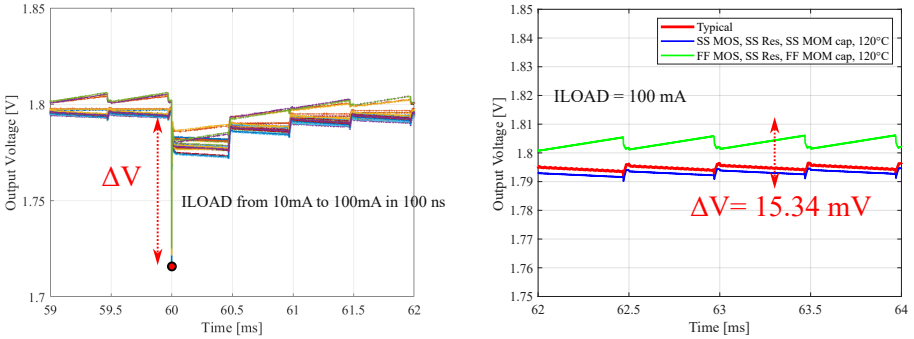


Figure 4.16: Corners simulations at 120°C and -40°C (a) Load transient response with current step from 10 mA to 100 mA in 100ns (b) Output voltage regulation in the worst-case condition with I_{LOAD}= 100 mA

Fig. 4.16a shows the transient response obtained from the corner simulations at 120°C and -40°C, considering a load current step of 90 mA, from 10 mA to 100 mA, with a rise time of 100 ns. Under these conditions, the worst-case output voltage undershoot is 83 mV, compared with 66 mV under typical operating conditions. Fig. 4.16b shows the regulated output voltage under both typical and worst-case conditions. The output voltage remains within a range of 15.34 mV, demonstrating that the output regulation remains within the specified accuracy.

Conclusions

This thesis presented the design and simulation of a nanopower NMOS-based low-dropout regulator (LDO) intended for wearable and low-power applications. The main objective was to investigate an architecture capable of combining low quiescent current with accurate voltage regulation, stability, and adequate dynamic performance over a wide range of load conditions. The proposed LDO employs an NMOS pass transistor, whose gate is driven by a charge-pump-based voltage booster. This solution allows the gate voltage to be increased above the supply voltage, overcoming the intrinsic limitation of an NMOS pass device when a regulated output voltage close to the input supply is required. Particular attention was devoted to minimizing the power consumption of the auxiliary circuits. The error amplifier and buffer were designed with low-power biasing techniques, while adaptive biasing was employed to provide increased driving capability under higher load conditions. In addition, a duty-cycled feedback network was implemented to reduce the current associated with the feedback resistors. Simulation results demonstrate that the proposed architecture is capable of regulating the output voltage at the target value over the considered load-current range. The regulator also maintains its regulation capability under low-input-voltage conditions, approaching the dropout region. The stability analysis shows adequate phase margin over the investigated operating conditions, confirming the robustness of the feedback loop. The transient simulations demonstrate the capability of the LDO to respond to load and input voltage variations while maintaining the output voltage within the required regulation range. The PSRR analysis also shows the effectiveness of the proposed architecture in attenuating supply disturbances over the investigated frequency range. Finally, the quiescent-current and efficiency analyses highlight the trade-off between ultra-low-power operation and the performance required to drive the load. The main results obtained in this work are summerized and compared with the state of the art in Table 4.4.
Future work could focus on the post-layout characterization and experimental validation of the proposed circuit. Further improvements could include the optimization of the charge-pump efficiency, additional reduction of the quiescent current, and optimization of the transient and PSRR performance. Process, voltage, and temperature variations could also be investigated more

extensively to assess the robustness of the design under practical operating conditions.

Parameter	This Work	[3] 2025	[4] 2025	[5] 2025
Process	55 nm	180 nm	350 nm	28 nm
Pass MOS	NMOS	PMOS	PMOS	PMOS
W (N-channel Pass MOS)	10 mm	-	-	-
Input voltage V_{IN}	1.7-5.5 V	1.4-1.8 V	2-5 V	1.2-2 V
Output Voltage V_{OUT}	1.7-1.8 V	1.2 V	1.6-4.5 V	1 V
Maximum Load current $I_{\mathrm{LOAD,Max}}$	100 mA	50 mA	50 mA	400 mA
Output capacitor C_{OUT}	1 uF	1 uF	1uF	4.7 uF
Quiescent current I_{q}	152 nA	96 nA	157 nA	150 nA
Output Voltage accuracy	0.4%	-	-	-
PSRR 1 kHz @10mA	79 dB	45 dB	55 dB @20 mA	-
PSRR 5 kHz @10mA	66 dB	42 dB	40 dB @20mA	-
PSRR 1 MHz @10mA	43 dB	40 dB	36 dB @20mA	-
PSRR 1 kHz @100mA	78 dB	-	-	65 dB
PSRR 1 MHz @100mA	44 dB	-	-	37 dB

Table 4.4: Performance summary and comparison between the proposed LDO and state of the art designs

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