UNIVERSITÀ
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Department of Electrical, Computer and
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Master's degree in Electronic Engineering

High Side current sense solutions for 100V Monolithic GaN Half-bridge

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Abstract

This thesis presents a detailed analysis and comparison of three current sensing circuits for the high-side transistor of a monolithic GaN half-bridge, aimed at tracking inductor ripples and detecting the zero-current condition. The research begins with a theoretical background on DC-DC converters and GaN technology, proceeds with the characterization of components available in this technology and basic building blocks, it concludes with an analysis and performance comparison of three different current sensing topologies. These circuits are compared based on various parameters, including temperature stability, stability against line and load variations, time and frequency response, in order to find the best compromise in terms of performance, area, and power consumption.

Introduction

Nowadays, DC-DC converters are everywhere, spanning from the automotive industry to medical devices, automation, consumer electronics, renewable energy, telecommunications, and many more. The key aspects to consider in designing such converters are space utilization, losses, cost, and lifetime. Designing a circuit that excels in all these areas is challenging, resulting in different converters being optimized to perform better in one or more of these parameters of interest. Considering that the application of the thesis, conducted in collaboration with STMicroelectronics, is a DC-DC converter from 48 V to 12 V with a load current of 10 A, the following analysis determines which option is best to use. The first division can be made into two categories:

- Linear converters
- Switching converters

The classification is based on the operating principle: the first category uses variable resistive elements (such as transistors) to drop the voltage to the desired level, dissipating excess power as heat, while the second category uses pulses generated by switching transistors at high frequency, converting the energy through inductors and capacitors [1] [2]. Based on this, it is straightforward to understand the pros and cons of these two categories. The fact that excess power in linear converters is dissipated as heat suggests that their efficiency is lower. However, the circuit is simpler compared to the other type, which results in better cost-effectiveness. In contrast, switching regulators are highly efficient but more complex and, therefore, more expensive. Another drawback of these regulators is the noise generated by the switching activity, which requires filtering to mitigate, further complicating the circuit. However, despite the increased complexity, the final circuit is smaller and lighter compared to linear regulators, which require a cooling system, such as a heat sink, to manage the high temperatures produced by the excess power dissipation. Taking this into consideration, the applications are straightforward: linear converters are best suited for low-power and noise-sensitive applications, while switching regulators are ideal for high-

power and high-efficiency requirements. Given the high-power application focus of the thesis the switching regulator is the optimal choice.
This type of DC-DC converters can be subdivided into two additional categories based on the energy storage elements used:

- Inductor-based
- Switched-capacitor-based

The first type stores energy in the magnetic field of an inductor, while the second type stores energy in the electric field of a capacitor. The inductor-based converters are more efficient due to lower energy losses and can achieve a larger range of output voltages and higher output currents. However, they are typically bulkier because they require an external inductor. Switched capacitors, also known as charge pumps, are simpler and lighter and can be fully integrated. However, they tend to have higher losses due to parasitic effects and switching inefficiencies, and they experience greater noise and ripple. Given the high-power application, an inductor-based solution is mandatory despite its larger size.
With the converter type selected, the next step is to choose an appropriate topology to achieve the 48 V to 12 V conversion. The three main topologies are:

- Buck
- Boost
- Buck-boost

Discarding the second option, which involves step-up conversion, the remaining options are those that can perform step-down conversions. To simplify the circuit and because a combination of step-down and step-up conversions is not necessary, the buck converter topology is selected [3]. It consists of a half-bridge (two power transistors), an inductor, a capacitor, a driver, and a control loop, as shown in Fig. 1. The output voltage is taken after the inductor and connected to a load, which in this case is simplified as a resistor.
Returning to switching converters, as previously mentioned, they are complex due to the requirement of a control loop to maintain a stable output voltage. This is where the relevance of this thesis work becomes evident: a current sense circuit is essential for implementing a current-based control loop. The current sense circuit must provide the most accurate measurement possible, despite variations in temperature, line and load conditions. This circuit, connected to the high-side power transistor as shown in Fig. 1, will be used to monitor the inductor ripples during the on-phase and to detect the zero-current condition. This detection is essential for implementing an

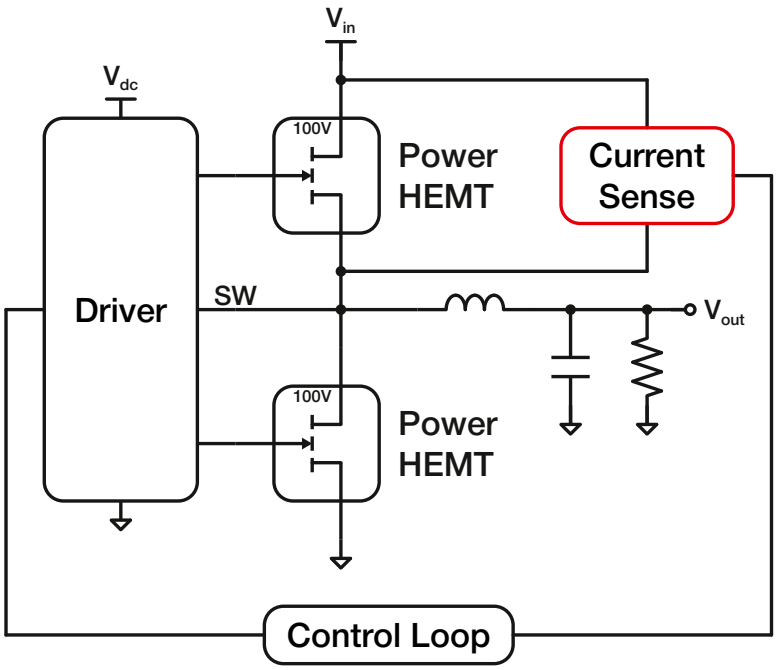

Figure 1: Buck converter with two power GaN transistor and control loop with the current sense block.

anti-cross-conduction circuit between the turn-off of the high-side transistor and the turn-on of the low-side transistor, without introducing a large fixed delay that would impact switching performance.
However, the most challenging and innovative aspect of this project is the choice of the semiconductor material. Instead of the more common silicon (Si), gallium nitride (GaN) is used. The advantages of GaN over silicon will be discussed in detail in Chapter 1. An important consideration is the absence of p-channel devices in GaN technology. As a result, the control loop in commercially available GaN DC-DC converters is implemented in silicon, while the half-bridge uses GaN, resulting in a discrete integrated circuit. Designing this control loop piece is a significant step toward the goal of developing a monolithic GaN DC-DC converter.
The thesis continues with Chapter 2, which provides a characterization of the available components and proceeds with an analysis of all the basic building blocks in Chapter 3, explaining the considerations behind the choices between different topologies. It concludes with Chapter 4, where three different solutions are compared across various aspects to determine the optimal one.

Chapter 1

GaN Technology Overview

1.1 Operating principle

Gallium Nitride (GaN) transistors rely on the high electron mobility that characterizes the material and its heterostructures. At the core of their operation is the High Electron Mobility Transistor (HEMT), which utilizes a two-dimensional electron gas (2DEG). This 2DEG forms at the interface between a GaN layer and an aluminum gallium nitride (AlGaN) layer, as shown in Fig. 1.1, due to the piezoelectric properties of GaN. In practice, as illustrated in Fig. 1.2, the conduction band in the GaN drops below the Fermi level near the surface. The formation of the 2DEG results in a high electron concentration that can move freely with minimal resistance when a voltage is applied across the device, which is crucial for fast switching and efficient power conversion.
GaN transistors come in two primary modes: depletion-mode (d-mode) and enhancement-mode (e-mode). In d-mode transistors, the device is naturally on and requires a negative gate voltage to switch off, making them less convenient for power applications. In contrast, e-mode transistors are off when no gate voltage is applied and turn on with a positive voltage thus they are increasingly favored for power applications due to their simpler

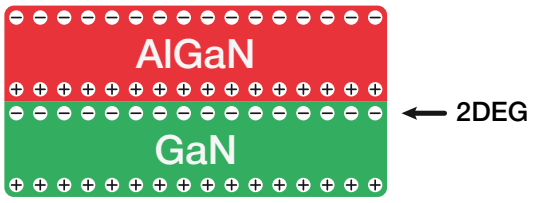

Figure 1.1: Cross-section of a GaN/AlGaN heterostructure showing the formation of a 2DEG.

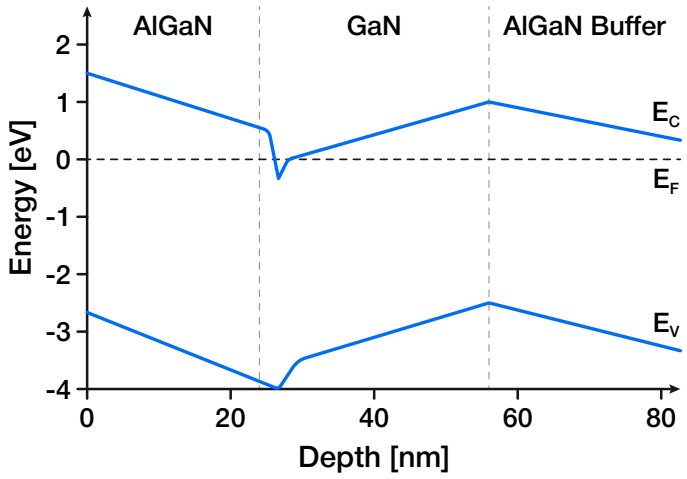

Figure 1.2: Band diagram of a GaN/AlgaN heterostructure showing the formation of a 2DEG.

control mechanism. However, these devices are inherently n-channel because the two-dimensional gas consists of electrons, resulting in the absence of p-channel devices in GaN technology.
The key benefit of the GaN HEMT structure is its ability to handle high electric fields and high temperatures. The high mobility of electrons in the 2DEG allows for low on-resistance and high-frequency operation, which translates into efficient power conversion. Additionally, the heterostructure design minimizes energy losses during switching, making GaN transistors ideal for high-efficiency applications in power electronics.

1.2 Advantages of GaN over silicon

GaN provides several key advantages over traditional silicon-based transistors, with one of the most significant being its wide bandgap. GaN has a bandgap of 3.39 eV, substantially larger than silicon's 1.12 eV, as shown in Tab. 1.1 from [4]. A wider bandgap enables GaN devices to function at much higher temperatures and withstand higher voltages without breaking down, making GaN transistors particularly well-suited for high-power and high-temperature environments commonly found in power conversion applications.
Another significant advantage is GaN's higher critical electric field, which allows the material to handle higher voltages before breaking down. As a result, GaN transistors can be made smaller for a given voltage rating compared to silicon-based devices, resulting in higher power density and more compact systems. GaN's electron mobility is also higher than silicon's,

	Silicon	**GaN**
Band Gap E_g [eV]	1.12	3.39
Critical Field E_{Crit} [MV/cm]	0.23	3.3
Electron Mobility μ_n [cm^2/V·s]	1400	1500
Permittivity ϵ_r	11.8	9
Thermal Conductivity λ [W/cm·K]	1.5	1.3

Table 1.1: Comparison between Silicon and GaN parameter.

enabling faster switching speeds and lower conduction losses. This results in increased efficiency, especially in applications that require high-frequency operation, such as switching power supplies and RF amplifiers.
In terms of thermal performance, GaN devices dissipate less heat because of their higher efficiency and reduced on-resistance. This reduces the need for complex cooling systems, which simplifies device packaging and lowers the overall system cost. Furthermore, GaN's ability to operate at higher frequencies and voltages can lead to smaller passive components, contributing to the overall reduction in system size.
Overall, GaN transistors offer better performance in terms of efficiency, switching speed, size, and thermal management when compared to silicon. These advantages make GaN the material of choice for next-generation power electronics.

1.3 Phisycal structure

The physical structure of GaN transistors is built on a heteroepitaxial growth process, where a thin nucleation layer of AlN is deposited on a substrate. There are several types of substrates used for this purpose, each offering unique advantages and disadvantages. The most common substrates include silicon (Si), silicon carbide (SiC), sapphire (Al_2O_3), and also native GaN.
Silicon is the least expensive and most widely used substrate, primarily due to the established silicon-based fabrication infrastructure. However, the mismatch between the lattice structures of GaN and silicon can lead to defects in the GaN layer, which can impact device performance. Additionally, silicon has lower thermal conductivity compared to other substrates, making it less efficient in high-power applications. Despite these limitations, silicon substrates remain popular in cost-sensitive commercial applications like DC-DC and AC-DC converters.
Silicon carbide (SiC) is another popular substrate due to its closer lattice match to GaN and superior thermal conductivity. SiC-based GaN transistors can handle higher power densities and operate efficiently at higher temperatures. This makes them ideal for applications requiring high performance and reliability, such as radio-frequency (RF) amplifiers and high-

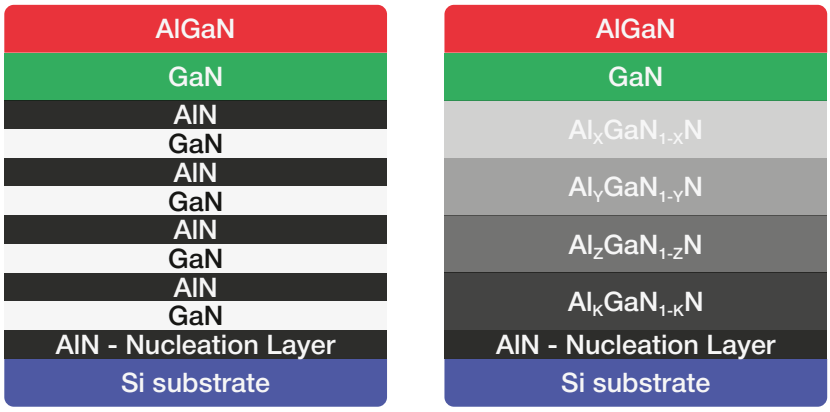

Figure 1.3: Two transition layer realization methods: super-lattice buffer and step-graded buffer.

power switching converters. However, the high cost of SiC wafers limits their use to high-end applications.
Sapphire (Al_2O_3) is sometimes used as a substrate for GaN transistors. While sapphire has good electrical insulation properties, its poor thermal conductivity and significant lattice mismatch with GaN limit its use in high-power applications. Nevertheless, sapphire is useful in optoelectronic applications, such as light-emitting diodes (LEDs), due to its transparency and low cost compared to SiC.
Native GaN substrates offer the best performance due to their perfect lattice match with the GaN layers grown on top, resulting in fewer defects and improved device performance, especially in high-power and high-frequency applications. However, their high cost and limited availability have restricted widespread adoption. Recently, however, there have been announcements about GaN wafers with dimensions comparable to common silicon wafers. This development suggests that with mass production, prices could decrease, leading to further advancements in GaN technology.
Due to the lattice mismatch between GaN and the substrate (especially silicon), a buffer layer is required between the substrate and the GaN/AlGaN layers. The buffer layer, typically made from aluminum nitride (AlN) or aluminum gallium nitride (AlGaN), serves several purposes. First, it reduces the strain caused by the lattice mismatch, minimizing the formation of defects that could degrade device performance. Second, it acts as a transition layer that helps stabilize the epitaxial growth of GaN on substrates with differing crystal structures. The quality and composition of the buffer layer significantly impact the overall device reliability and performance, especially

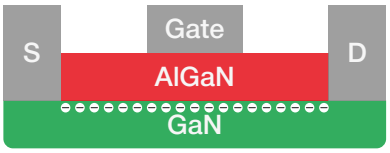

Figure 1.4: Cross-section of a depletion HEMT.

in terms of thermal dissipation and breakdown voltage. Two approaches for realizing the buffer layer are illustrated in Fig. 1.3.
On top of this buffer layer, the GaN HEMT is constructed. As illustrated in Fig. 1.4, the d-mode transistor is formed by piercing the AlGaN layer to create contacts with the 2DEG for the source and drain terminals. For the gate, a metal contact is placed over the AlGaN layer between the source and drain terminals. This gate structure forms a Schottky diode between the metal gate and the AlGaN semiconductor layer beneath it.
The structure of e-mode GaN transistors can be realized in different ways to achieve the desired normally-off behavior. One method is the recessed gate structure, where part of the AlGaN barrier is etched to thin the layer above the 2DEG, as shown in Fig. 1.5(a). By reducing the thickness of the AlGaN, the voltage required to induce electron conduction in the 2DEG increases, effectively shifting the threshold voltage of the device. This allows precise control over the device's threshold voltage, making this design suitable for power applications that require stringent control over switching.
Another approach involves fluorine implantation into the AlGaN barrier, as illustrated in Fig. 1.5(b). Fluorine atoms introduce fixed negative charges that locally deplete the 2DEG under the gate region, ensuring that the device remains off at zero gate voltage. This approach, while less common, offers a controlled way to tune the threshold voltage and improve the transistor's switching characteristics.
A third technique involves the use of a p-type GaN layer grown on top of the AlGaN barrier, as shown in Fig. 1.5(c). This p-GaN layer introduces positive charges that deplete the 2DEG under zero gate bias, ensuring that the transistor is normally off. When a positive voltage is applied to the gate, the 2DEG reforms, allowing current to flow. With this approach, the gate is formed by two back-to-back diodes. The first diode is a Schottky diode between the p-GaN layer and the gate metal contact, while the second is a PIN diode between the p-GaN layer and the AlGaN semiconductor. This configuration provides unique control characteristics for the GaN HEMT, combining the benefits of both diode types in regulating the gate voltage and current flow.
These structural variations allow for customization of the GaN transistor to meet varying performance needs, such as switching speed, on-resistance,

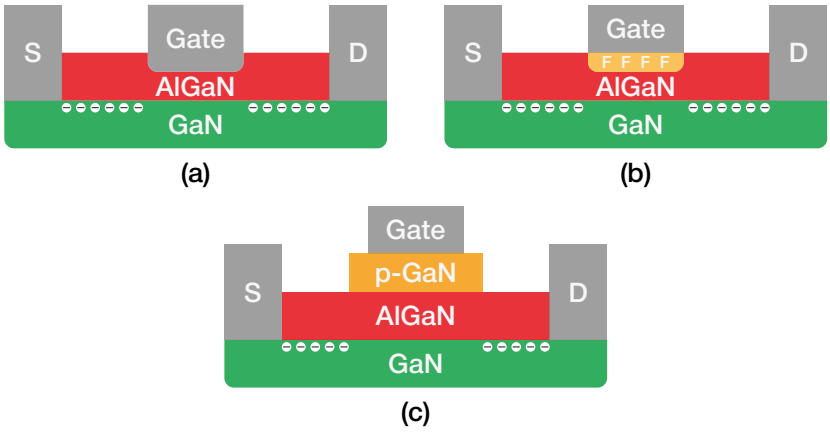

Figure 1.5: Cross-section of three different implementations of monolithic enhancement HEMTs: (a) Recessed gate, (b) Fluorine implantation and (c) p-type gate.

and breakdown voltage. The selection of a particular method depends on the specific application and the desired characteristics of the transistor.

1.4 Conclusion

GaN transistors, with their unique operating principles, offer significant advantages over traditional silicon devices, especially in high-power, high-frequency applications. Their ability to operate at higher temperatures, higher voltages, and faster switching speeds, along with their smaller size and higher efficiency, make GaN technology an attractive choice for the future of power electronics. With continued improvements in fabrication techniques and cost reductions, GaN is positioned to replace silicon in many critical applications, from power converters to RF amplifiers.

Chapter 2

GaN components characterization

In this chapter, all the devices available in ST Microelectronics 100V monolithic pGaN technology will be characterized, and comparisons will be provided to explain the motivations behind the choices of the components used for the design of the current sense circuits.

2.1 Enhancement 12-V HEMT

Let us start from the 12-V enhancement transistor (neh12V), shown in Fig. 2.1. The dimensions under which it was tested are:

- L = 1 µm
- W = 5 µm
- number of fingers = 1

These represent the minimum size, enabling the analysis of the behavior of the smallest device.

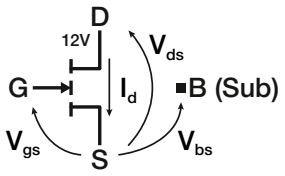

Figure 2.1: Symbol of the 12-V enhancement transistor.

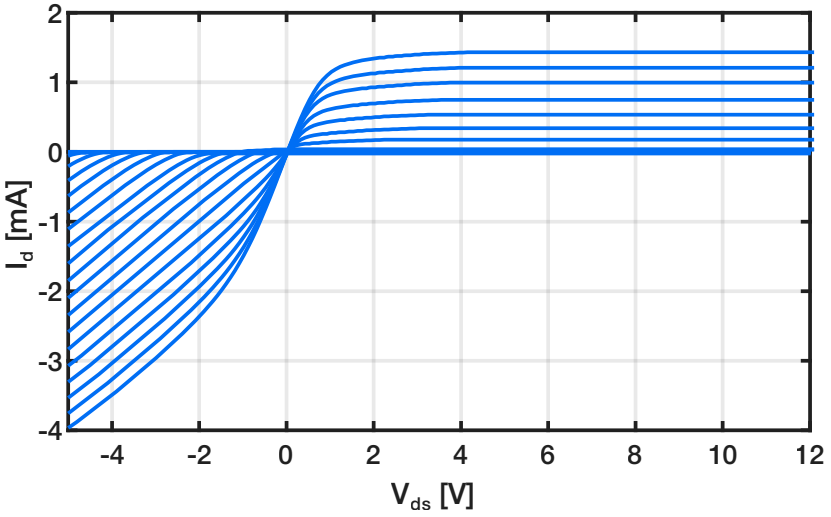

Figure 2.2: I_d-V_{ds} characteristic as a function of V_{gs} [-5 V ÷ 5 V] of a 12-V enhancement HEMT.

2.1.1 I_d-V_{ds} characteristic as a function of V_{gs}

As in every transistor characterization, let us start from the I_d-V_{ds} characteristic, sweeping the V_{gs} variable. The first thing that can be noticed in Fig. 2.2 is that it was also tested in the negative range of V_{ds}. This is because it can be used in inverse current operation due to the gate structure, which is composed of a PIN diode and a Schottky diode back-to-back, rather than a capacitor, as explained in Sec. 1.3. From Fig. 2.2, it can be observed that a significant direct current flows for values of V_{gs} greater than 1 V. This reflects what mentioned in Sec. 1.2 regarding the high electron mobility of this new technology. For $V_{ds} < 0$ V inverse current is present for every value of V_{ds} only if $V_{gs} > 1$ V, while for $V_{gs} < 1$ V the inverse current start to flow at increasingly smaller values of V_{ds}.

2.1.2 I_d-V_{ds} characteristic as a function of V_{bs}

To understand how the substrate voltage influences the drain current, a parametric analysis was performed by sweeping V_{bs}. Considering the right part of the Fig. 2.3, for positive V_{bs} values it exhibits slight variations with respect to $V_{bs} = 0$ V, while for negative values it has a small reduction of the output current. For example at V_{bs} = -5 V it is 15 µA lower, over a 1 mA current. This reflect the behavior seen in MOSFET devices, despite the absence of a body diode that connect directly the substrate to the drain contact. Considering now the negative values of V_{ds} in Fig. 2.3, a change

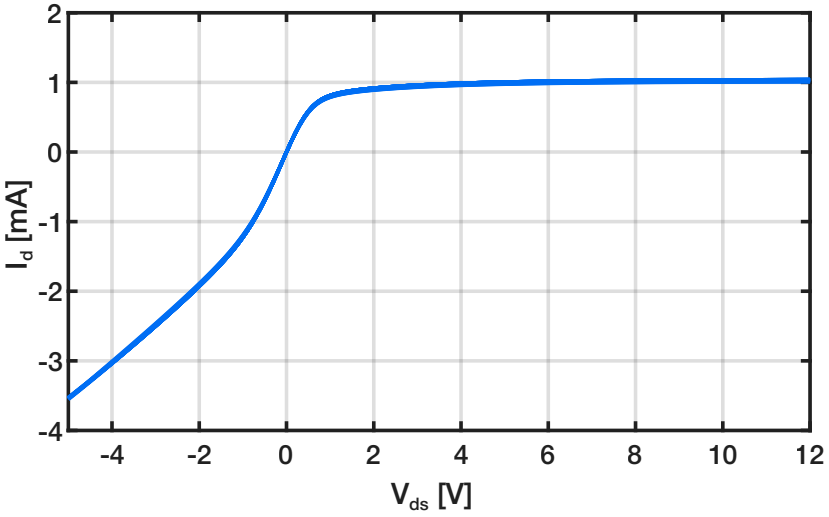

Figure 2.3: I_d-V_{ds} characteristic as a function of V_{bs} [-5 V ÷ 5 V] of a 12-V enhancement HEMT.

in the drain current can be observed compared to nominal condition for all values of V_{bs}. This can be understood by analogy to a MOS transistor: if the drain voltage becomes negative, the substrate voltage must be more negative to prevent the body diode from turning on, thereby increasing the range of conditions under which the effect occurs.

2.1.3 I_d-V_{ds} characteristic as a function of Temperature

Another important variable is the temperature, so the transistor was characterized at five different temperatures: -40°C, 0°C, 27°C, 100°C and 150°C; with 27°C being the nominal condition. From the Fig. 2.4 it can be noticed that the magnitude of the current decreases for increasing temperatures. This effect, unlike from what just seen for substrate variation, is definitively not negligible. At 150°C the current is halved, whereas at -40°C it is 25% greater than the nominal condition. This behavior must be considered during the design of a circuit.

2.1.4 I_d-V_{gs} characteristic as a function of V_{ds}

From an I_d-V_{gs} characteristic as a function of V_{ds} some other behaviors can be better observed. First of all here is clear that the threshold voltage (V_{th}) is 1 V. From Fig. 2.5, it can be appreciated that, beyond the triode region, the current in saturation is not perfectly equal across all voltage values, this is due to the channel modulation effect induced by the drain, known as

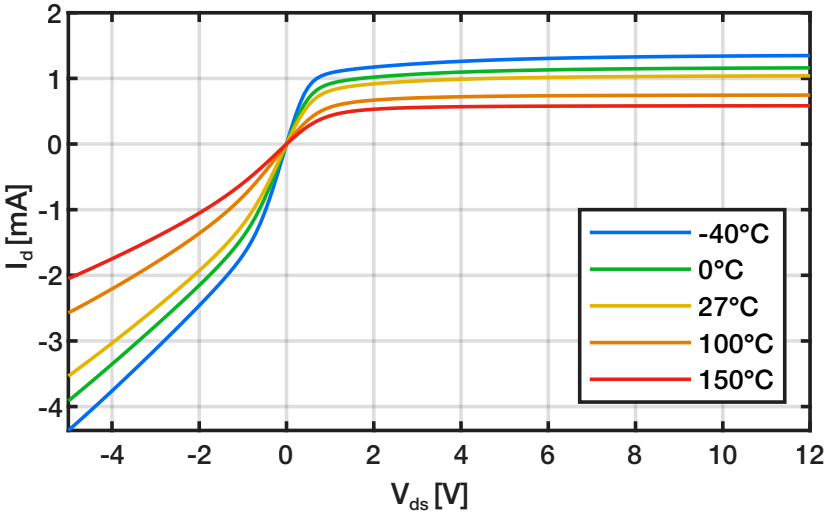

Figure 2.4: I_d-V_{ds} characteristic of a 12-V enhancement HEMT, with temperatures of: -40°C, 0°C, 27°C, 100°C and 150°C.

Drain-Induced Barrier Lowering (DIBL). This effect could also be noticed in the previous analyses by observing where the slope of the drain current in the saturation region was different from zero.

2.1.5 On-resistance

The on-resistance (R_{on}) is a critical parameter when considering its use as a switch. Therefore, the dimensions under which it was tested have been adjusted to better reflect a more typical use case:

- L = 1 µm (minimum)
- W = 100 µm
- number of fingers = 10

With this defined and considering the maximum allowable gate voltage of 6 V, the on-resistance (R_{on}), measured with a V_{ds} of 100 mV, is 28.2 Ω.

2.2 Depletion 12-V HEMT

Let us now analyze the 12-V depletion transistor (ndh12V), shown in Fig. 2.6, which exhibits behaviors quite different from the previous device. To maintain comparability, it was tested using the same dimensions:

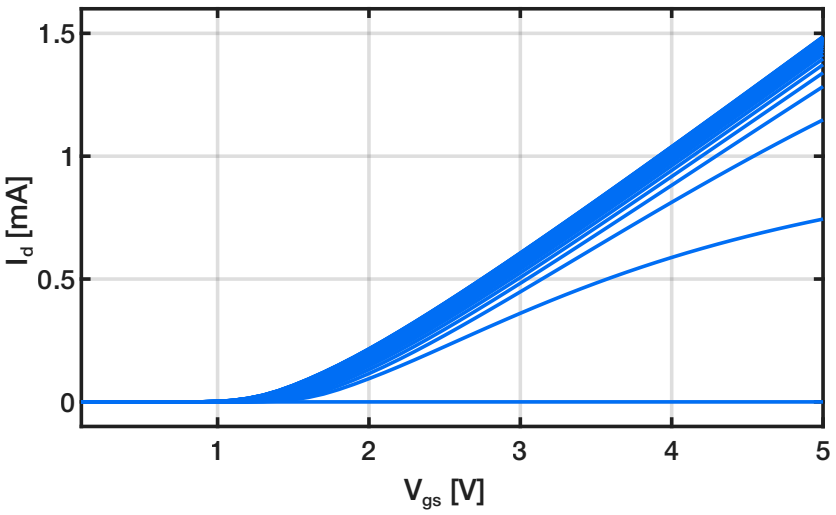

Figure 2.5: I_d-V_{gs} characteristic as a function of V_{ds} [0 V ÷ 5 V] of a 12-V enhancement HEMT.

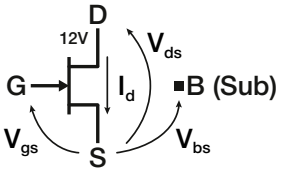

Figure 2.6: Symbol of the 12-V depletion transistor.

- L = 1 µm
- W = 5 µm
- number of fingers = 1

In this case the length is not the minimum one.

2.2.1 I_d-V_{ds} characteristic as a function of V_{gs}

Differences can be immediately noticed with respect to the enhancement type. From Fig. 2.7, it can be roughly estimated that for V_{gs} values between -0.5 V and 0.5 V, the behavior is similar to that of a MOSFET for $V_{ds} >$ 0 V. In the same V_{ds} condition, for gate voltages lower than -0.5 V there is no current, while for $V_{gs} > 0.5$ V current starts to flow only from increasing values of V_{ds}. Examining the left side of Fig. 2.7, it can be seen that if V_{gs}

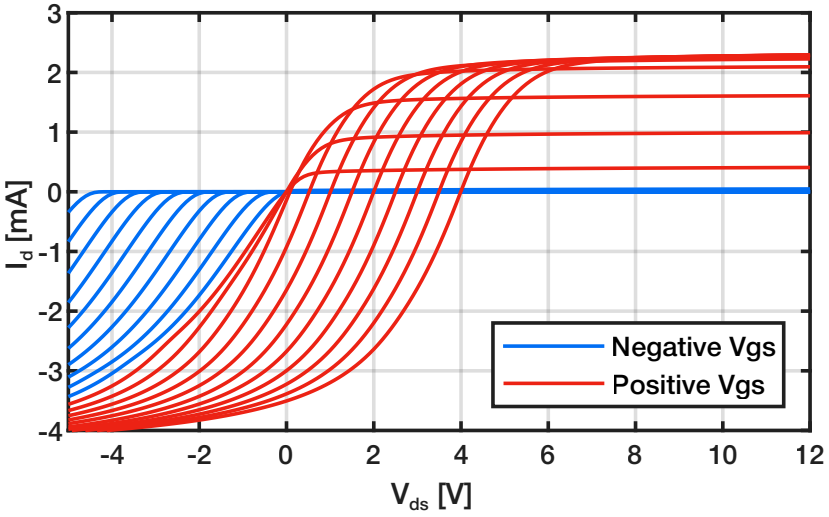

Figure 2.7: I_d-V_{ds} characteristic as a function of V_{gs} [-5 V ÷ 5 V] of a 12-V depletion HEMT.

$>$ -0.5 V, inverse current is present for every value of V_{ds}. Conversely, if V_{gs} is lower, the current starts to flow only from a decreasing value of V_{ds}. Inverse current is possible because the gate is a Schottky diode.
From Fig. 2.8, where there is a higher density of curves around the MOS-like interval, it can be seen that this interval is between -700 mV and 800 mV. Since there is already a drain current at $V_{gs} = 0$ V, this device is well-suited for designing current generators, as will be discussed in the next chapter.

2.2.2 I_g-V_{ds} characteristic as a function of V_{gs}

Studying the I_g-V_{ds} characteristics reveals a significant difference compared to MOS devices: outside the transistor-like interval, current flows into the gate when it is on, and this current can be quite large, in the order of mA. Specifically, for $V_{ds} > 0$ V and $V_{gs} > 700$ mV, a non-zero gate current is observed, whereas for lower values of V_{gs}, the gate current remains zero.

2.2.3 I_d-V_{ds} characteristic as a function of V_{bs}

In this device, the substrate voltage affects both positive and negative values of V_{ds} similarly, as shown in Fig. 2.9. When V_{bs} is greater than 0 V, the drain current has negligible variations, while for negative V_{bs} values, the current magnitude decreases.

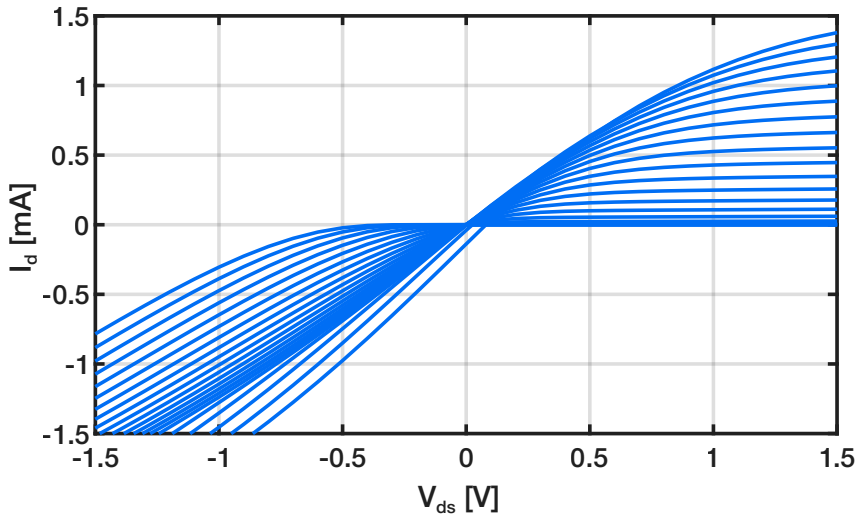

Figure 2.8: I_d-V_{ds} characteristic as a function of V_{gs} [-1 V ÷ 1 V] of a 12-V depletion HEMT, with a detail in the MOS-like region.

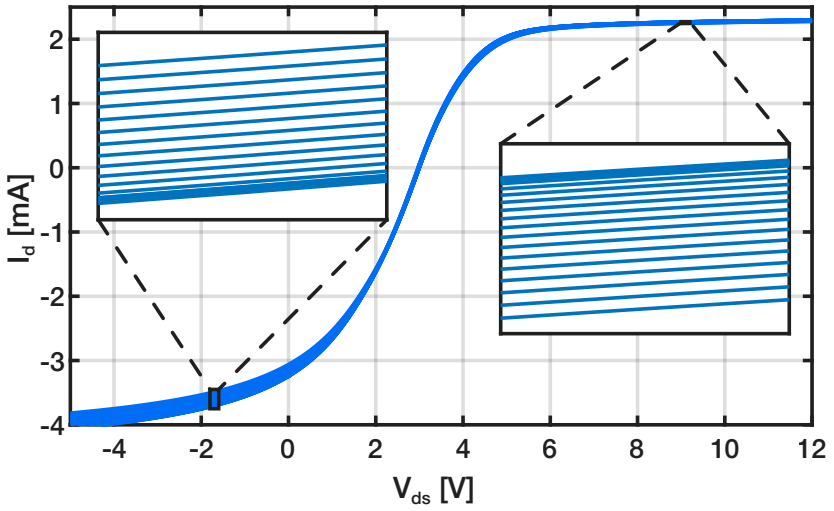

Figure 2.9: I_d-V_{ds} characteristic as a function of V_{bs} [-5 V ÷ 5 V] of a 12-V depletion HEMT.

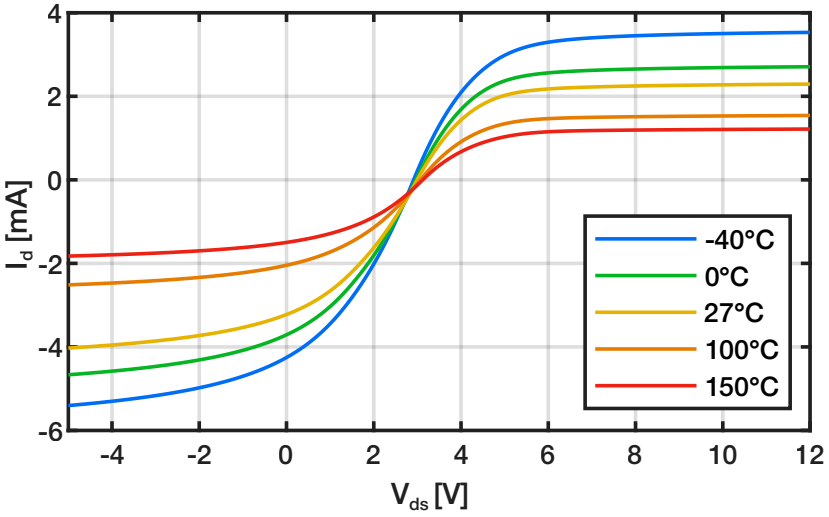

Figure 2.10: I_d-V_{ds} characteristic of a 12-V depletion HEMT, with temperatures of: -40°C, 0°C, 27°C, 100°C and 150°C.

2.2.4 I_d-V_{ds} characteristic as a function of Temperature

Similar to the enhancement device, temperature has a noticeable effect on the drain current, which decreases as the temperature increases. This behavior is depicted in Fig. 2.10, where the drain current is plotted for various temperatures, including -40°C, 0°C, 27°C, 100°C and 150°C. Therefore, when designing with depletion devices, temperature is an important factor to consider.

2.2.5 I_d-V_{gs} characteristic as a function of V_{ds}

Using the characteristic in Fig. 2.11, it can be observed that the threshold voltage is negative, as expected for a depletion-mode device. As with the enhancement device, the channel modulation effect is observable as a thick line. However, the more distinctive behavior occurs for positive values of V_{gs}. The drain current starts to decrease from a certain value of V_{gs}, becoming inverse at a certain point. This value increases as V_{ds} rises.

2.2.6 On-resistance

Like for the enhancement device, considering its different application, it was tested with different dimensions to better match a real-world application:

- L = 500 nm (minimum)

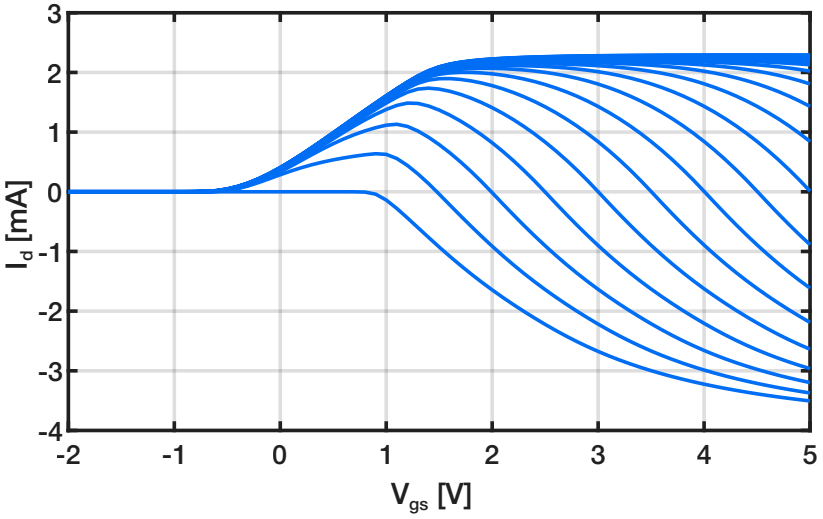

Figure 2.11: I_d-V_{gs} characteristic as a function of V_{ds} [0 V ÷ 5 V] of a 12-V depletion HEMT.

- W = 100 µm
- number of fingers = 10

With this defined and considering the maximum allowable gate voltage of 6 V, the on-resistance (R_{on}), measured with a V_{ds} of 100 mV, is 37.7 Ω. It can be deducted that, despite a shorter channel length, the on-resistance of the depletion device is higher than that of the enhancement device, measured in Sec. 2.1.5.

2.3 Enhancement 100-V HEMT

The only normally off, high voltage transistor available in this platform is the 100-V enhancement HEMT, shown in Fig. 2.12. This will be the key component for interfacing the analog part of the circuit with high voltage domain and for the realization of power components. For this purpose, the device was tested under different dimensions:

- L = 600 nm
- W = 50 µm
- number of fingers = 1

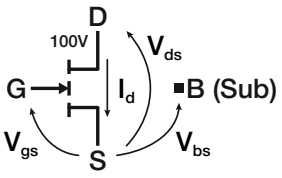

Figure 2.12: Symbol of the 100-V enhancement transistor.

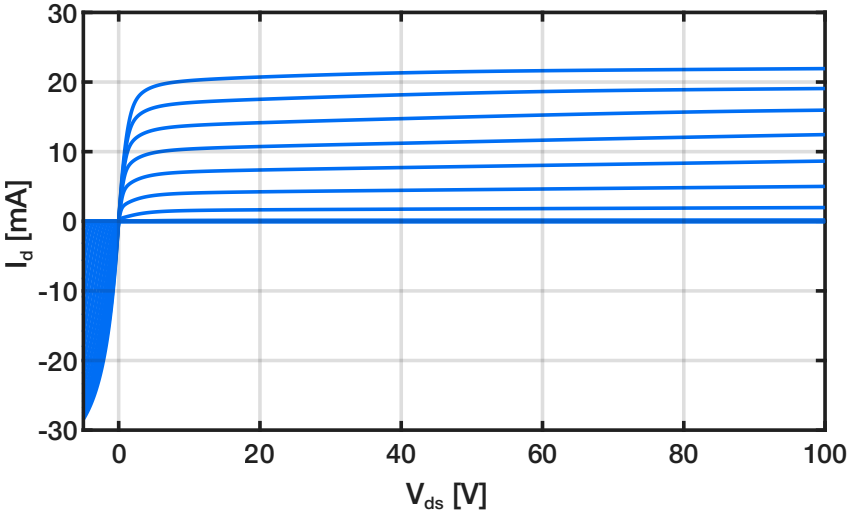

Figure 2.13: I_d-V_{ds} characteristic as a function of V_{gs} [-5 V ÷ 5 V] of a 100-V enhancement HEMT.

2.3.1 I_d-V_{ds} characteristic as a function of V_{gs}

Looking at the right part of Fig. 2.13, it can be seen that the device was tested up to 100 V, and its behavior is similar to that of the 12-V device. Direct current is present for V_{gs} values greater than 1.5 V. Another thing that can be noticed is the high current achieved even with the minimum sizes. This device also conducts an inverse current for $V_{ds} < 0$ V. For V_{gs} greater than 2 V, the inverse current is present for all values of V_{ds}, while for lower V_{gs} values, it flows only beyond a certain V_{ds}.

2.3.2 I_d-V_{ds} characteristic as a function of V_{bs}

Unlike the other devices, in this case, a wider testing range was used for the substrate voltage, sweeping it from -50 V to 50 V. This was done to simulate real conditions in a DC-DC converter, where the high-side power is biased with 50 V at the source and 0 V at the substrate, resulting in V_{bs} = -50 V.

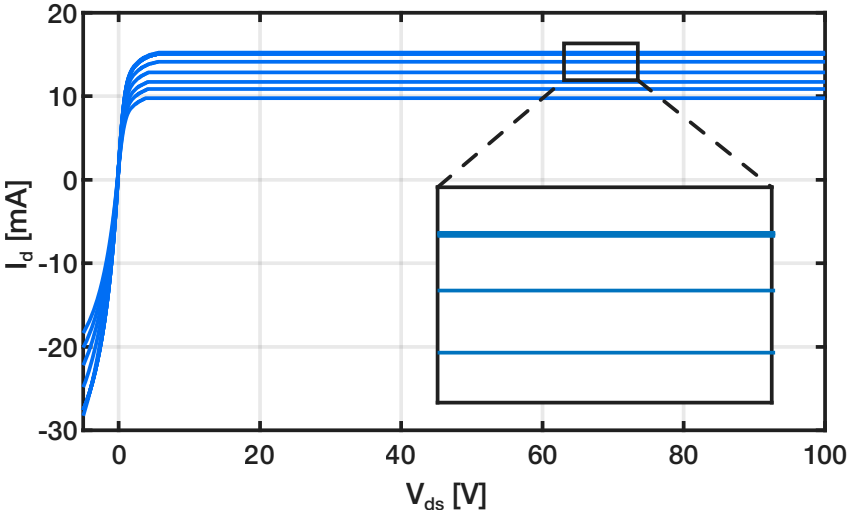

Figure 2.14: I_d-V_{ds} characteristic as a function of V_{bs} [-50 V ÷ 50 V] of a 100-V enhancement HEMT.

Looking at Fig. 2.14, the impact of this condition on the output current is significant. The drain current reduction exceeds 30% in saturation and it is also present in the linear region. This effect will be a key parameter to consider during the sizing of the power HEMTs.

2.3.3 I_d-V_{ds} characteristic as a function of Temperature

Similar to the 12-V devices, a reduction in the magnitude of the current with increasing temperatures can be observed, as shown in Fig. 2.15. This significant variation is the other crucial parameter to consider when sizing power HEMTs.

2.3.4 I_d-V_{gs} characteristic as a function of V_{ds}

Let us conclude the analysis with the I_d-V_{gs} characteristic shown in Fig. 2.13. The first thing that can be observed is the V_{th} equal to 1.5 V, higher than that of the 12-V devices. The second notable point is the large spread of the curves in the saturation region, indicating that the output resistance of this device is not as high as that of the other two devices.

2.4 Resistors

Let us now analyse the two types of resistors present in the design kit. To obtain comparable results, the same dimensions were used for both:

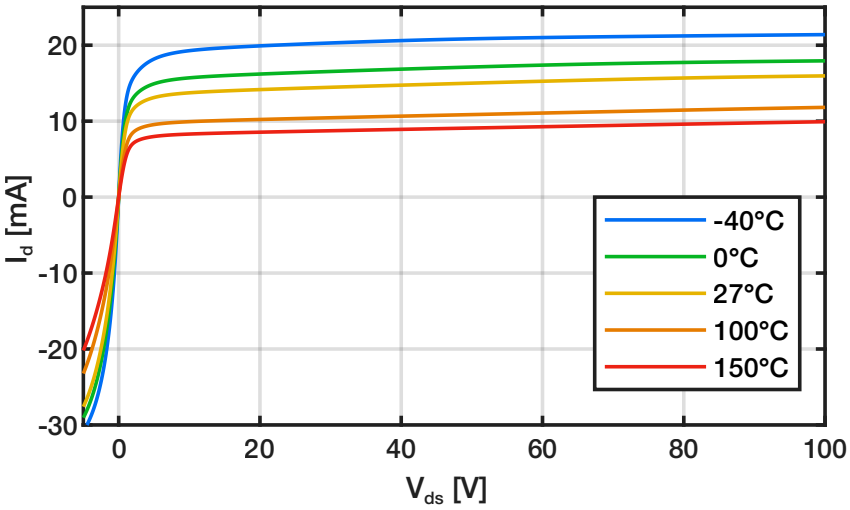

Figure 2.15: I_d-V_{ds} characteristic of a 100-V enhancement HEMT, with temperatures of: -40°C, 0°C, 27°C, 100°C and 150°C.

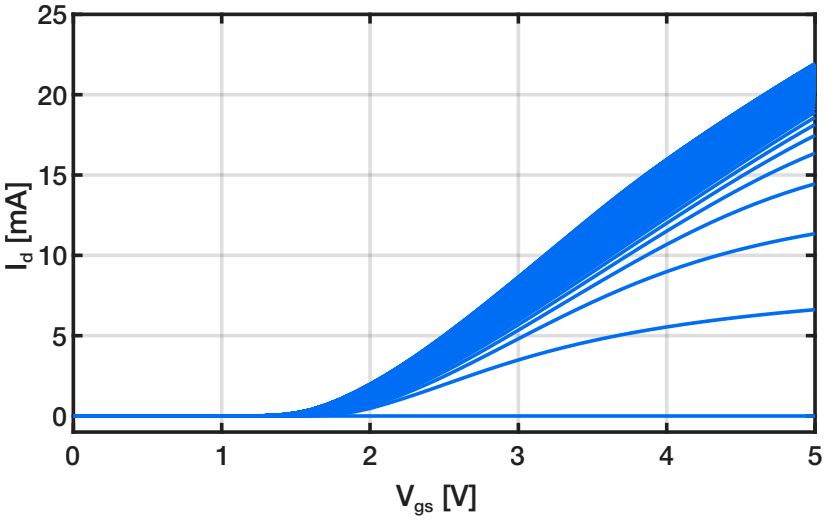

Figure 2.16: I_d-V_{gs} characteristic as a function of V_{ds} [0 V ÷ 100 V] of a 100-V enhancement HEMT.

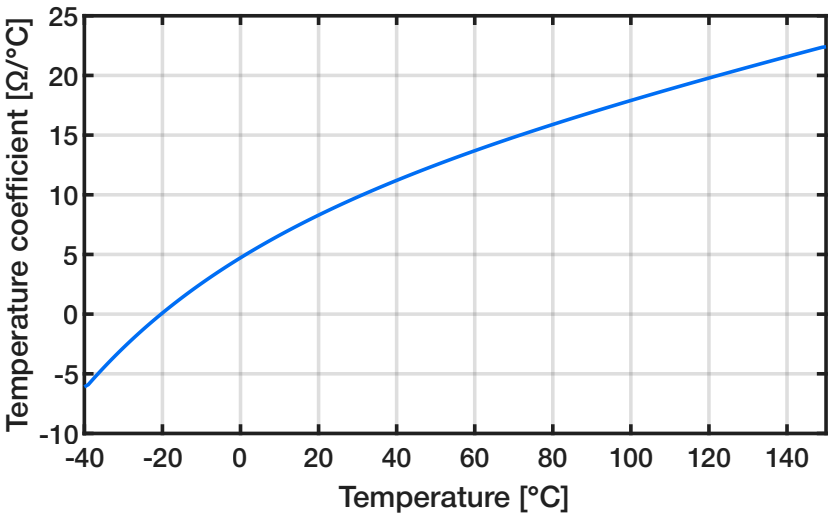

Figure 2.17: Temperature coefficient-Temperature characteristic of a GaN resistor.

- L = 7.5 µm
- W = 2.5 µm

2.4.1 GaN resistor

The first type of resistor is fabricated within the natural 2DEG channel, which introduces several related issues. The most significant characterization for a resistor is how its resistance varies with temperature, as shown in Fig. 2.20. A substantial variation in resistance can be observed, with more than a 50% change between -40°C and 150°C. In Fig. 2.17, the temperature coefficient as a function of temperature is shown, revealing two key points: first, the coefficient is non-linear, and second, it is negative up to -20°C, after which it becomes positive. However, this behavior is not consistent across all dimensions, and thus nominal values. Another important analysis concerns the influence of the substrate voltage on the resistance value, as shown in Fig. 2.18. It can be observed that the resistance value is not stable when the substrate voltage varies.

2.4.2 Thin film resistor

The second type of resistor is made by depositing a thin film of silicon-chromium, which mitigates some of the substrate-related issues. The resistance versus temperature characteristic shown in Fig. 2.20 demonstrates a

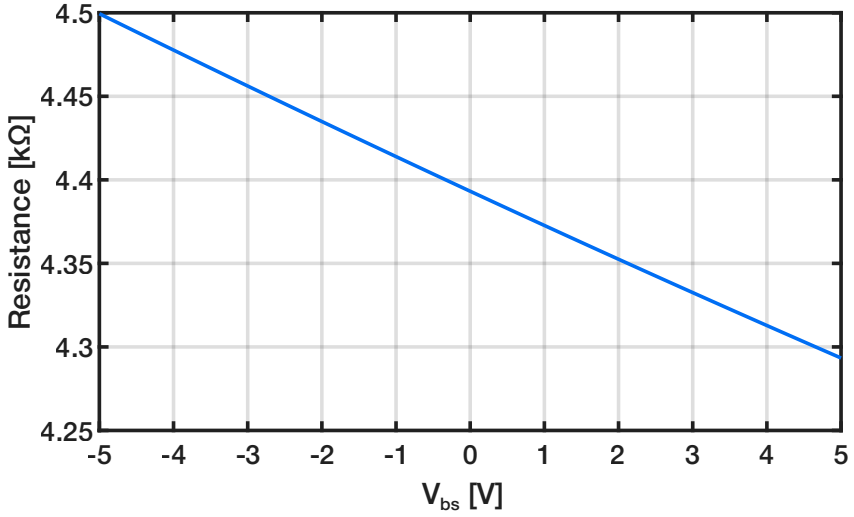

Figure 2.18: Resistance-V_{bs} characteristic of a GaN resistor.

very stable resistance over temperature. As shown in Fig. 2.19, the temperature coefficient is perfectly linear and slightly negative, almost negligible. The resistance remains stable even with variations in substrate voltage.

2.4.3 Comparison

For the same size, Fig. 2.20 shows that the GaN resistor has more than twice the resistance of the thin film resistor. At 27°C, the GaN resistor has a resistance of 4.39 kΩ, while the thin film resistor has 1.81 kΩ. Despite this, the thin film resistor (rthf) is preferred due to its nearly perfect stability with respect to both temperature and substrate voltage.

2.5 Capacitors

The design kit includes two types of capacitors: GaN capacitors and MIM capacitors. To obtain comparable results, the same sizes were used for both:

- L = 10 µm
- W = 10 µm

2.5.1 pGaN capacitor

This first type of capacitor is fabricated within GaN, which introduces several related issues. By connecting a ramp generator across the capacitor,

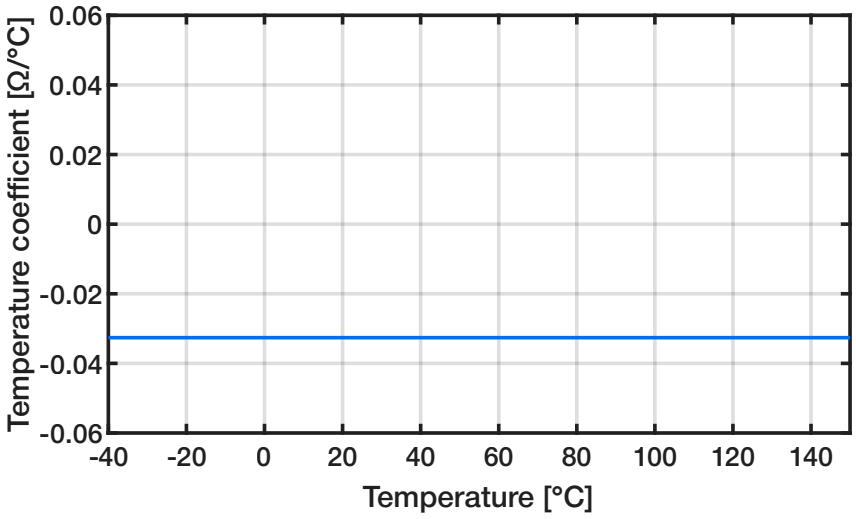

Figure 2.19: Temperature coefficient-Temperature characteristic of a thin film resistor.

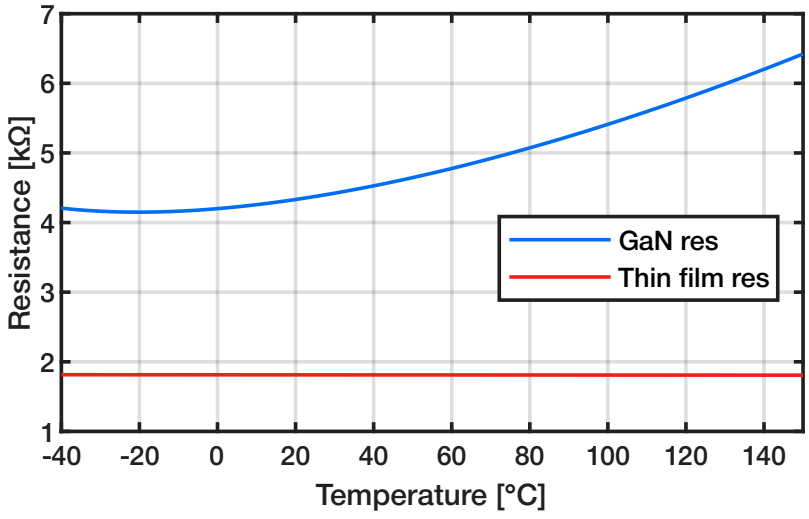

Figure 2.20: Resistance-Temperature characteristics of a GaN and a thin film resistor.

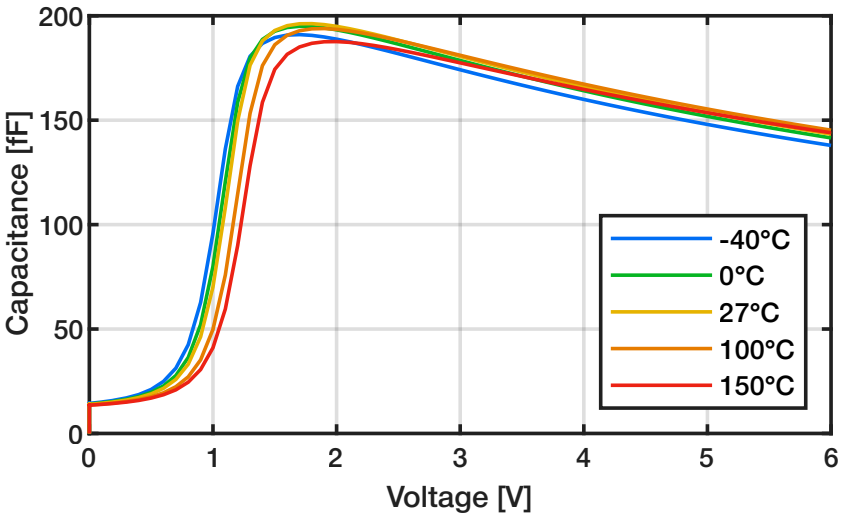

Figure 2.21: Capacitance-voltage characteristic of a pGaN capacitor, with temperatures of: -40°C, 0°C, 27°C, 100°C and 150°C.

the capacitance was measured as a function of voltage variation, as shown in Fig. 2.22. The capacitance varies significantly with changes in voltage, starting at less than 20 fF, rapidly increasing to a peak value of 196 fF at 1.7 V, and then gradually decreasing to slightly over than 140 fF at 6 V. The temperature behavior, shown in Fig. 2.21, is, as expected, not stable.

2.5.2 MIM capacitor

MIM capacitors (Metal-Insulator-Metal) are composed of two metal layers with a thin dielectric in between. As shown in Fig. 2.22, this type of capacitor exhibits a very stable capacitance value under varying voltage, which in this case is 31 fF, and the temperature stability is nearly perfect.

2.5.3 Comparison

For the same size, the pGaN capacitor has a capacitance value several times higher than the MIM capacitor, with a peak of 196 fF compared to 31 fF, as shown in Fig. 2.22. Despite this, the voltage and temperature instability of the pGaN capacitor make the MIM capacitor the preferable choice.

2.6 Conclusion

From this chapter, it can be deduced that the available technology includes two transistors for low-voltage analog design: one e-mode and one d-mode,

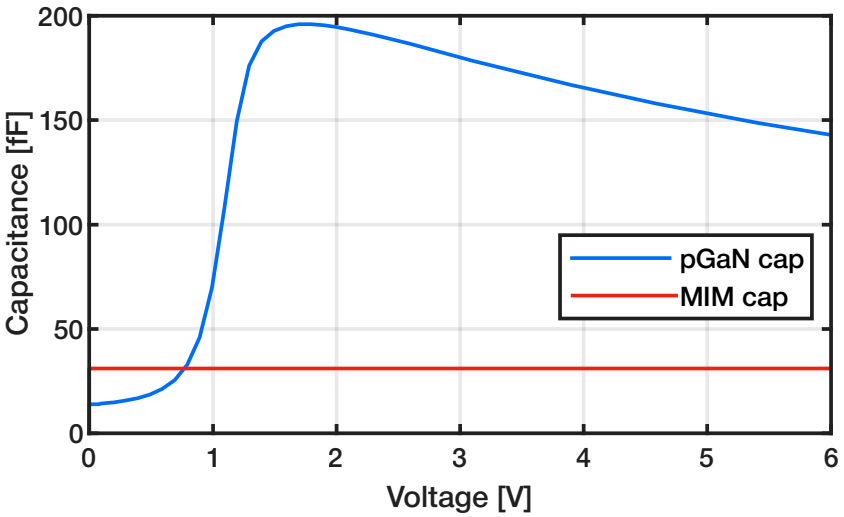

Figure 2.22: Capacitance-voltage characteristics of a GaN and a MIM capacitor.

both capable of handling high currents even at minimum sizes and to sustain 12 V between drain and source, but they are highly sensitive to temperature variations. Additionally, there is another e-mode transistor better suited for high-voltage applications, up to a maximum of 100 V, and for triode operation due to its low output impedance. However, this transistor is also prone to significant variations in performance with changes in temperature and substrate voltage. The thin film resistor is preferable to the GaN 2DEG resistor in all aspects except for square resistance[1]. Similarly, the MIM capacitor is preferable to the pGaN capacitor in most respects, such as linearity, substrate immunity and temperature variation.
Due to the early development stage of the technology, statistical models are not yet available, and thus matching and process variations have not been analyzed.

[1]It represents the resistance of a square die of conductive material. A higher value corresponds to a smaller area required to achieve the same resistance.

Chapter 3

Basic building blocks characterization

In this chapter, all the basic building blocks used to design the half-bridge and current sense circuits are characterized, with comparisons provided to explain the motivations behind choosing between different structures for implementing the same block.

3.1 Current generators

Current generators are a crucial component in analog design. Their simple structure in GaN technology makes them versatile for various applications. They can be employed in the reference branch of current mirrors and their current can be mirrored throughout the circuit. Additionally, they can be directly integrated where a current source is needed, such as in the tail current generator of a differential pair. Thanks to the normally-on d-mode transistors in this technology, start-up circuits are not required. On the other hand, due to the absence of p-channel devices, current generators can also serve as loads of low-side n-channel sections of a circuit, providing both stable current and high output impedance, effectively replacing resistors. A very high output impedance is also needed to maintain a stable current regardless of the voltage at its output terminals. The key parameters to consider are temperature stability and output impedance. In addition, stability against process variations is also an important factor that should not be overlooked.
Four different topologies are analyzed in the following of this section: three for low voltages and one for high voltages. Comparison are provided on:

- Area occupation: sum of the transistors and resistors $W \cdot L$.
- Temperature stability: percentage variation of the current over the temperature range -40°C to 150°C.

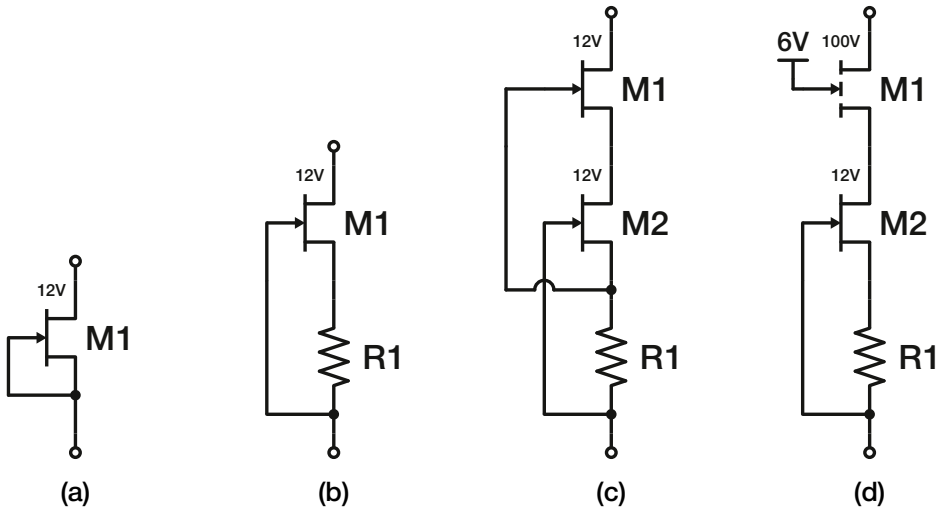

Figure 3.1: Schematic of the four considered current generator topologies: (a) simple current generator, (b) improved simple current generator, (c) cascoded current generator and (d) 100-V cascoded current generator.

- Output impedance: output impedance with a 3 V voltage drop across output terminals to guarantee the operation in saturation of the transistors.

3.1.1 Simple current generator

The simplest type of current generator is shown in Fig. 3.1(a). It utilizes a single 12 V depletion transistor with the gate connected to the source voltage. This configuration provides a high current output even at minimum sizes, but compared to the other structures, this one exhibits a lower output impedance. To reduce the current, the channel length must be increased.

3.1.2 Improved simple current generator

The limitation of the simple current generator discussed above can be addressed by adding a resistor between the source and gate, as shown in Fig. 3.1(b). This modification shifts the V_{gs} from 0 V to a negative value. As the resistance increases, the V_{gs} decreases, leading to a reduction in the current provided. This adjustment allows for more precise and stable tuning of the channel length, making it less sensitive to process variations. The resistor can be implemented using one of the two resistors available in the design kit; however, the difference in temperature stability between these implementations is significant. When using a thin film resistor, the performance

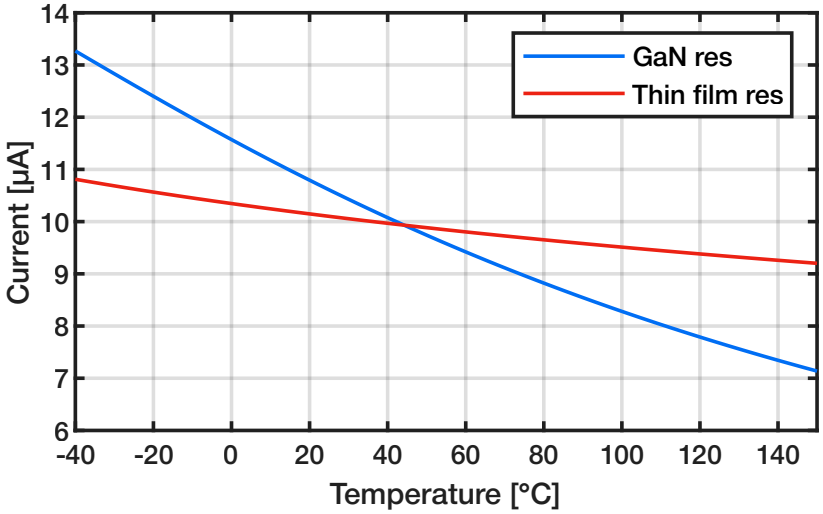

Figure 3.2: Comparison of the improved simple current generator temperature stability with the GaN and thin film resistor.

Current	Area occup.	Temp. stability	Output imp.
5 µA	535 μm^2	10.5%	37.8 MΩ
10 µA	225 μm^2	16.0%	17.3 MΩ
20 µA	120 μm^2	21.0%	7.7 MΩ

Table 3.1: Improved simple current generators comparison table for different currents.

is better than when using a GaN resistor, as shown in Fig. 3.2. To evaluate the performance of this current generator, three designs were realized for 5 µA, 10 µA and 20 µA. The data collected are summarized in Tab. 3.1. As can be seen, designing a current generator for low current levels results in an increase in transistor and resistor sizes, which also enhances temperature stability and output impedance [5]. These results correspond to specific transistor and resistor sizings; however, the same current can be achieved with different combinations of sizes, although the overall trend remains consistent.

3.1.3 Cascoded current generator

To improve the output impedance, a cascode structure is implemented, as shown in Fig. 3.1(c). While this change reduces the possible output voltage swing, it significantly increases the output impedance, which is especially crucial for high-current generators. This enhancement can be fundamental,

Current	Area occup.	Temp. stability	Output imp.
5 µA	586.3 μm^2	9.7%	191 MΩ
10 µA	255 μm^2	20.0%	51.1 MΩ
20 µA	130 μm^2	25.1%	13.5 MΩ

Table 3.2: Cascoded current generators comparison table for different currents.

Current	Area occup.	Temp. stability	Output imp.
5 µA	610 μm^2	3.1%	35.9 MΩ
10 µA	295 μm^2	10.6%	16.7 MΩ
20 µA	155 μm^2	15.6%	7.2 MΩ

Table 3.3: 100-V cascoded current generators comparison table for different currents.

for instance, to increase the gain of an amplification stage. As in the previous subsection, three current generators were designed for 5 µA, 10 µA and 20 µA, with the results summarized in Tab. 3.2. The data indicate an increase in output impedance, particularly for the 5 µA current generator.

3.1.4 100-V cascoded current generator

Considering the need for a current generator capable of withstanding high voltages, a new design was developed. As shown in Fig. 3.1(d), a 100-V enhancement device is used to cascode an improved simple current generator. This device handles the high voltage drop, protecting the components below. In this configuration, an external bias is required; however, the 6 V supply, which is common in analog circuitry in the adopted technology, makes this voltage easily accessible. Similar to the previous two topologies, three current generators were designed for 5 µA, 10 µA and 20 µA, with the results summarized in Tab. 3.3.
To obtain comparable results, the output impedance for this current generator was measured at 3 V. However, starting from approximately 4 V, the output impedance begins to rise, reaching hundreds and later thousands of MΩ. This increase is due to the 100-V enhancement device, which absorbs the excess voltage, maintaining a constant voltage across the current generator underneath. As a result, the circuit exhibits an extremely high output impedance.
This type of current generator was also utilized in this thesis work, making a deeper analysis of the 50 µA current generator particularly interesting. The area occupied is 76.3 µm^2. Similar analyses were carried out, just as with the other current generators. The current variation across the temperature range is between 55.4 µA and 43.5 µA, indicating a temperature stability of 23.8%, which is relatively low despite to the high current provided. The

	Area occup.	Temp. stability	Output imp.
Improved	225 μm^2	16.0%	17.3 MΩ
Cascoded	255 μm^2	20.0%	51.1 MΩ
100-V cascoded	295 μm^2	10.6%	16.7 MΩ

Table 3.4: 10 µA current generators comparison table.

output impedance is below 10 MΩ at 3 V, increases to 150 MΩ at 10 V, and exceeds 1000 MΩ after 15 V.

3.1.5 Comparison

Let us now summarize the collected data by focusing on the 10 µA current generators, as shown in Tab. 3.4. The increase in size across the different topologies can be observed, which is attributed to the additional transistor used in the two cascoded current generators, particularly in the 100-V cascoded current generator, which has a relatively large minimum size. Regarding temperature stability, the last topology outperforms the first two. As expected, the output impedance of the cascoded current generator is higher than that of the improved simple current generator. However, the output impedance of the high-voltage compatible current generator is surprisingly low. As mentioned earlier, this low impedance occurs only up to 4-5 V, after which it begins to rise, approaching thousands of MΩ.
For these reasons, the two current generators that will be used are the two implemented with cascoded topologies.

3.2 Current mirrors

Current mirrors are key blocks in analog design [6]. They can be used to bias branches or even to transfer information in form of current to other branches. They typically consist of a reference branch, where a current source is present, and one or more branches where a copy of the current is reproduced as accurately as possible. This current can either maintain the same ratio or vary depending on the design, allowing it to be proportionally scaled or attenuated. To ensure an accurate replica, the transistors in the mirrored branch must be insensitive to variations in V_{ds}, which is achieved through higher output impedances. Another important factor, as always, is temperature stability. Therefore, these three current mirrors were analyzed, as shown in Fig. 3.3, with respect to two key aspects: temperature stability and output impedance. In all the topologies, an ideal 10 µA current generator was placed on the reference branch and the transistors were designed to achieve a 1% matching error in the mirrored current.

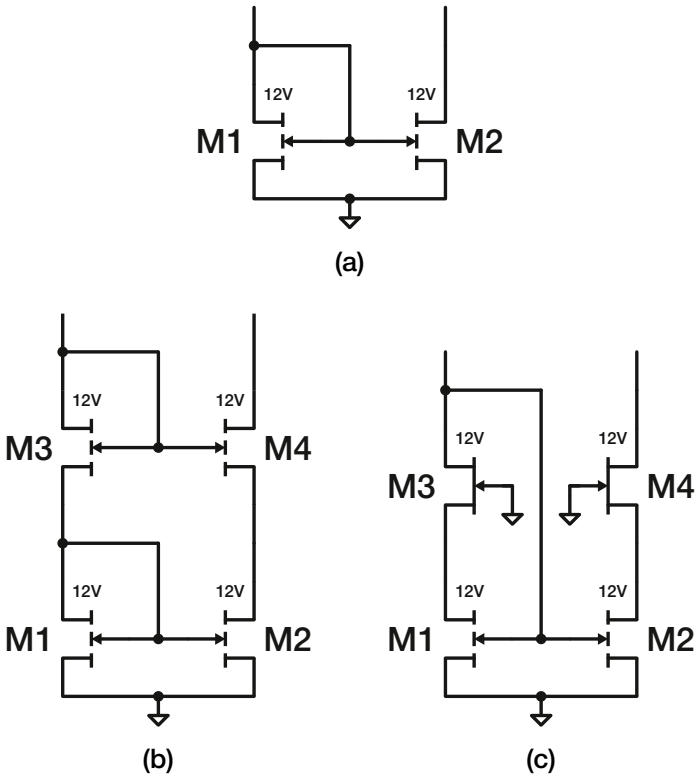

Figure 3.3: Schematic of three current mirror topologies: (a) simple current mirror, (b) cascode current mirror and (c) high compliance current mirror.

3.2.1 Simple current mirror

This topology comprises two enhancement HEMTs, as shown in Fig. 3.3(a). M1, configured as a diode, defines the reference branch, while M2, sharing the same V_{gs} as M1, mirrors the current. The dimensions of the two transistors needed to achieve a 1% matching error are:

- L = 40 µm
- W = 5 µm
- number of fingers = 1

It exhibits a variation in current with temperature of 7.1% relative to the nominal value, indicating moderately stable performance, with lower current at higher temperatures. However, it does not have a high output impedance, with values starting at less than 1 MΩ and reaching up to 25 MΩ, making the mirrored current sensitive to V_{ds} variations.

3.2.2 Cascode current mirror

In this case, four enhancement transistors are needed, as shown in Fig. 3.3(b). This topology adds an identical structure on top of a simple current mirror to increase the output impedance. The dimensions for M1 and M2 are:

- L = 5 µm
- W = 5 µm
- number of fingers = 1

while for M3 and M4:

- L = 1 µm
- W = 5 µm
- number of fingers = 1

This topology is quite stable in temperature, with only a 3% variation, and, as expected, the output impedance is increased, starting from less than 10 MΩ and reaching up to 220 MΩ. However, the drawback is a reduced output swing.

3.2.3 High compliance current mirror

To overcame this problem, a third circuit is proposed in Fig. 3.3(c). The output swing is now higher, and two depletion devices are used to cascode the two enhancement devices instead of using two more enhancement HEMTs. This avoids generating an additional bias voltage and achieves a higher output impedance. The dimensions for the two enhancement HEMTs are:

- L = 4 µm
- W = 5 µm
- number of fingers = 1

while for two depletion devices:

- L = 500 nm
- W = 5 µm
- number of fingers = 1

The temperature stability is notably high, with only a 0.7% variation. Additionally, the output impedance for low output voltages is increased, starting at more than 15 MΩ and reaching up to 65 MΩ.

	Area occup.	Temp. stability	Output imp.
Simple	400 μm^2	7.1%	1.5 MΩ
Cascode	60 μm^2	3.0%	10 MΩ
High compliance	45 μm^2	0.7%	22.5 MΩ

Table 3.5: Current mirrors comparison table.

3.2.4 Comparison

Let's give some definitions:

- Area occupation: sum of the transistors $W \cdot L$.
- Temperature stability: percentage variation of the current over the temperature range -40°C to 150°C.
- Output impedance: output impedance at 3 V output voltage[1].

The data collected are summarized in the comparison Tab. 3.5. The high compliance current mirror performs best in all categories considered in the analysis. For this reason, it will be used in all the current sensing topologies.

3.3 High-side current mirror

High-side current mirrors are generally straightforward in conventional MOS technology, they typically involve a simple transposition of the current mirrors from the low-side to the high-side using p-MOS transistors. However, in GaN technology, the situation changes significantly because p-channel devices are not available, this limitation necessitates the design of circuits that do not rely on these devices. Unfortunately, this is not always feasible, as encountered in this thesis work, and in such cases, alternative solutions must be developed. A possible approach employs a feedback loop to replicate the behavior of a classical high side current mirror, with the reference branch positioned on the right side, as depicted in Fig. 3.4.
Let us begin the analysis from a stable operating condition and suppose that the current increases on the reference branch. As a result, the source voltages of M2 and M6 tend to decrease, which increases V_{gs2} and V_{gs6}, causing these transistors to demand more current. M6 responds immediately by supplying more current, whereas M2 cannot provide additional current due to the limitation imposed by I1. The increased current demand from M2

[1]This voltage was selected based on the following considerations: a 12 V device is used for voltages between 0 V and 6 V, and in the analog circuits, the mirror is usually complemented by a similar structure on top. Therefore, 3 V is the optimal intermediate choice.

perturbs the balance at the drain node of M4, causing its voltage to drop and consequently triggering two effects. The gate voltage of M2 decreases, which in turn lowers the initially increased V_{gs2}, helping to restore the balance; simultaneously, the gate voltage of M1 also decreases, reducing V_{gs1}. This reduction in V_{gs1} decreases the current through M1, disrupting the balance at the drain of M3, which causes its voltage to rise and consequently increases the gate voltages of M5 and M6. M5 continues to supply more current until it matches the current flowing in the reference branch, and, at the same time, M6 also increases its current supply. The loop finally stabilizes when a new balanced operating point is reached.
Let us analyze the components of the structure, which will be represented in future circuits by the symbol shown in Fig. 3.4(a), and consider the associated trade-offs. The structure is composed by a low-side high compliance current mirror, similar to the one discussed in Subsec. 3.2.3, located just above the output connections. This current mirror is loaded with two identical cascode current generators, like those analyzed in Subsec. 3.1.3, which offer a very high output impedance to the mirror below. The structure is completed by two lateral transistors that supply the additional current required. For the circuit to operate perfectly without any offset under balanced conditions, the drain voltages of M3 and M4 must be equal and maintained at a suitable level that allows for adequate voltage swing in both directions. This structure introduces an important trade-off between response time and the minimum current that can flow through the branches. To achieve a faster response time, an increase in the current supplied by the two current generators is necessary; however, this leads to a reduction in the current swing possible in the branches. If the current in the reference branch decreases to I1, M5 and M6 must be turned off. This situation results in a complete imbalance in the structure: the drain voltage of M4 begins to rise, which compresses the current generator and forces the drain of M3 down, along with the gates of M5 and M6, until V_{gs5} and V_{gs6} both reach 0 V. However, to achieve $V_{gs5} = V_{gs6} = 0$ V, V_{ds1} and V_{ds3} must drop to 0 V, effectively turning off M1 and M3 and breaking the feedback loop. Therefore, when designing this structure, it is crucial to consider the minimum current that is present in the reference branch.

3.4 Power HEMT

Power transistors are the key switching elements in a buck converter, controlling the energy transfer between the input and the inductor to regulate the output voltage. GaN technology enhances performance by reducing the size of these transistors and enabling higher current handling, primarily due to the material's lower on-resistance, as discussed in Sec. 1.1 and Sec. 1.2. The smaller size leads to reduced parasitic capacitances, enabling higher

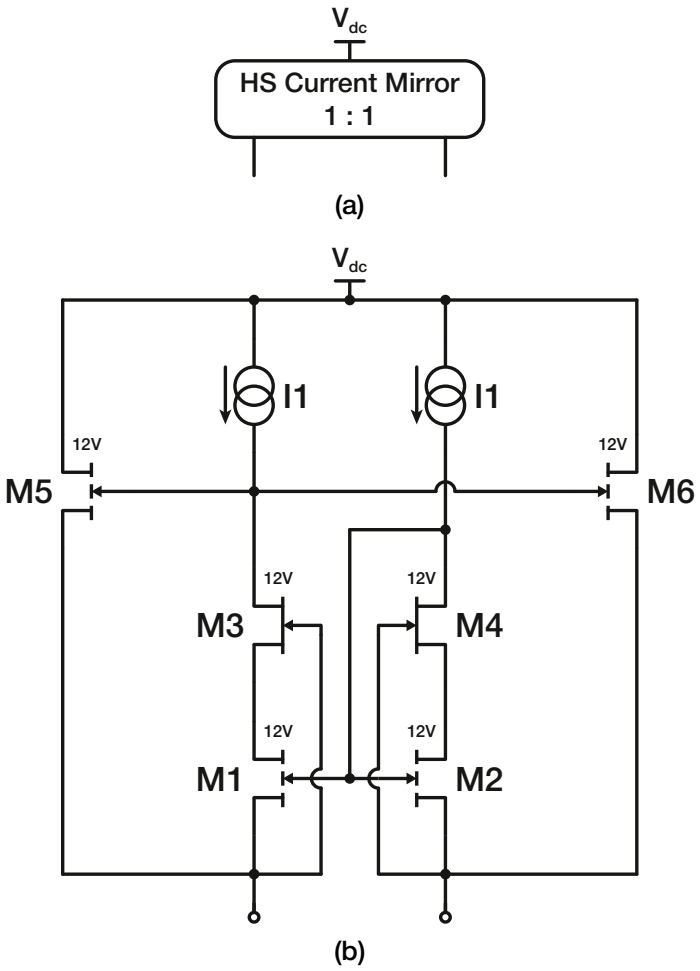

Figure 3.4: (a) Symbol and (b) schematic of the high-side current mirror.

switching frequencies and simplifying the driver design.
Let us start the sizing of the two power transistors according to the project specifications:

- Input voltage = 48 V
- Load current = 10 A

Let us give two design choices about the maximum allowable voltage drops:

- Nominal voltage drop < 1.5 V (on-resistance < 150 mΩ)
- Worst case voltage drop < 3 V (on-resistance < 300 mΩ)

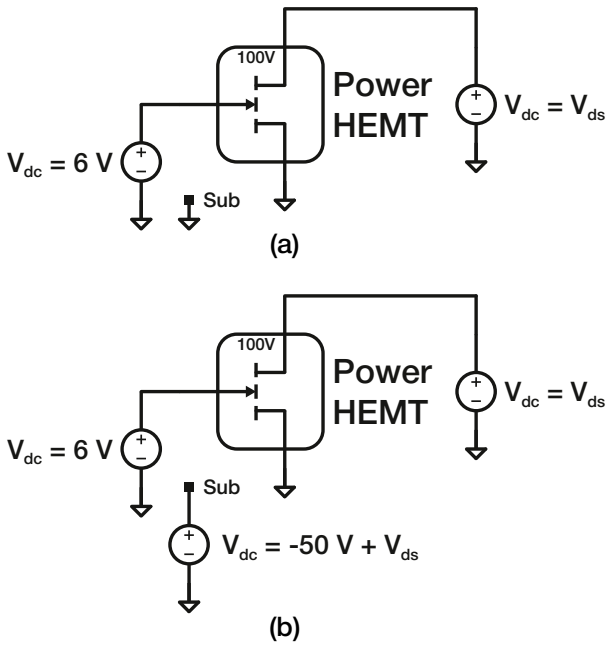

Figure 3.5: Testbench for (a) low-side power HEMT and (b) high-side power HEMT.

These parameters are chosen as a compromise between minimizing voltage drop and the effective size of the power transistors, which is related to their on-resistance.
Given the high input voltage, the most suitable device from the design kit is the 100-V enhancement transistor. The low-side and high-side HEMTs were tested using two different circuits, respectively in Fig. 3.5(a) and Fig. 3.5(b). For the low-side device, the gate was connected to the maximum voltage of 6 V, the source and substrate were grounded, and the drain was swept from 0 V to 50 V while measuring the drain current. For the high-side device, a more complex testing circuit was implemented to replicate the operation between the switching node and the input voltage to ground. The gate was connected to 6 V, the source to ground, and the drain was swept between 0 V and 50 V, as with the low-side device. However, in this case, the substrate voltage was swept from -50 V to 0 V. This approach accounts for the significant substrate effect, ensuring the reliability of the data.
The size of the transistors was adjusted to meet the design targets, resulting in the following specifications:

- L = 600 nm
- W = 55 mm

	-40°C	**27°C**	**150°C**
Low-side voltage drop	0.50 V	0.73 V	1.45 V
High-side voltage drop	0.94 V	1.36 V	2.92 V

Table 3.6: Voltage drops of the low-side and high-side power transistors at three different temperatures.

	-40°C	**27°C**	**150°C**
Low-side on-resistance	50 mΩ	73 mΩ	145 mΩ
High-side on-resistance	94 mΩ	136 mΩ	292 mΩ

Table 3.7: On-resistances of the low-side and high-side power transistors at three different temperatures.

The voltage drops for the two power transistors at three different temperatures are summarized in Tab. 3.6. Given the 10 A current load and the associated voltage drops, it is straightforward to determine the on-resistances for the different scenarios. These are summarized in Tab. 3.7.
Regarding the number of fingers, in order to achieve a good current sense, minimum size fingers are preferable. Therefore, for symmetry reasons, both power transistors were divided into 1100 fingers of minimum size. To manage this large number of fingers, each transistor was further divided into 11 sub-transistors, as shown in Fig. 3.6, with the dimensions of:

- L = 600 nm
- W = 5 mm
- number of fingers = 100

The layout of these transistors is shown in Fig. 3.7, and it can be seen that the area occupied by a single power HEMT is of 0.35 mm^2.
This structure will be represented in future schematics by the symbol shown in Fig. 3.5.

3.5 Clamps

Clamps are circuits used to limit voltage levels or protect other circuits. They typically consist of diodes that may have different threshold voltages.

3.5.1 Anti-divergence clamp

As shown in Fig. 3.8(a), the anti-divergence clamp consists of two e-mode transistors with their gates connected to the source, effectively forming two

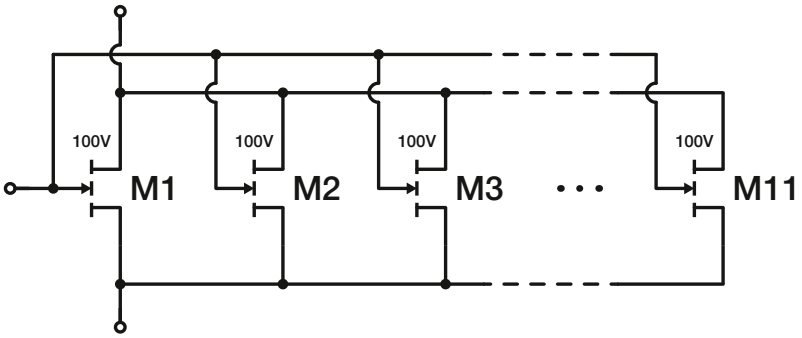

Figure 3.6: Schematic of the power HEMT.

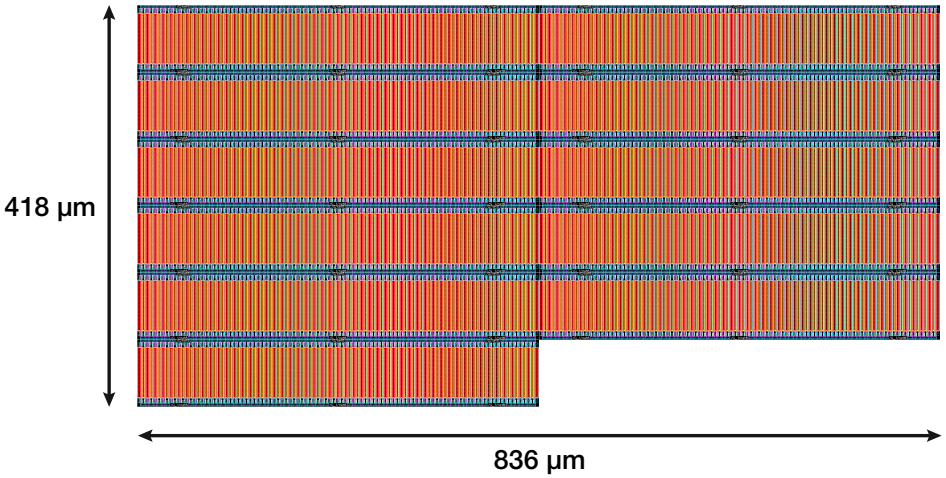

Figure 3.7: Layout of the power HEMT.

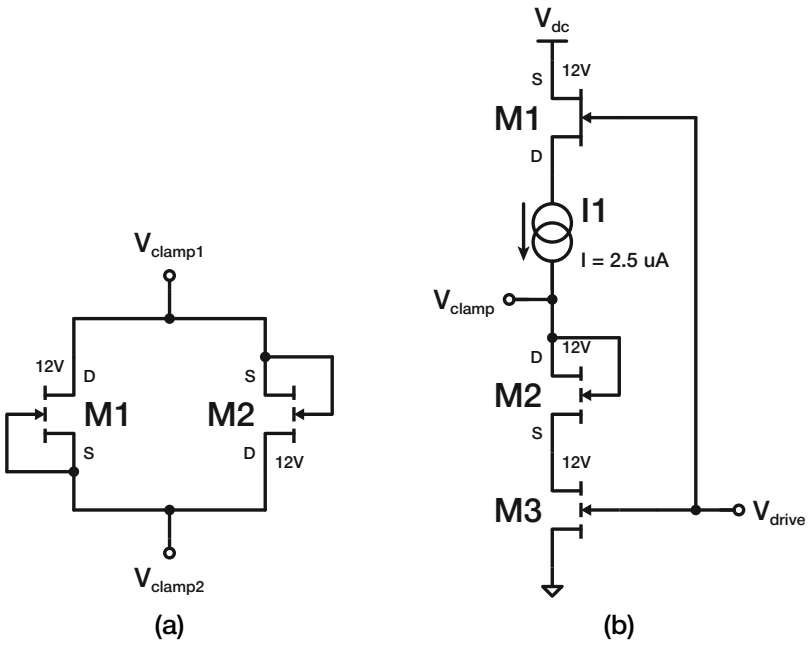

Figure 3.8: Schematics of the (a) anti-divergence clamp and the (b) dual-phase clamp.

diodes. These diodes are connected in parallel in opposite directions, ensuring that, regardless of whether V_{clamp1} or V_{clamp2} is at a higher voltage, the voltage difference between the two in both direction cannot exceed 2.5 V, as illustrated in Fig. 3.9.

3.5.2 Dual-phase clamp

The dual-phase clamp is more complex than the previous one, as shown in Fig. 3.8(b). It operates as a clamp only when V_{drive} is high, with M1 and M3 functioning as switches. To simplify the top switch, a depletion transistor with the source above and the drain below is used. In this configuration, when V_{drive} is high, V_{gs} is 0 V, allowing conduction. When V_{drive} is low, the depletion-mode device, with a V_{gs} of -6 V, acts as an open switch. When the clamp is active, a diode, formed by connecting the gate to the drain of an enhancement transistor, is charged by a low current generator, similar to the one described in Sec. 3.1.2. This configuration clamps the voltage to 1.3 V, as shown in Fig. 3.10, regardless of whether the input voltage is lower or higher, thanks to the current generator. When the clamp is off, the signal is free to follow the input voltage if it is higher than the clamp voltage.

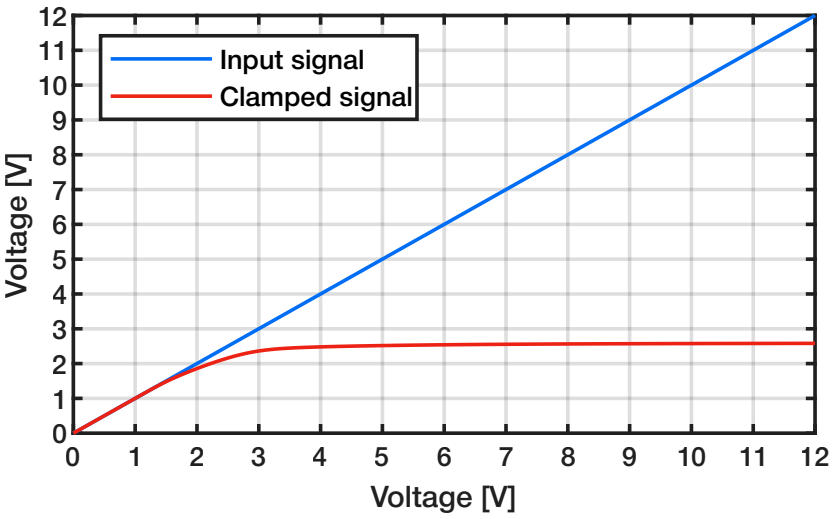

Figure 3.9: Anti-divergence clamp signal.

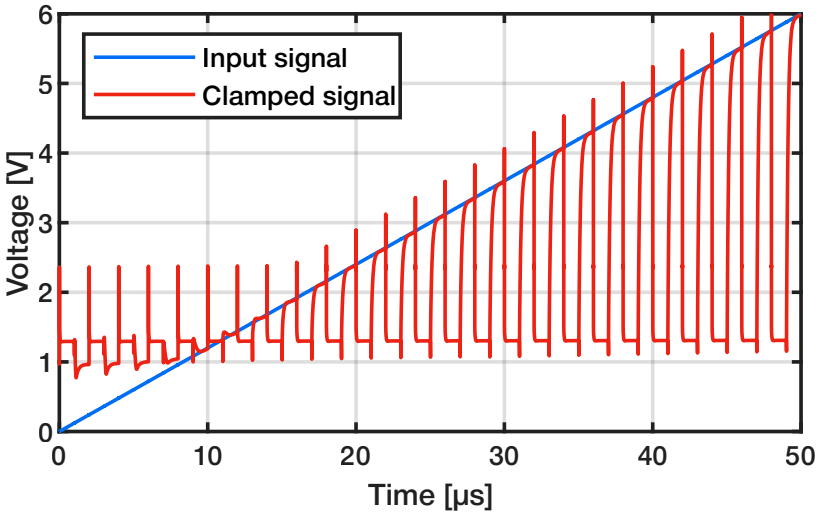

Figure 3.10: Dual-phase clamp signal.

Chapter 4

Current sense

The current sense circuit, connected to the high-side power transistor, has two objectives in this thesis work:

- Ripple following: tracks the ripple of the current in the high-side power transistor.
- Zero-current detection: monitors when the current in the high-side power transistor drops to zero.

When the gate voltage of the high-side power transistor rises, current starts to flow from the input to the output. This current is not constant, it has a ripple, as shown in Fig. 4.1. To accurately control the high-side on-time duration, precise information on the current passing through the transistor is needed. This allows the control loop to send a signal to the driver to turn off the high-side transistor when the current reaches a certain value. If the current information is affected by offsets, incorrect data will lead to an inaccurate output voltage level. The circuit also has a crucial role when the high-side transistor turns off. The current does not stop flowing immediately,

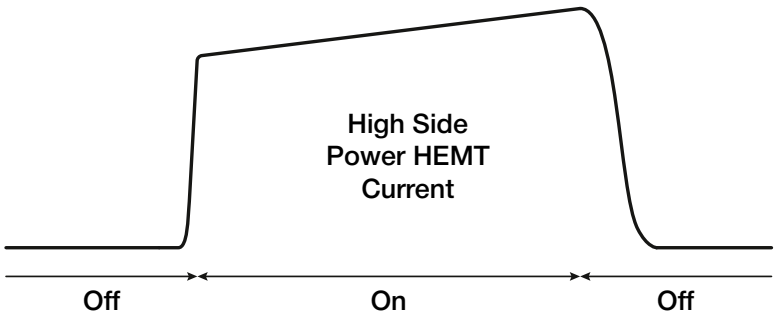

Figure 4.1: High-side power HEMT current.

as shown in Fig. 4.1, a variable amount of time is needed for it to cease. If the low-side transistor is turned on while current is still present, a very large cross-conduction current would pass through the two power transistors from the input to ground, reducing efficiency and potentially damaging the circuit. Instead of using a large fixed delay to cover the worst-case scenario, thereby degrading circuit performance in the other situations, a zero-current detection is required. Thus, this current sense circuit also takes over the function of the disoverlap circuit, which is discussed in Sec. 4.1.2.
The information obtained from the high-side transistor is referenced to the switching node (SW) of the buck converter, making it unusable in its form since it fluctuates with the switching signal. To be effective, this information needs to be consistently referenced to ground. During the preliminary analysis, several topologies were developed to translate this information to the low side. All open-loop topologies were discarded because their output was not independent of temperature, line, and load variations. Concluding that a closed-loop topology was the best choice, various other structures were analyzed, ultimately leading to the general scheme shown in Fig. 4.2. The main component of this structure is the sense transistor, with its drain connected to the input voltage, and its gate connected to the same voltage as the high-side power transistor, supplied by the driver. The source is part of a loop that restores the voltage present at the source of the power transistor, which corresponds to the voltage at the switching node. In this configuration, the sense transistor is connected to the same three voltages as the high-side power HEMT, ensuring that the current passing through it is the same, scaled by a factor determined by their sizes [7]. The loop consists of an operational amplifier and a structure that closes on the source of the sense transistor, providing a path to ground for the current flowing through it. The operational amplifier is the critical component of this circuit. It must be designed to minimize offset across all conditions of temperature, line voltages, and load currents. Additionally, the amplifier must have a fast response time to function effectively at high frequencies. A high gain is also important, as it reduces offsets related to the voltage difference between the sources of the power and sense transistors. The loop-closing structure includes a mirror branch of a high-compliance current mirror, cascoded by a 100-V enhancement transistor that protects the underlying structure when the switching node is at high voltages. The output information is extracted via another high-compliance mirror branch. A buffer is required to connect the two drains of the depletion transistors, because in this configuration, when the switching node drops to zero, it turns off the current mirror via the drain rather than the gate. This ensures that, like the sense transistor, the two current mirror branches are connected to the same three voltages. The operational amplifier for the buffer is less complex and demanding, it only needs a relatively low gain of 40 dB and is already referenced to ground. Therefore, it was not implemented at the transistor level, and the current

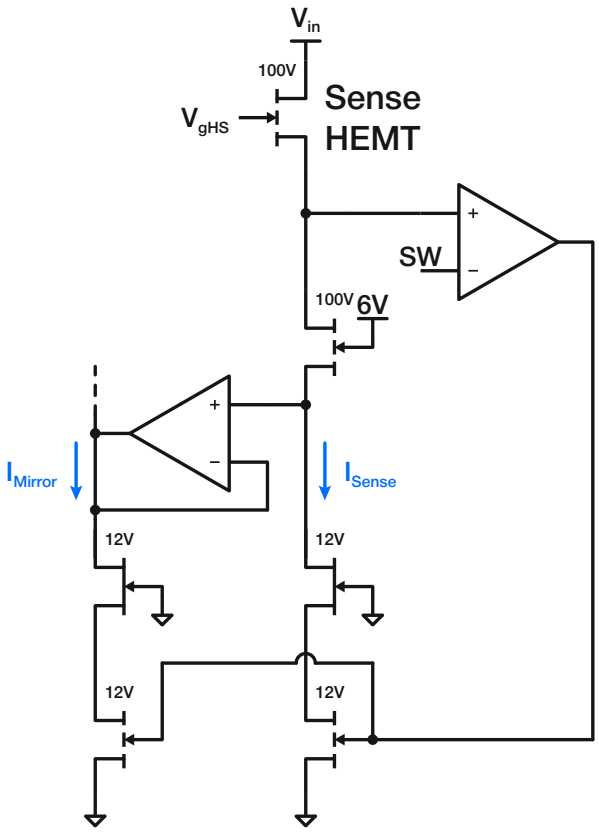

Figure 4.2: Current sense general scheme.

used for analysis is the one flowing through the sense transistor.
The design of the sense transistor is another key aspect, involving trade-offs between current consumption, accuracy, and area. A single-finger implementation can lead to matching inaccuracies and significant offsets in the sense current. This occurs because of the differences in the physical structure between single-finger and multi-finger transistors. Three design choices can be considered:

- keep the offset
- double-finger sense transistor
- double-finger sense transistor and double the size of the power transistor

The first solution, given the required circuit performance, was not considered. The second option addresses the offset problem through better matching, but it doubles the already non-negligible current in the sense transistor

branch. To maintain the same current as the single-finger solution, a power transistor with twice the size would be required. Given the substantial area needed to double its size, the second option was selected. With this implementation, the size of the sense transistor is:

- L = 600 nm
- W = 100 µm
- number of fingers = 2

Considering the dimension of the power transistor discussed in Sec. 3.4 and the load current of 10 A, an 18.18 mA current will flow through the sense transistor under ideal conditions, with a scaling factor of 550.
The parameters used to analyze the different circuits are:

- current offset: the difference between the ideal sense current and the actual obtained sense current at the conclusion of switching during ripple following;
- response time: the time required for the sense current to stabilize to the correct value during switching.

All analyses are conducted under typical corner, and no process spread analyses are provided due to the early stage of the technology and immaturity of the models.

4.1 Testbench

To test the circuit without designing a full buck converter and to avoid its non-idealities, a testbench is required and a schematic representation is shown in Fig. 4.3. It consists of two power transistors, a driver, and two ideal generators. The power transistors have already been discussed, while the driver is covered in the next section. The ideal current generator replaces the inductor generating a current equal to what would have been present in the high-side power transistor in a fully implemented buck converter. An ideal voltage pulse generator, on the other hand, is used to provide the PWM signal to the half bridge. Both generators are parameterized to easily modify the period, duty cycle, load current, and ripple. The V_{in} and V_{dc} terminals are connected to ideal dc voltage generators, with the first one parameterized to easily vary the line voltage.
The settings for the tests are as follows:

- period = 4 µs
- duty cycle = 50%

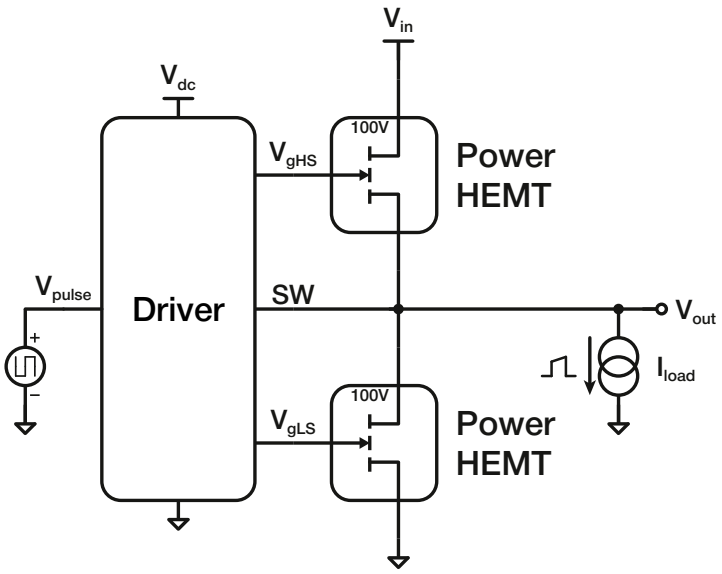

Figure 4.3: Testbench for the current sense circuits.

- load current = 10 A
- ripple = 10%
- line voltage = 50 V
- dc voltage = 6 V

4.1.1 Driver

The driver's purpose is to take the voltage from the ideal pulse voltage generator and produce the signals needed to drive the two power transistors [8]. These signals must be timed and strong enough to meet specific criteria: the timing must prevent both power transistors from being on simultaneously, thereby avoiding cross-conduction, while the strength must ensure that, even under worst-case conditions, the phase node (SW) maintains a minimum slope of 10 V/ns, which is another design requirement. Fig. 4.4 illustrates a schematic representation of the driver consisting of a real final driving stage, with all other components modeled as ideal. The bootstraps and level-shifters are implemented using voltage-controlled voltage sources (VCVS), while the disoverlap is realized with ideal logic gates, as explained in the following section. The four driving signals switch between 0 V and 6 V, corresponding to logic states 0 and 1.

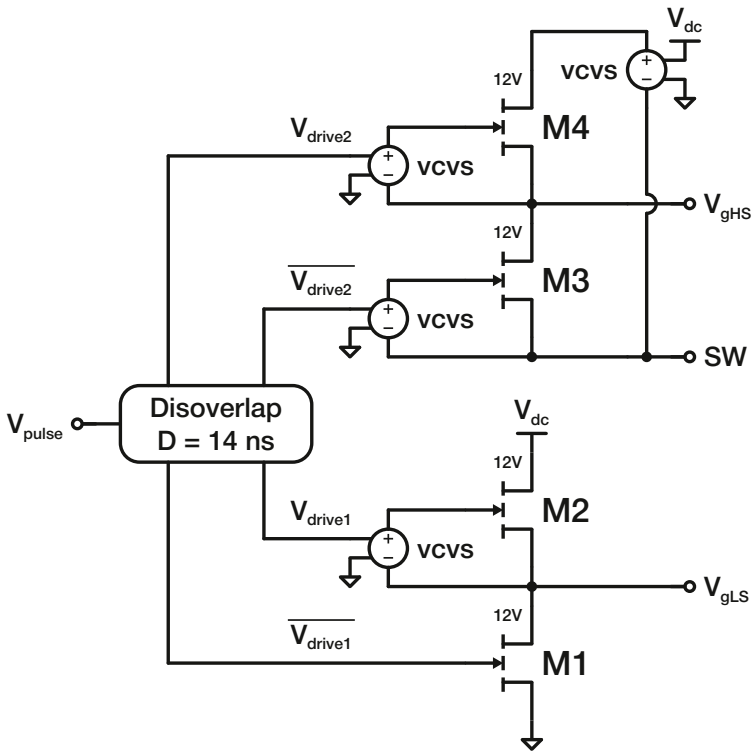

Figure 4.4: Driver circuit.

Let's now describe the circuit operation in detail, referring to the schematic of the driver in Fig. 4.4 and the switching voltage in Fig. 4.5. Starting with the soft-switch major transition (a), the switching node is initially high and needs to be pulled down. To achieve this, the high-side power transistor must be turned off by setting V_{gHS} to 0 V and this is done by turning on M3 and turning off M4. The gate voltage of M3 must remain 6 V above the switching node throughout the transition; therefore, a VCVS is connected between the SW node and the gate of M3, driven by the signal from the dead-time control circuit. The inductor pulls down the switching node, but to control the slope, M3 must be appropriately sized. Additionally, the voltage supply for the high-side driver is bootstrapped from the switching node itself. Once the transition is completed, after a delay set by the dead-time control to prevent cross-conduction, the low-side power transistor is turned on, bringing the switching node up to 0 V plus the V_{ds} of the low-sside power transistor. This hard-switch minor transition (b) is managed by M2. Like M3, M2 is connected to the disoverlap circuit, with its gate bootstrapped relative to the source voltage. The strength of M2 is less critical for proper circuit operation, so its width was set to the minimum

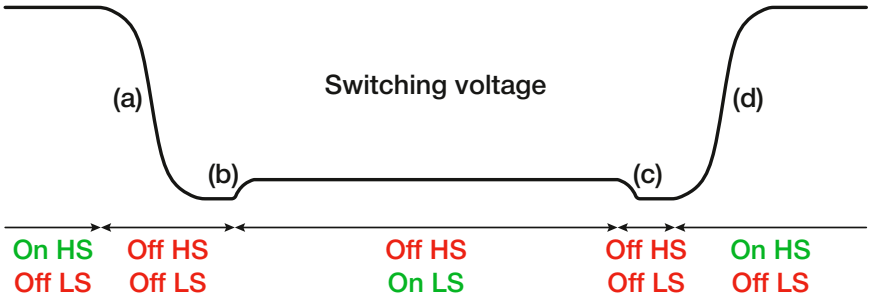

Figure 4.5: Switching voltage.

	M1	**M2**	**M3**	**M4**
On HS, Off LS	On	Off	On	Off
Off HS, Off LS	On	Off	Off	On
Off HS, On LS	Off	On	Off	On
Strength (W)	1.6 mm	260 μm	260 μm	500 μm

Table 4.1: Driver transistors states and strengths.

required by the others. Before raising the switching node again, the low-side power transistor must be turned off to avoid cross-conduction. The soft-switch transition (c) is managed by M1, and in this case, its width is crucial. During the hard-switch major transition (d), the switching node voltage rapidly rises to the maximum value. During this transition, the initially discharged parasitic capacitor C_{gd} of the low-side power transistor must charge quickly, requiring a large current. This current flows through the on-resistance of M1, which keeps the low-side power HEMT off. If the on-resistance is not low enough, V_{gLS} will start to rise, and once it crosses the V_{th}, the low-side power transistor will turn on, causing a short-circuit. Returning to transition (d), it is managed by M4, which turns on the high-side power transistor with sufficient strength to ensure the correct minimum slope is achieved under worst-case conditions.
The states and strengths of the driving transistors are summarized in Tab. 4.1, while the slopes of the switching node at three different temperatures are shown in Tab. 4.2. As described above, M1 is sized over three times larger than the others to prevent the current flowing through its on-resistance from inadvertently turning on the low-side power transistor when it should remain off. With this sizing, V_{gLS} never exceeds 1 V, while the threshold voltage of the power transistor is 1.5 V. Another important observation is that the slope of the hard-switch transition (d) varies significantly with temperature.

	-40°C	**27°C**	**150°C**
Transition (a)	-26.6 V/ns	-20.4 V/ns	-10.2 V/ns
Transition (d)	57.2 V/ns	40.9 V/ns	10.2 V/ns

Table 4.2: Slopes of the switching node at three different temperatures.

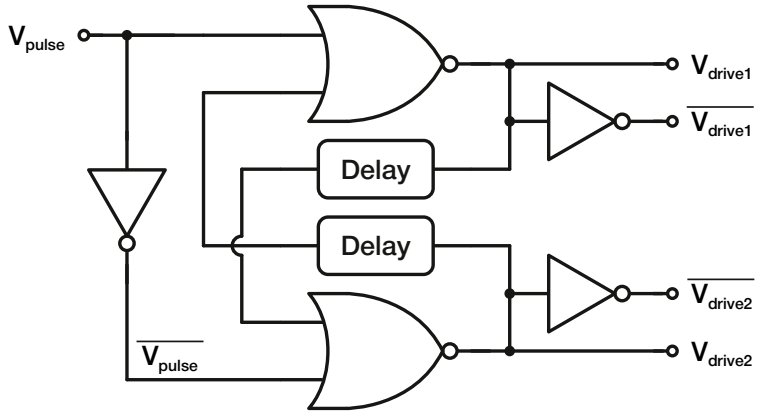

Figure 4.6: Disoverlap circuit.

4.1.2 Disoverlap

The disoverlap circuit, or dead-time control circuit, is a key component of the driver, ensuring that the high-side and low-side power stages are never active simultaneously. A possible design is shown in Fig. 4.6, it uses a limited number of logic gates: 2 NOR gates, 3 inverters, and 2 delay blocks. Starting from an input signal, V_{pulse}, generated by the pulse generator, it produces two non-overlapping output signals, V_{drive1} and V_{drive2}, along with their negated signal. The amount of disoverlap is determined by the two

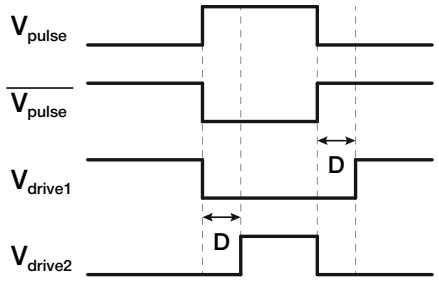

Figure 4.7: Disoverlap signals.

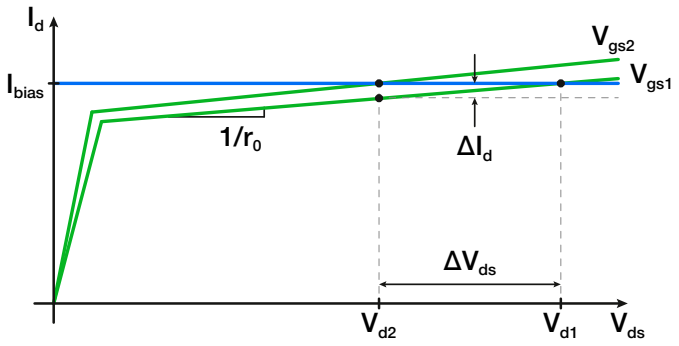

Figure 4.8: Operating principle of the information translation with the 100V HEMT.

delay blocks. A clear representation of the circuit signals is shown in Fig. 4.7, where it is exaggerated to illustrate that the two driving signals are never both active simultaneously. In practice, the disoverlap time D is a very small percentage of the period. In this case, a delay of 14 ns was chosen to prevent cross-conduction, considering the following worst-case scenario:

- line voltage = 100 V
- temperature = 150°C
- load current = 1 A

4.2 Degenerated 100V HEMT current sense

The first implementation of the amplifier, shown in Fig. 4.9, consists of three amplification stages. The technique used to translate the signal to ground relies on a 100-V enhancement transistor, with its inherently low output resistance further degenerated by two resistors. The working principle is illustrated in Fig. 4.8. The 100-V enhancement transistor is biased with a constant current, and its gate voltage is fixed at 6 V. When the drain voltage drops, the operating point shifts, causing the current to deviate from the bias current and to compensate V_{gs} must increase. Since the gate voltage remains fixed, the source voltage must decrease to establish a new operating point. This mechanism enables the translation of information from the high voltage at the drain to the lower voltage at the source. However, this process results in an attenuation greater than 50 dB, which must be compensated by the subsequent amplification stages. The underlying mechanism is explained by Eqs. (4.1), (4.2) and (4.3). To reduce the attenuation, a large resistor is placed in parallel, with an additional resistor connected between the transistor's source and one end of the parallel resistor. The first resistor serves

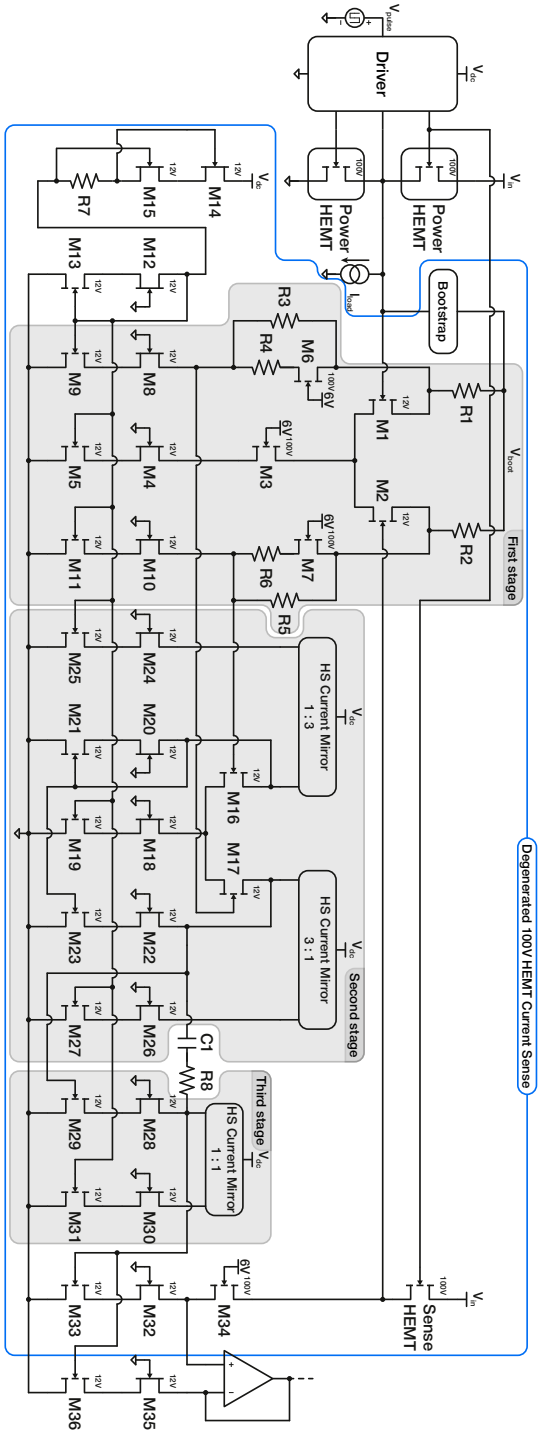

Figure 4.9: Schematic of the degenerated 100V HEMT current sense.

to degrade the output impedance, while the second resistor reduces the G_m of the structure and adjusts the voltage translation to a level compatible with the subsequent stage.

$$\Delta I_d = \frac{\Delta V_{ds}}{r_0} \tag{4.1}$$

$$\Delta V_{gs} = \frac{1}{g_m} \cdot \Delta I_d = \frac{\Delta V_{ds}}{g_m r_0} \tag{4.2}$$

$$\frac{\Delta V_{gs}}{\Delta V_{ds}} = \frac{1}{g_m r_0} \tag{4.3}$$

Let us analyze the operation of this circuit. The core components are the two transistors, M1 and M2, with their gates connected respectively to the source of the high-side power transistor (the switching node) and the source of the sense transistor. If the voltage at the source of the sense transistor matches that of the high-side power transistor, the circuit will be perfectly balanced, and the sense current will be an accurate scaled replica of the current flowing through the high-side power transistor. Achieving this requires high gain and the elimination of offset. To accomplish this, a single current generator is used for the entire structure, with its current mirrored throughout the circuit. The cascoded current generator, described in Sec. 3.1.3 and consisting of M14, M15, and R7, was selected to provide high impedance despite the relatively high current generated. The bias current was chosen based on a trade-off between power consumption and the output impedance of the 100-V enhancement devices used to translate the signal. A higher current reduces output impedance but increases power consumption, so a bias current of 100 µA was selected. Twice the bias current is mirrored into the differential pair by M4 and M5, which are cascoded by M3. Resistors R1 and R2 were used instead of a current generator to set a precise voltage at the drains of M1 and M2 and to minimize offset, despite the lower impedance offered to the differential pair. They are connected to a bootstrapped voltage from the switching node (realized with an ideal block), allowing sufficient voltage headroom for the differential pair. As a result, this amplification stage moves up and down with the switching node. After translation, the voltage difference at the drains of M8 and M10, the outputs of the first stage, is applied to a second differential pair composed of M16 and M17. This second stage is similar to the first but serves a different function, it performs single-ended conversion rather than translation. To achieve high gain, a high impedance is required on the differential pair, making a current generator preferable to a resistor. To minimize offset, two high-side current mirrors were employed, ensuring that current variations are consistent with those in the rest of the circuit. The drawback of this approach is the additional power consumption due to the two mirroring branches, which must

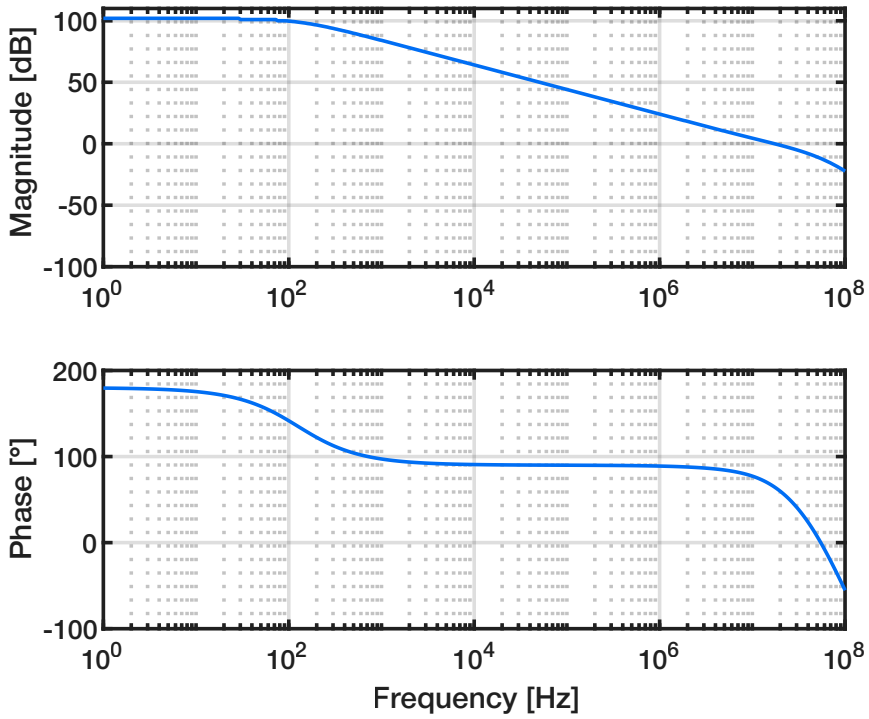

Figure 4.10: Loop gain and phase of the Degenerated 100V HEMT current sense.

bias the input pair with three times the bias current each. To mitigate this, a mirroring factor of three was used. Unlike the previous stage, the outer branches of this stage are used for single-ended conversion. The left branch, consisting of M20 and M21, is diode-connected, while the output is taken from the drain of M22. This output is then connected to the third single-ended amplification stage, composed of M29 and M28, and is biased by a high-side current mirror for the same reasons as before. The drain of M28 serves as the output of the amplifier shown in Fig. 4.2, which is connected to the source of the sense transistor through M32, M33, and M34. A copy of the current is extracted by M35, M36, and the buffer to close with a control loop on the driver input. The structure is simply compensated between the second and the third amplification stage by an 8.5 pF MIM capacitor C1 to split the poles and a 2 kΩ thin film resistor R8 that introduces a zero [9].

4.2.1 Frequency response

As shown in Fig. 4.10, the loop gain of this structure is very high, exceeding 100 dB, which helps to minimize the error in the sense current, and a

Temperature	Loop Gain	Bandwidth	Phase Margin
-40°C	100.4 dB	29.5 MHz	60.5°
27°C	101.7 dB	17.3 MHz	66°
150°C	103.4 dB	9.1 MHz	50.1°

Table 4.3: Loop gain, bandwidth and phase margin of the degenerated 100V HEMT current sense.

bandwidth greater than 17 MHz ensures good circuit responsiveness. The phase margin was set at 66°, achieved through compensation capacitance and resistance, with a target minimum of 50° across the entire range from 30 V to 70 V. Tab. 4.3 presents the loop gain, bandwidth, and phase margin at three different temperatures, revealing that while the gain remains stable, the bandwidth varies. At higher temperatures, the phase margin tends to degrade, but the minimum design requirement is still met.

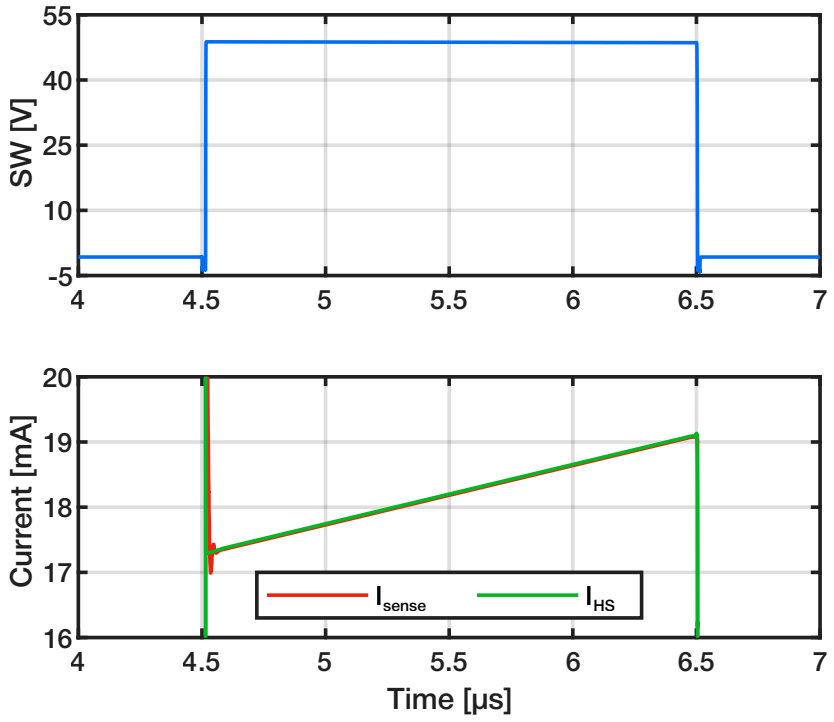

Figure 4.11: Ripple following of the degenerated 100V HEMT current sense in nominal condition.

Temperature	Current Offset	Response Time
-40°C	23.5 µA	230 ns
27°C	17.1 µA	165 ns
150°C	28.5 µA	230 ns

Table 4.4: Current offset and response time at three temperatures of the degenerated 100V HEMT current sense.

Input Voltage	Current Offset	Response Time
10 V	240.1 µA	90 ns
30 V	34.1 µA	90 ns
50 V	17.1 µA	165 ns
70 V	15.9 µA	165 ns
100 V	X	X

Table 4.5: Current offset and response time at five input voltages of the degenerated 100V HEMT current sense.

4.2.2 Ripple following

The primary task of the circuit is ripple following. In Fig. 4.11, the circuit's response to high-side current variation under nominal conditions is shown, with the temperature at 27°C, input voltage at 50 V, load current at 10 A, frequency at 250 kHz, and a duty cycle of 50%. The results indicate a current offset of 17.1 µA and a response time of 165 ns. Tab. 4.4 details the circuit's behavior across different temperatures, showing that while the current offset remains relatively stable, the response time tends to increase. Tab. 4.5 presents the current offset and response time across the entire input voltage range the circuit may encounter. From 30 V to 70 V, both parameters remain stable; however, at lower input voltages, the current offset rises sharply, and at higher input voltages, the circuit ceases to function, with the sense current flatlining at zero. Additionally, as the load current decreases, the current offset increases, as shown in Tab. 4.6. Fig. 4.12 shows the behavior of the circuit at different frequencies, and it can be observed that the response of the circuit tends to improve at higher frequencies, likely due to the incomplete discharge of parasitic capacitances, which leads to faster turn-on. However, the current offset deteriorates, particularly at low current loads.
Tab. 4.7 presents a comparison between nominal conditions and the worst-case scenario, which occurs at -40°C, with a 70 V input voltage and 1 A load current. This is not the absolute worst condition, as the circuit fails to operate under various other scenarios. The operating range of the circuit is limited to input voltages between 30 V and 70 V, but even within this range, both the current offset and response time significantly deteriorate in certain

Load Current	Current Offset	Response Time
1 A	62.4 µA	305 ns
5 A	29.1 µA	125 ns
10 A	17.1 µA	165 ns

Table 4.6: Current offset and response time at three load currents of the degenerated 100V HEMT current sense.

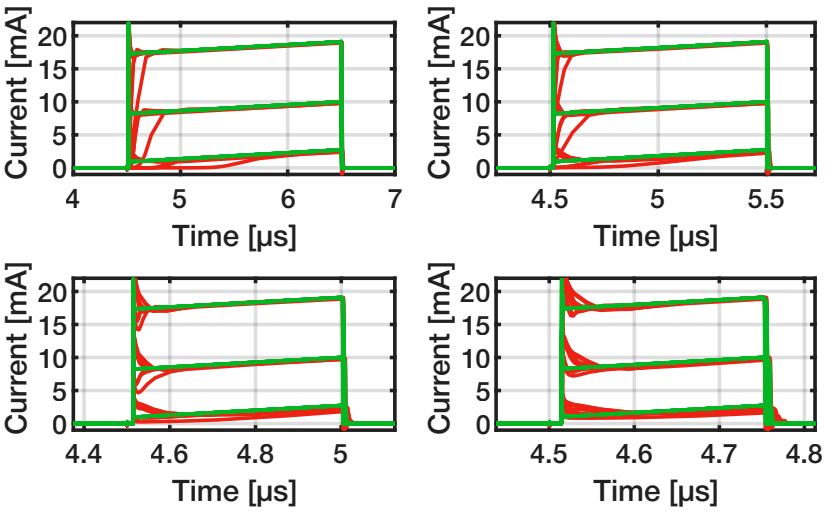

Figure 4.12: Ripple following of the degenerated 100V HEMT current sense at four different frequencies: 250 kHz, 500 kHz, 1 MHz and 2 MHz with 50% duty cycle. Each figure shows the sense current at temperatures in the range [-40°C ÷ 150°C], input voltages in the range [30 V ÷ 70 V] and load currents in the range [1 A ÷ 10 A].

	Current Offset	Response Time
Nominal	17.1 µA	165 ns
Worst	450 µA	1500 ns

Table 4.7: Current offset and response time in the nominal and worst case of the degenerated 100V HEMT current sense, excluding 10 V and 100 V.

corner cases, making this amplification topology practically unusable. The limitation arises from the translation structure, particularly at the drains of M8 and M10. The voltages at these points are set by R4 and R6 to maximize the operating range, but even minor shifts in the values of these resistors, easily caused by process variations, lead to a further reduction in the circuit's functional range.

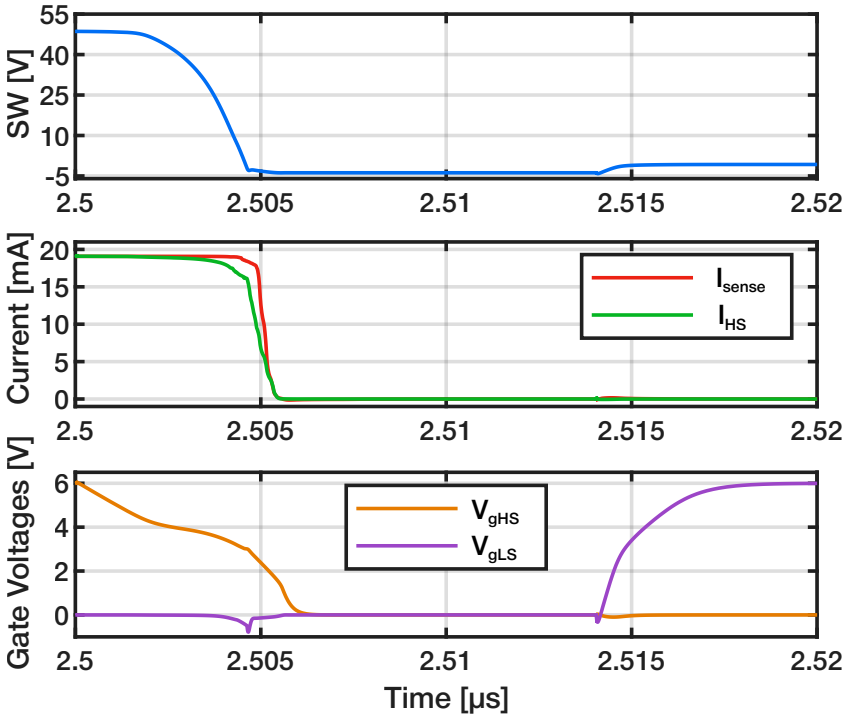

Figure 4.13: Zero-current detection of the degenerated 100V HEMT current sense in nominal condition.

4.2.3 Zero-current detection

The zero-current detection functionality of the circuit is shown in Fig. 4.13, where it can be observed that the sense current does not exactly follow the path of the scaled high-side power current depicted in the figure, but it reaches zero at the same time. Problems arise in the worst condition, as shown in Fig. 4.14, where the input voltage is at the maximum possible value, the load current is at a minimum, and the temperature is at its peak. This causes a slow descent of the switching node, leading the sense current to reach zero significantly later than the high-side current, rendering the circuit unusable for zero-current detection in these conditions. Additionally, Fig. 4.14 shows the condition under which the delay of the anti-cross-conduction circuit was designed. The two power gate voltages are never active simultaneously, and when the low-side power transistor turns on, the high-side power current has already reached zero.

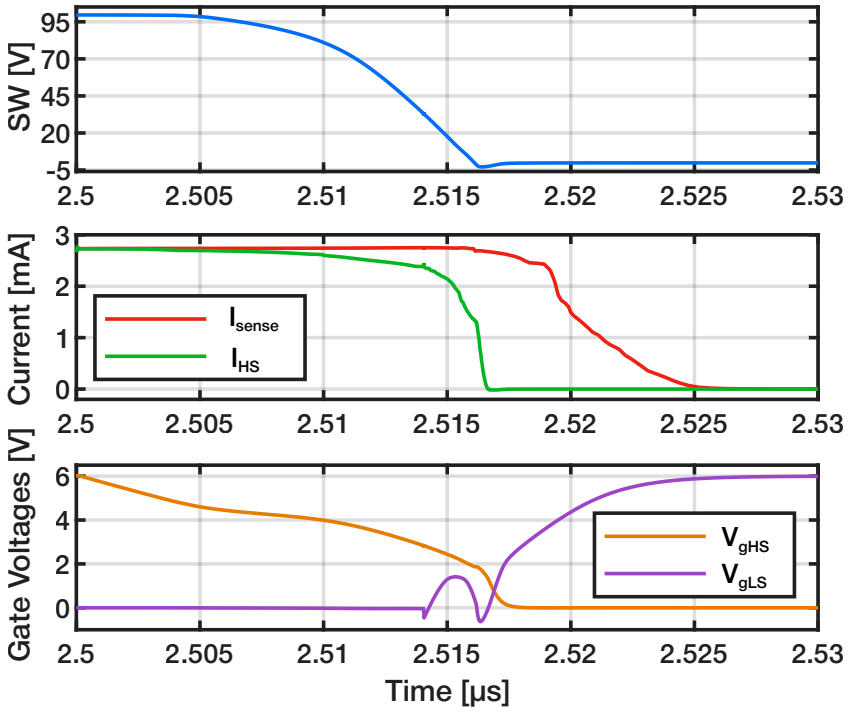

Figure 4.14: Zero-current detection of the degenerated 100V HEMT current sense in worst condition.

4.3 Single stage current sense

To address the issues of the previous implementation, a new translation and amplification topology was designed, as shown in Fig. 4.15. This design replaces the structure using a 100-V enhancement device and two resistors with a simple resistor, saving area and reducing attenuation. As in the first implementation, the source of the power HEMT (the switching node) and the source of the sense transistor are connected to the input differential pair composed of M1 and M2. This pair is directly biased by a 50 µA 100-V cascoded current generator, similar to the one described in Subsec. 3.1.4, consisting of M3, M4, and R3. The drains of the differential pair are connected to two resistors that set the drain voltage and minimize offset compared to an equivalent implementation using current generators. As in the previous design, these resistors are connected to a bootstrapped voltage from the switching node (realized with an ideal block) to provide sufficient headroom for the differential pair, allowing this single-stage amplifier to move up and down with the switching node. Unlike the previous structure, the outer branches are not biased by a fixed current; instead, the current varies with the input voltages of the differential pair, the bootstrap voltage, and thus with the switching node and the input voltage of the buck converter. The relationship between the current flowing through R4 and R5 and the input voltage of the buck converter is given in Eq. (4.7).

$$I_{R4} = \frac{V_{sM5} - V_{dM7}}{R_4} \tag{4.4}$$

$$I_{R4} = \frac{V_{boot} - (R_1 \cdot I_{dM1}) - V_{gsM5} - V_{gsM8}}{R_4} \tag{4.5}$$

$$I_{R4} = \frac{V_{sHS-PW} + V_{dc} - (R_1 \cdot \frac{I_{bias}}{2}) - V_{gsM5} - V_{gsM8}}{R_4} \tag{4.6}$$

$$I_{R4} = \frac{V_{in} - V_{dsHS-PW} + V_{dc} - (R_1 \cdot \frac{I_{bias}}{2}) - V_{gsM5} - V_{gsM8}}{R_4} \tag{4.7}$$

This dependency arises due to the absence of p-channel devices; if M5 and M6 were not n-channel devices, the current would be independent of the input voltage. The structure must be designed without additional current sources that are independent of this relationship to avoid introducing offsets. After translation, the current from the two outer branches is mirrored through two high-compliance current mirrors into two other branches connected by a high-side current mirror further enhancing the gain. To compensate the circuit, a small 0.8 pF MIM capacitor C1 and a 14 kΩ thin film resistor R6 are used. The output is taken from the drain of M11, and closes with M16, M15, and M17 at the source of the sense transistor. An

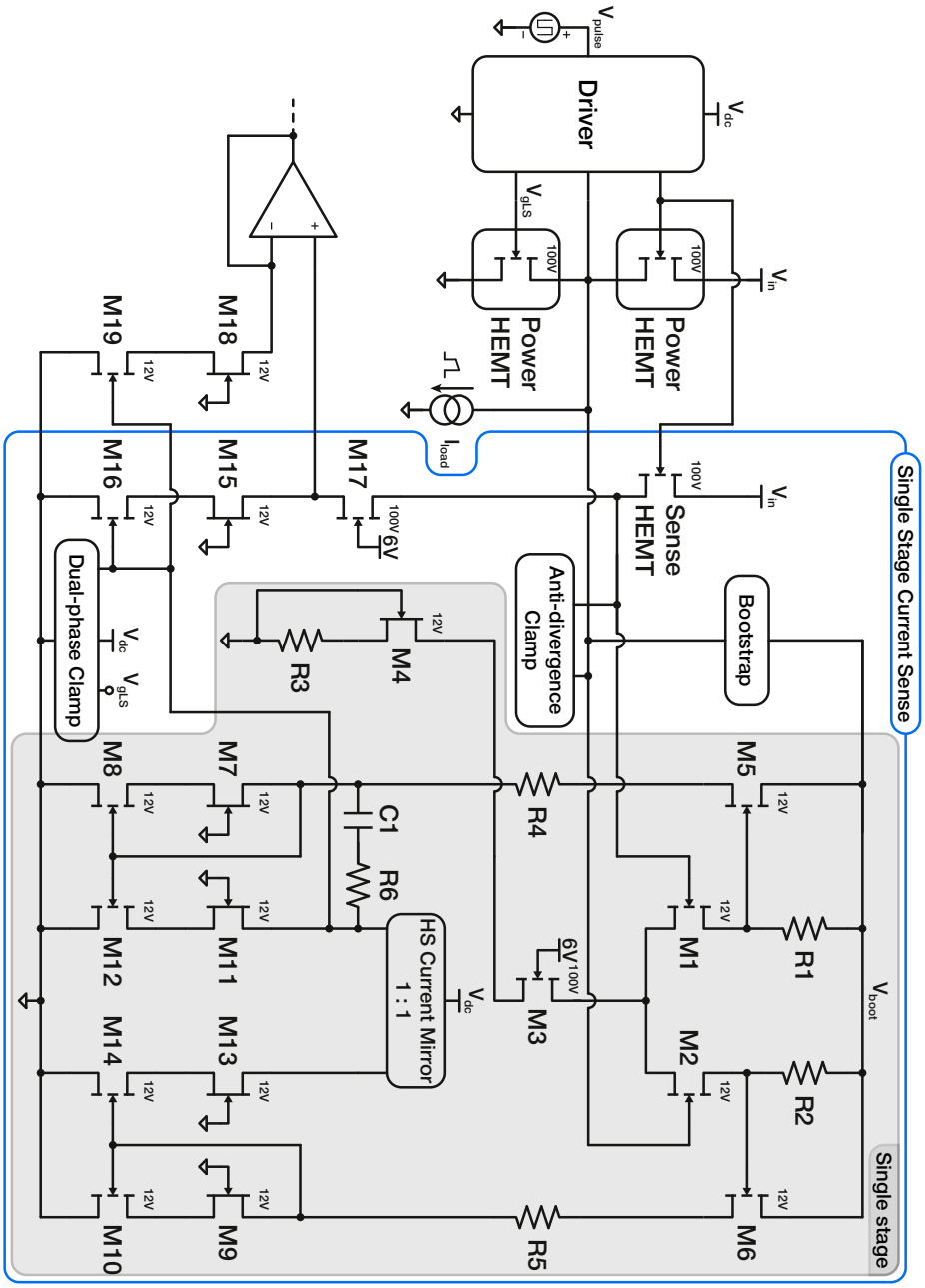

Figure 4.15: Schematic of the single stage current sense.

anti-divergence clamp is placed between the switching node and the node that follows it to limit the voltage difference between the two during switching, thereby enhancing circuit robustness. Additionally, a dual-phase clamp, driven by the gate voltage of the low-side power transistor, is used to prevent the gate voltage of M16 from dropping too low due to the action of the high-side current mirror. This improves the reaction time, particularly during startup, thereby enhancing the operating frequency range.
The sizing of R4 and R5, and consequently the current flowing through them, involves a trade-off between power consumption, area, matching offset, and operating range. If reducing power consumption is mandatory, larger resistors must be used; however, without adequate tuning of the rest of the circuit, this can lead to matching offsets and a reduced operating range. The sizes of all high-compliance current mirrors must be adjusted to account for the lower current in the circuit, scaling them according to the new current ratios. By ensuring that the smallest mirror uses at least two fingers, this approach minimizes matching offset. However, this smaller current can create issues with the operating range. The current generators within the high-side current mirror are pushed to their limits to maximize response time while maintaining a wide operating range (as discussed in Sec. 3.3). If the mirror factor between the outer branches and those connected to the high-side current mirror is set to one, reducing the current to lower power consumption requires scaling the current generators within the mirror. While this prevents a significant reduction in the operating range, it also slows the circuit's response time, thus limiting the frequency range at which it can operate. To address these issues, a different mirror factor can be employed, but the challenge of a high ratio between the lowest and highest current persists, which impacts the area. If current consumption is not a stringent requirement, the resistors can be made smaller to increase the current in the outer branches. The mirror factor can then be increased to boost the current in the branches of the high-side current mirror. This allows the internal current generator to be designed for higher current, which enhances the circuit's response time and reduces the total area by lowering the current ratio between the highest and lowest currents in the circuit.
The final design employs a mirror factor of 1 and a current ratio of 60, providing a balanced solution to the trade-offs discussed.

4.3.1 Frequency response

In Fig. 4.16, the loop gain and phase noise of this new amplification topology are presented. The first noticeable point is that the gain is over 37 dB lower compared to the previous structure, yet it achieves superior performance. Additionally, while the bandwidth is lower, it demonstrates greater stability across temperature variations, as shown in Tab. 4.8. The phase margin is significantly higher, compensating for other challenging operating

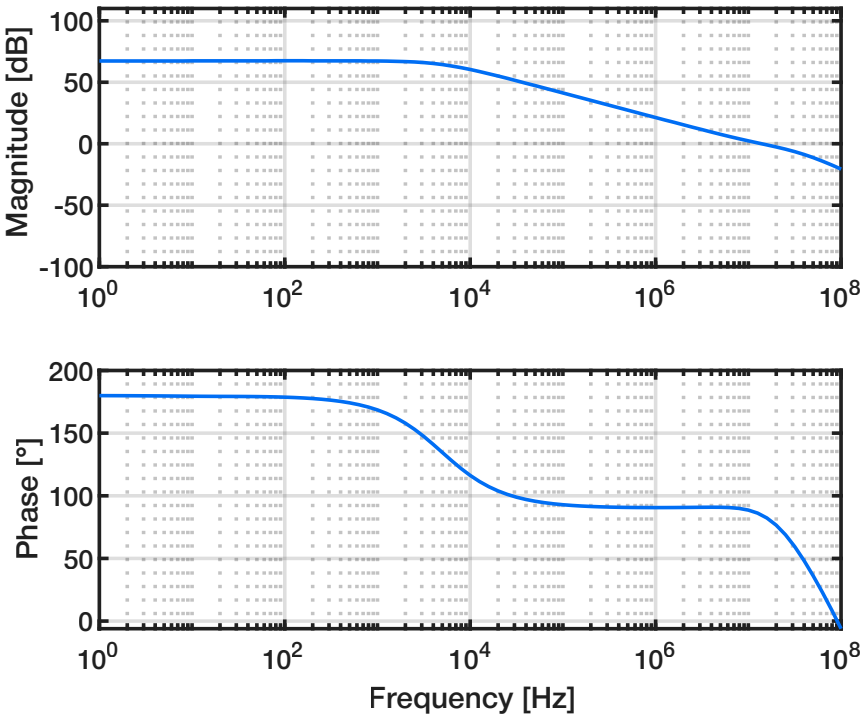

Figure 4.16: Loop gain and phase of the single stage current sense.

conditions.

4.3.2 Ripple following

The sense current is depicted in Fig. 4.17, illustrating that with two fewer stages, the circuit performs even better. As shown in Tab. 4.9, the current offset improves across all temperatures, while the response time only worsens at -40°C. Regarding the operating range for different input voltages, as detailed in Tab. 4.10, the circuit performs well across the entire voltage span, maintaining a relatively stable current offset and very stable response

Temperature	Loop Gain	Bandwidth	Phase Margin
-40°C	61.6 dB	10 MHz	95.4°
27°C	67.5 dB	14 MHz	84.5°
150°C	57 dB	14.7 MHz	58.2°

Table 4.8: Loop gain, bandwidth and phase margin of the single stage current sense.

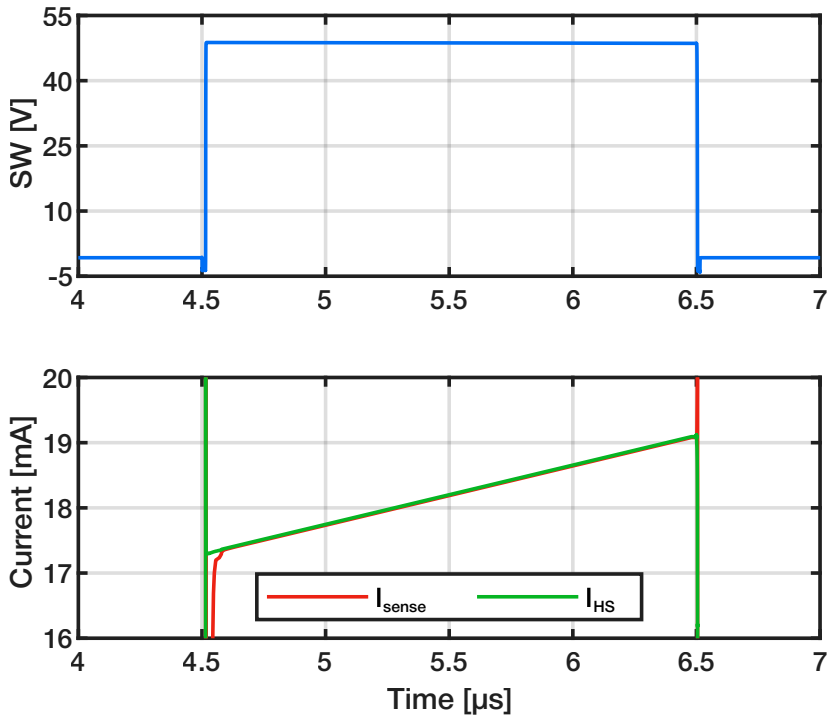

Figure 4.17: Ripple following of the single stage current sense in nominal condition.

time. Although the performance deteriorates with lower load currents, it is less severe than with the previous circuit, and the response time is longer, as shown in Tab. 4.11. This increase in response time can be misleading if not properly considered. The previous circuit consumed more current than this topology, so, given the trade-offs discussed earlier, increasing the current consumption could potentially enhance performance without issues. Fig. 4.18 shows that, despite very good performance at low frequencies, at higher frequencies the response time deteriorates due to the circuit's low bandwidth. However, it maintains a good current offset once the transient phase has concluded.
In Tab. 4.12, a comparison of the nominal and worst conditions is presented, including input voltages of 10 V and 100 V, it reveals a substantial improvement over the previous design.

4.3.3 Zero-current detection

The zero-current detection, shown in Fig. 4.19, illustrates that the sense current reaches zero, and even turns negative, before the high-side current

Temperature	Current Offset	Response Time
-40°C	18.3 µA	310 ns
27°C	13.4 µA	125 ns
150°C	25.1 µA	220 ns

Table 4.9: Current offset and response time at three temperatures of the single stage current sense.

Input Voltage	Current Offset	Response Time
10 V	2 µA	135 ns
30 V	7.6 µA	120 ns
50 V	13.4 µA	125 ns
70 V	25.8 µA	115 ns
100 V	33.1 µA	125 ns

Table 4.10: Current offset and response time at five input voltages of the single stage current sense.

Load Current	Current Offset	Response Time
1 A	39 µA	335 ns
5 A	18.3 µA	335 ns
10 A	13.4 µA	125 ns

Table 4.11: Current offset and response time at three load currents of the single stage current sense.

	Current Offset	Response Time
Nominal	13.4 µA	125 ns
Worst	85.6 µA	390 ns

Table 4.12: Current offset and response time in the nominal and worst case of the single stage current sense.

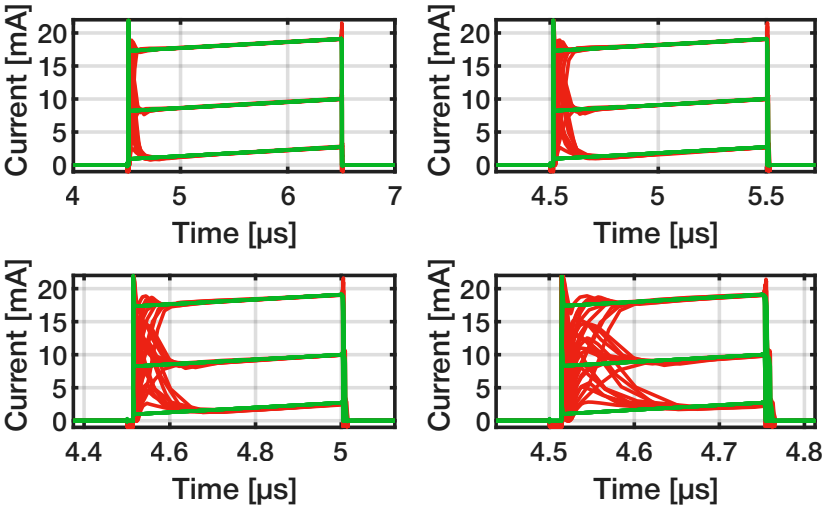

Figure 4.18: Ripple following of the single stage current sense at four different frequencies: 250 kHz, 500 kHz, 1 MHz and 2 MHz with 50% duty cycle. Each figure shows the sense current at temperatures in the range [-40°C ÷ 150°C], input voltages in the range [30 V ÷ 70 V] and load currents in the range [1 A ÷ 10 A].

goes to zero. This behavior occurs because the sense current ceases as the switching node turns off the three transistors stacked below the sense HEMT by the drain. A small delay could be added to correct this, without significantly affecting the circuit's performance. However, as shown in Fig. 4.20, in the worst-case condition, the sense current reaches zero after the high-side power current, though it performs better compared to the previous circuit.

4.4 Two stage current sense

To reduce offsets, a new version of the previous circuit, shown in Fig. 4.21, has been designed with a second amplification stage, utilizing the same signal translation technique. The initial section, up to the translation, is equal to the circuit described in the previous section. However, after translation, a single-ended conversion is performed, where one branch is diode-connected and the output of the first stage is taken from the other branch. The second stage consists of M14 and M13, biased by a current replicated from the first stage. This approach, as explained in the previous section and shown in Eq. (4.7), is necessary because the current in this branch must depend on the input voltage of the buck converter to avoid offset. Simply placing a 100-

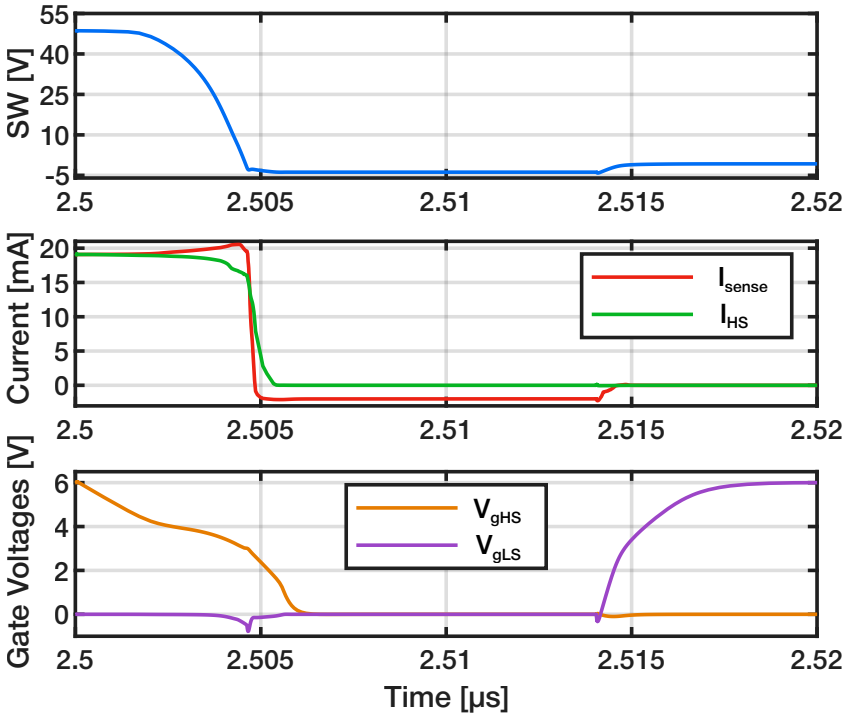

Figure 4.19: Zero-current detection of the single stage current sense in nominal condition.

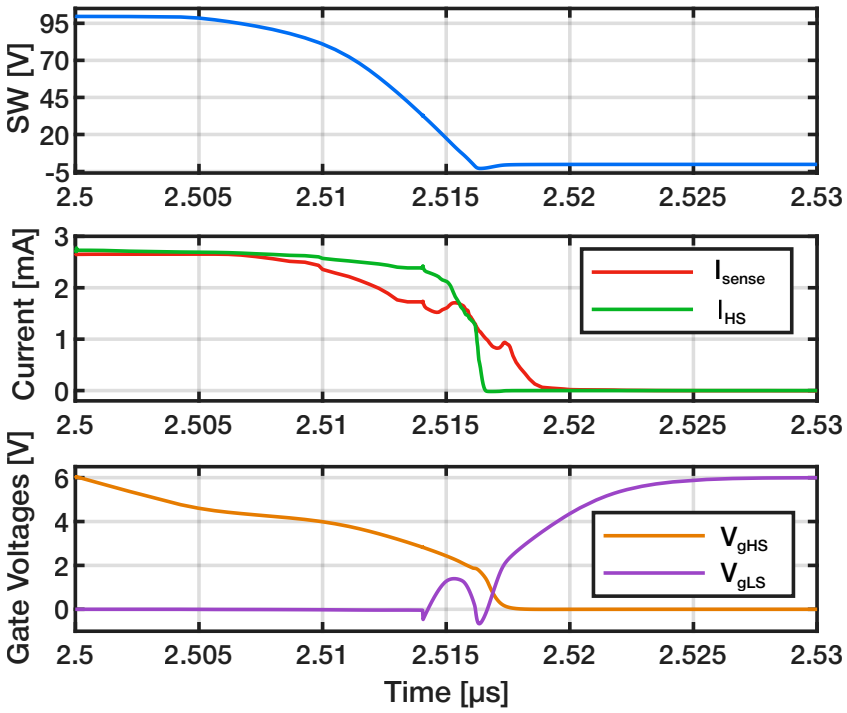

Figure 4.20: Zero-current detection of the single stage current sense in worst condition.

V current generator over this stage, connected to the input voltage, would have been insufficient, as the relationship between current and input voltage would differ significantly from that of the first stage, or potentially not exist at all, due to the extremely high output impedance of the current generator. This mismatch would create offsets caused by discrepancies in the sizing and current of the different branches, making it essential to add another branch to replicate the current from the first stage. The output of the amplifier is taken at the drain of M13, and the structure is closed on the source of the sense transistor using M16, M15, and M17. The current is extracted by a high-compliance current mirror branch, composed of M19 and M18, with its drain in virtual short-circuit with the drain of M15, thanks to a buffer that, with a control loop, connects to the driver's input. The anti-divergence clamp and dual-phase clamp are also included, connected in the same manner as in the previous circuit, for the same reasons. The two-stage amplifier is compensated by a 3.1 pF MIM capacitor C1 and a 9 kΩ thin film resistor R6 connected between the output of the two stages.

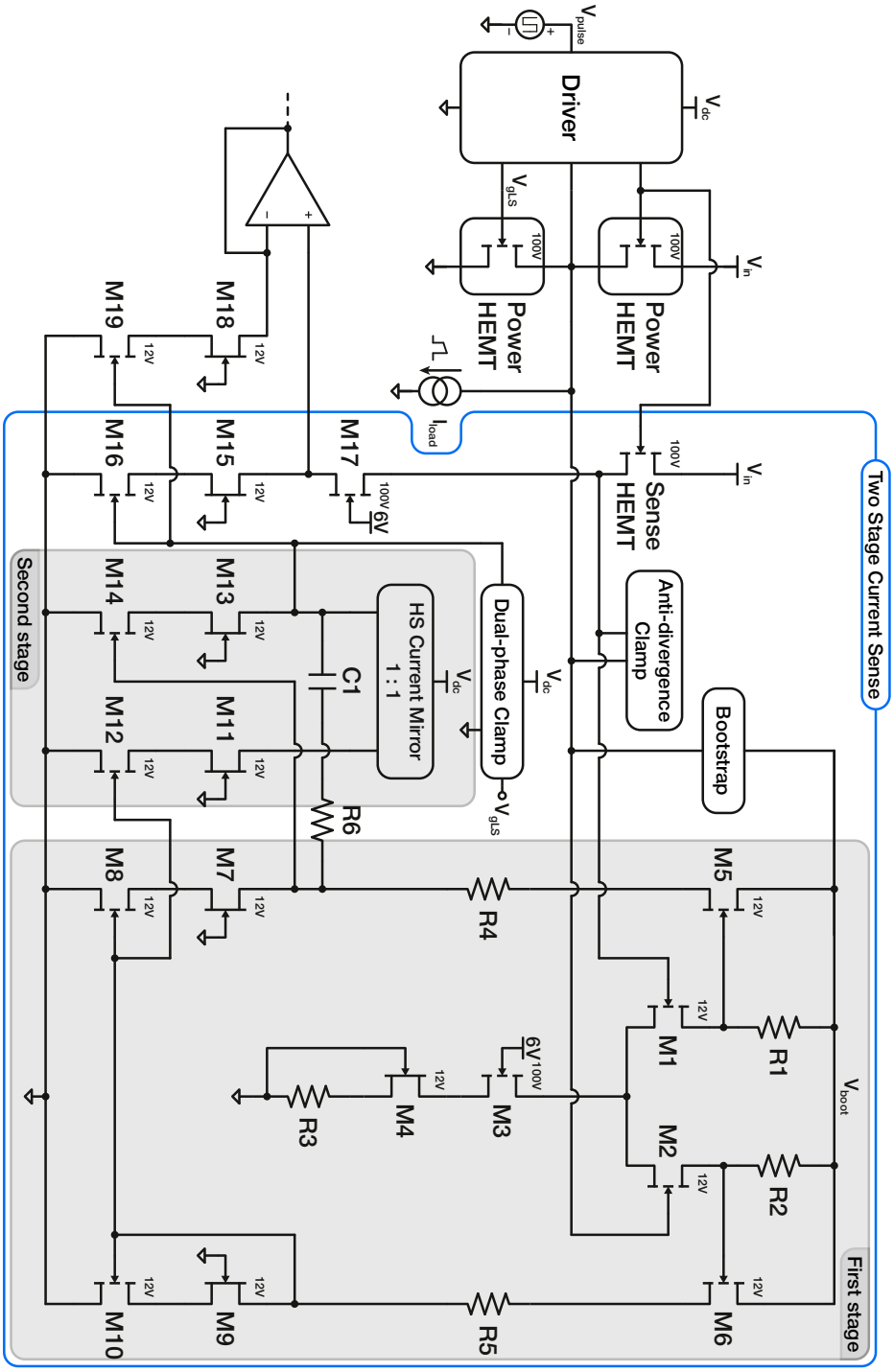

Figure 4.21: Schematic of the two stage current sense.

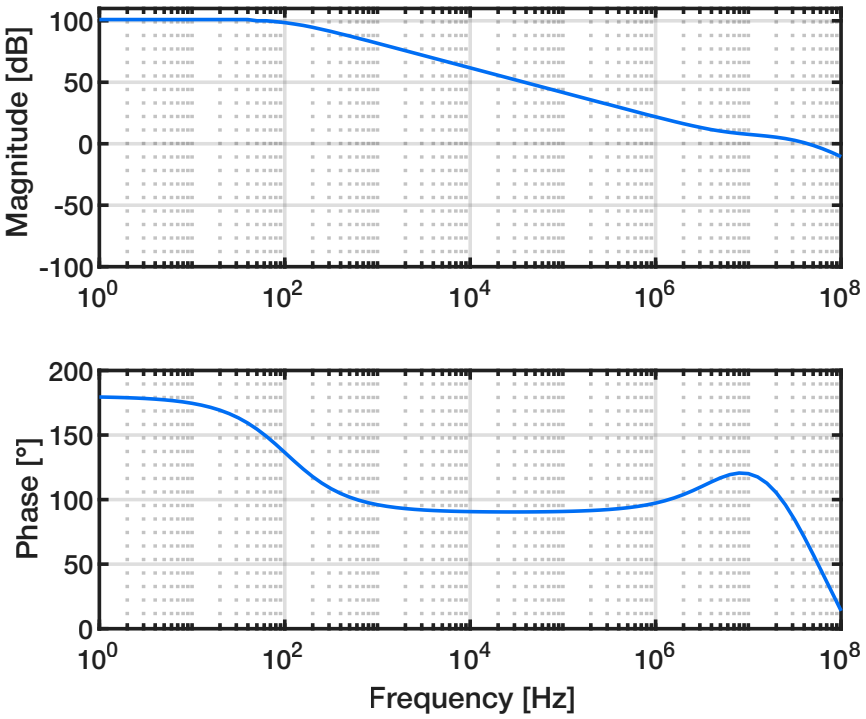

Figure 4.22: Loop gain and phase of the two stage current sense.

4.4.1 Frequency response

As shown in Fig. 4.22 and Tab. 4.13, with the two-stage design, the loop gain has increased to values similar to those of the three-stage topology of the degenerated 100-V current sense, although the stability over temperature is reduced. The bandwidth has also increased, while the phase margin is tuned differently compared to the previous design.

Temperature	Loop Gain	Bandwidth	Phase Margin
-40°C	98.6 dB	50.7 MHz	84.8°
27°C	101.3 dB	43.9 MHz	65.8°
150°C	84.6 dB	23.6 MHz	50.6°

Table 4.13: Loop gain, bandwidth and phase margin of the two stage current sense.

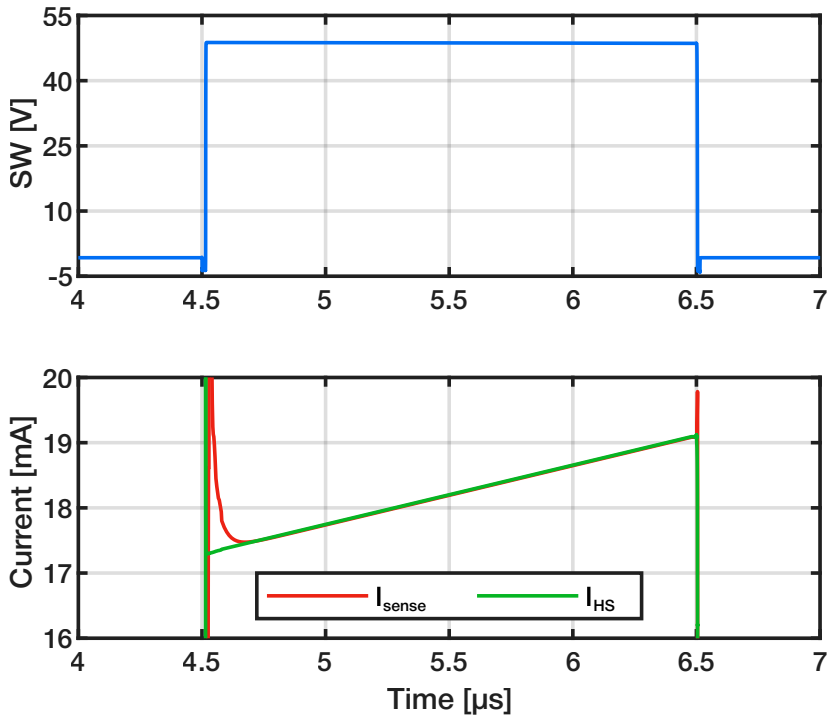

Figure 4.23: Ripple following of the two stage current sense in nominal condition.

4.4.2 Ripple following

With the addition of this second stage, the current offset has been reduced to just 7.9 µA, more than halving the offset of the initial circuit with one less stage. Fig. 4.23 illustrates the circuit's behavior, while Tab. 4.15 shows that the current offset is now very stable over temperature, with only a slight increase in response time at ambient temperature. Regarding input voltage variation, as shown in Tab. 4.15, the current offsets are generally lower, although they are higher in certain conditions compared to the previous circuit. As with the other two circuits, the current offset and response time increase at lower load currents, but the average values are lower for both metrics with this circuit. Fig. 4.24 illustrates the advantages of the higher bandwidth of this circuit, which is now capable of operating at higher frequencies. This improvement allows for faster response times and better performance, particularly in high-frequency applications, compared to previous designs.
This circuit has a worse worst-case performance compared to the previous one, as shown in Tab. 4.17, but, as mentioned earlier, the average perfor-

Temperature	Current Offset	Response Time
-40°C	9.3 µA	155 ns
27°C	7.9 µA	145 ns
150°C	8.9 µA	175 ns

Table 4.14: Current offset and response time at three temperatures of the two stage current sense.

Input Voltage	Current Offset	Response Time
10 V	19 µA	195 ns
30 V	11.9 µA	145 ns
50 V	7.9 µA	145 ns
70 V	6 µA	155 ns
100 V	5 µA	155 ns

Table 4.15: Current offset and response time at five input voltages of the two stage current sense.

Load Current	Current Offset	Response Time
1 A	42.6 µA	265 ns
5 A	12.8 µA	170 ns
10 A	7.9 µA	145 ns

Table 4.16: Current offset and response time at three load currents of the two stage current sense.

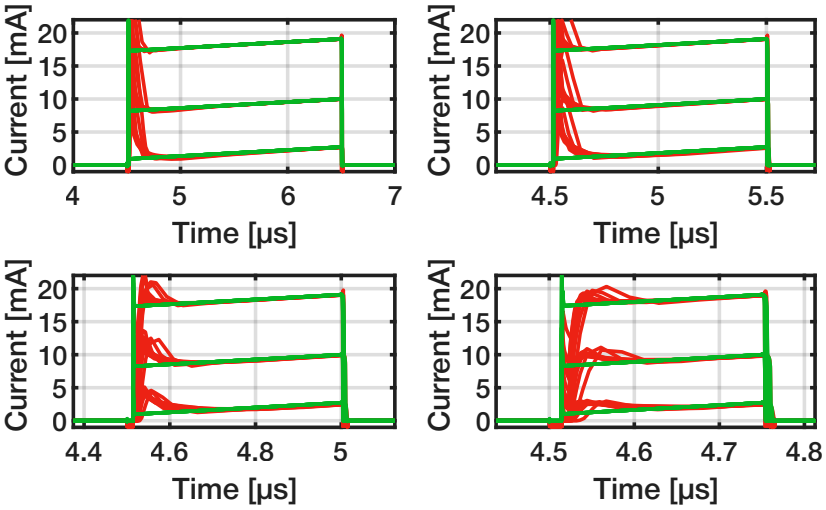

Figure 4.24: Ripple following of the two stage current sense at four different frequencies: 250 kHz, 500 kHz, 1 MHz and 2 MHz with 50% duty cycle. Each figure shows the sense current at temperatures in the range [-40°C ÷ 150°C], input voltages in the range [30 V ÷ 70 V] and load currents in the range [1 A ÷ 10 A].

	Current Offset	**Response Time**
Nominal	7.9 µA	145 ns
Worst	104.9 µA	525 ns

Table 4.17: Current offset and response time in the nominal and worst case of the two stage current sense.

mance is improved.

4.4.3 Zero-current detection

The performance of this circuit regarding zero-current detection is comparable to the previous one under nominal conditions, as shown in Fig. 4.25. However, due to its higher gain and bandwidth, in worst-case conditions, the sense current reaches zero approximately at the same point as the high-side current, as illustrated in Fig. 4.26, leading to improved overall performance.

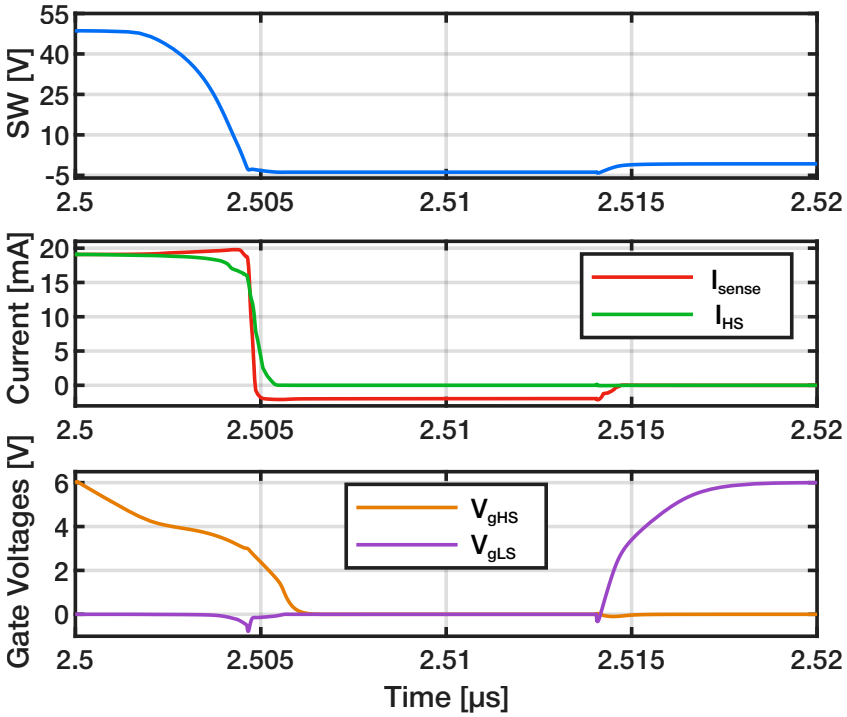

Figure 4.25: Zero-current detection of the two stage current sense in nominal condition.

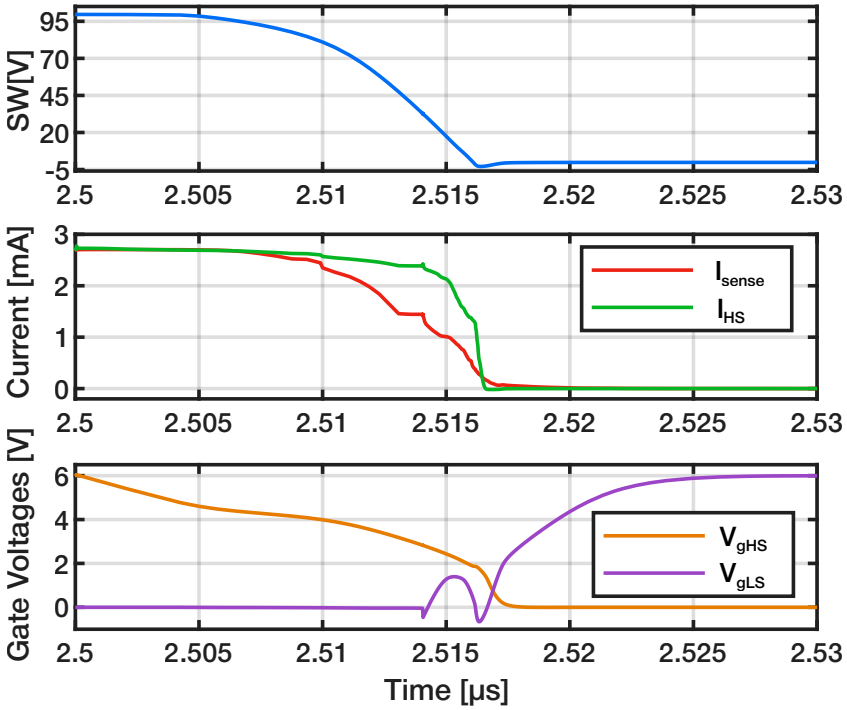

Figure 4.26: Zero-current detection of the two stage current sense in worst condition.

Conclusions

In Tab. 4.18, the three solutions are compared across various aspects such as current consumption, area occupation, operating range, and others, which are defined as follows:

- current consumption: the total sum of currents flowing through the branches of the amplifier, excluding both the sense current and the current mirrored outside the current sense loop[1];
- area utilization: the sum of the $W \cdot L$ of all components, excluding only the branch that mirrors the current outside the control loop[2];
- operating range: the range of input voltages within which the circuit operates without issues.

The current consumption of the first solution is higher than that of the other two circuits, but it remains stable across input voltage variations, whereas the current consumption of the other two circuits fluctuates, resulting in higher current consumption in some cases. The area occupation increases with the number of stages, particularly due to the compensation capacitance, resulting in a smaller area for the single-stage current sense. The operating range is a key comparison parameter, and as shown in Tab. 4.18, the first solution, which utilizes the degenerated 100-V HEMT for information translation, has limitations related to this choice. The loop gain of the first and third solutions is higher than that of the single-stage current sense due to the increased number of stages. However, despite having an extra stage, the degenerated 100-V HEMT current sense offers a similar gain to the two-stage current sense because of the high attenuation in the translation structure. The third solution has the highest bandwidth and can operate at higher frequencies, as illustrated in the figures from the previous chapter. In nominal conditions, the two-stage current sense has the best current

[1]The sense current is excluded from comparison as it is common to all proposed solutions, while the externally mirrored current is excluded because it pertains to the control loop design rather than the current sensing itself.

[2]The branch of the current mirrored outside is excluded because it is related to the design of the control loop, not the current sensing itself.

	Deg. 100-V HEMT	Single stage	Two stage
I consumpt.	1.7 mA	1.2 mA	1.2 mA
Area occup.	0.077 mm^2	0.014 mm^2	0.024 mm^2
Operat. range	30 ÷ 70 V	10 ÷ 100 V	10 ÷ 100 V
Compens. C	8.5 pF	0.8 pF	3.1 pF
Compens. R	2 kΩ	14 kΩ	9 kΩ
Loop Gain	101.7 dB	67.5 dB	101.3 dB
Bandwidth	17.3 MHz	14 MHz	43.9 MHz
Phase Margin	66°	84.5°	65.8°
Offset nom	17.1 µA	13.4 µA	7.9 µA
Offset max	450 µA	85.6 µA	104.9 µA
Resp. T nom	165 ns	125 ns	145 ns
Resp. T max	1500 ns	390 ns	525 ns
Zero-current	Worst	Good	Best

Table 4.18: Comparison table of the three solutions.

offset, but in worst-case scenarios, the single-stage current sense performs better. Nonetheless, across different conditions, the third structure generally maintains lower offsets compared to the other two. The first solution's response time is less reliable outside nominal conditions, whereas the other two are comparable. Although the two-stage current sense shows higher response times in some worst-case scenarios, it generally delivers better average performance, with peaks in only two analyzed conditions, while the single-stage solution exhibits higher response times more frequently. Regarding zero-current detection, the first circuit becomes unusable when the load current decreases, while the second circuit performs well. However, the third solution delivers near-perfect performance in this respect.
In conclusion, the two-stage current sense emerges as the optimal choice among the proposed topologies, whereas the degenerated 100-V HEMT solution ranks the lowest in most of the analyzed parameters.
The next steps involve designing the essential blocks, such as the bootstrap, buffer, control loop, and driver components, to prepare for tape-out and subsequent circuit measurement.

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