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Design of a PMOS Capless Flipped-Voltage-Follower LDO in FinFET Technology

Supervisors:

Prof. Edoardo Bonizzoni

Prof. Piero Malcovati

Co-supervisor:

Dott. Antonio Aprile

Company supervisors:

Darshan Shetty

Michael Simone Marioli

Sofia Luddi

Infineon Technologies AG

Master thesis of:

Giacomo Chiesa

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Abstract

This thesis presents the design of a fully integrated PMOS capless low-dropout regulator (LDO) based on the Flipped Voltage Follower (FVF) scheme in a 12-nm FinFET technology. This work aims to develop a high-bandwidth regulator able to operate without an external output capacitor while meeting demanding static and dynamic specifications: overall output accuracy below 10% and maximum load-transient overshoot and undershoot below 8%.

The work starts from an analysis of LDO fundamentals and performance metrics, including dropout voltage, quiescent current, load and line regulation, output impedance, power-supply rejection, stability, and transient response. Different integrated LDO architectures are then compared in order to identify the most suitable solution for the required specifications. The analysis motivates the choice of a PMOS capless FVF-based architecture, where local fast feedback is used to reduce the output impedance and improve the transient behavior with limited output capacitance.

The proposed regulator is designed and validated through transistor-level simulations. The verification includes DC accuracy, frequency response, loop stability, and load-transient performance, with particular attention to the specified accuracy and over/undershoot limits.

Sommario

Questa tesi presenta il progetto di un regolatore low-dropout (LDO) PMOS capless completamente integrato basato sullo schema Flipped Voltage Follower (FVF), in tecnologia FinFET a 12 nm. Il lavoro mira a sviluppare un regolatore ad alta banda, capace di funzionare senza condensatore esterno di uscita e di soddisfare specifiche statiche e dinamiche stringenti: precisione complessiva della tensione di uscita inferiore al 10% e massimo overshoot/undershoot nei transitori di carico inferiore all'8%.

Il lavoro parte dall'analisi dei fondamenti degli LDO e dei principali parametri di prestazione, tra cui tensione di dropout, corrente quiescente, regolazione di linea e di carico, impedenza di uscita, reiezione dei disturbi di alimentazione, stabilità e risposta ai transitori. Diverse architetture LDO integrate vengono quindi confrontate per individuare la soluzione più adatta al raggiungimento delle specifiche richieste. L'analisi motiva la scelta di un'architettura PMOS capless basata su FVF, in cui una retroazione locale veloce viene utilizzata per ridurre l'impedenza di uscita e migliorare la risposta dinamica in presenza di capacità di uscita limitata.

Il regolatore proposto viene progettato e validato mediante simulazioni a livello transistor. La verifica include accuratezza in continua, risposta in frequenza, stabilità e risposta ai transitori di carico, con particolare attenzione ai limiti specificati di precisione e di over/undershoot.

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List of Acronyms

AC	Alternating Current
CMOS	Complementary Metal-Oxide-Semiconductor
DC	Direct Current
EA	Error Amplifier
ESR	Equivalent Series Resistance
FVF	Flipped Voltage Follower
IC	Integrated Circuit
IQ	Quiescent Current
LDO	Low-Dropout Regulator
LHP	Left-Half Plane
LNA	Low-Noise Amplifier
MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
MOS	Metal-Oxide-Semiconductor
NMOS	N-channel Metal-Oxide-Semiconductor
PMIC	Power Management Integrated Circuit
PMOS	P-channel Metal-Oxide-Semiconductor
PSR	Power Supply Rejection
PSRR	Power Supply Rejection Ratio

PVT	Process, Voltage, and Temperature
RF	Radio Frequency
RHP	Right-Half Plane
SoC	System-on-Chip
UGB	Unity-Gain Bandwidth
UGF	Unity-Gain Frequency

Chapter 1

Introduction

The increasing complexity of modern integrated systems has made power management a central topic in analog and mixed-signal circuit design. In a System-on-Chip (SoC), digital logic, analog interfaces, memories, sensors, and radio-frequency blocks often coexist on the same silicon platform, while requiring supply rails with different voltage levels, noise limits, transient requirements, and efficiency targets. The voltage available at chip or block level is never ideal: it can be affected by switching ripple, package parasitics, IR drops, substrate coupling, and abrupt load-current variations generated by the powered circuitry itself. If these disturbances are not properly attenuated, they can directly degrade gain accuracy, noise, jitter, phase noise, linearity, or timing margins.

Voltage regulators are therefore used to generate and distribute controlled supply voltages across the system. Among the available solutions, low-dropout regulators (LDOs) are widely adopted as local post-regulators because they operate in the linear domain, do not introduce switching ripple, and can provide clean supply rails to noise-sensitive analog and RF blocks. A conventional LDO can be seen as a feedback-controlled buffered reference: an error amplifier senses the output through a feedback network and drives a power transistor so as to regulate the output current and the equivalent output resistance, as shown in Fig. 1.1.

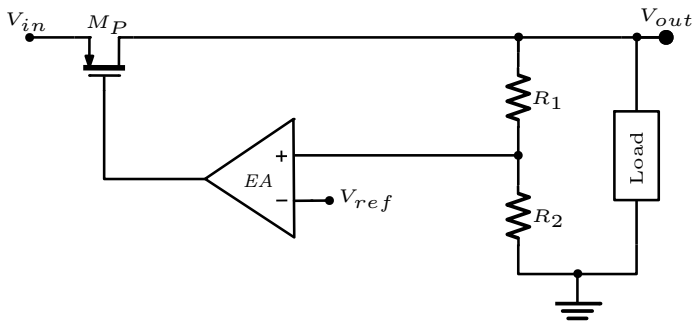


Figure 1.1: Basic LDO regulator.

This simple principle, however, leads to a design problem involving several interdependent specifications, including dropout voltage, headroom voltage, quiescent current, current efficiency, DC accuracy, load regulation, line regulation, output noise, power-supply rejection ratio (PSRR), loop stability, and transient response.

Depending on the application, local supply voltages may range from below 1 V to a few volts, while load currents may extend from the microampere range to hundreds of milliamperes.

The role of the output capacitor is especially important in this trade-off. In traditional LDOs, an off-chip capacitor in the microfarad range helps stabilize the loop and supplies or absorbs charge during load transients. This approach is effective, but it increases board area and cost, requires external pins, and limits the possibility of placing many independent local regulators close to their loads. Fully integrated LDOs, also referred to as on-chip, capacitor-less, or capless LDOs, address this limitation by avoiding a large external output capacitor and relying instead on integrated capacitance, package capacitance, and the parasitic capacitance of the load, resulting in a total capacitance typically in the picofarad to nanofarad range. A practical capless regulator should not be interpreted as operating with zero output capacitance, but rather as a regulator able to satisfy load-transient and stability requirements without an additional external capacitor over a specified output-capacitance range.

Removing the external capacitor shifts much of the burden from passive energy storage to the control architecture. Since only a small capacitance is available at the output node, the regulator must react quickly to load-current steps and must keep the output impedance low over the frequency range of interest. At the same time, increasing the loop bandwidth doesn't come for free: the large pass device introduces gate capacitance, the output pole moves with load current and output capacitance, and additional internal poles may threaten phase margin. Moreover, high power-supply rejection requires both a favorable open-loop ripple path and sufficient loop gain over frequency. These constraints make the design of fully integrated LDOs a multi-objective problem in which dynamic performance, PSRR, stability, silicon area, and quiescent current must be balanced from the beginning of the architecture selection.

This thesis focuses on the analysis and design of a PMOS capless LDO based on the Flipped Voltage Follower (FVF) concept. The design target is not only to implement a regulator, but to select a suitable architecture after comparing the main alternatives available for fully integrated LDOs. The FVF topology is attractive in this context because it provides a local feedback mechanism capable of driving the pass device rapidly and lowering the small-signal output resistance, which is crucial when the output capacitor is small. Depending on the final stability and accuracy requirements,

this local fast regulation can be combined with a slower high-gain path, but the thesis first motivates this choice through a comparison with other possible LDO architectures.

The choice of a PMOS pass transistor determines both advantages and design constraints. Compared with an NMOS pass device, a PMOS transistor can realize low-dropout operation without requiring a gate voltage higher than the input supply, making it well suited for compact integrated implementations. On the other hand, PMOS LDOs require careful treatment of the gate-drive path, supply-ripple coupling, loop compensation, and PSRR. In a high-bandwidth capless regulator, these aspects become tightly connected: the same fast path that improves transient response may also affect stability and the way supply disturbances are transferred to the output. The goal of this work is therefore to analyze these trade-offs and develop a PMOS capless FVF LDO architecture able to combine full integration, robust stability, accurate regulation, and fast transient behavior.

1.1 Context

In modern SoCs, power delivery is not merely a matter of providing energy to the load; it is part of the signal integrity problem of the whole system. A noisy or weak supply rail can couple directly into sensitive circuit quantities, while the current transient of one block can disturb neighboring modules through shared supply paths, package inductances, and finite impedance of the power distribution network. Local fully integrated LDOs mitigate these effects by placing the regulator closer to the load, reducing voltage drops along the supply path and isolating different power domains without requiring a large number of off-chip components.

This approach is particularly relevant for analog and RF blocks, which often require clean local supplies and can exhibit strongly time-varying current profiles. The regulator must reject low-frequency and high-frequency disturbances from the input supply, maintain the desired DC operating point, and respond to load steps with limited undershoot, overshoot, and recovery time. The relevant design metrics cannot be optimized independently: reducing quiescent current may limit slew rate and bandwidth, increasing bandwidth may complicate compensation, and improving PSRR may require specific gate-drive or ripple-cancellation techniques.

For capless LDOs, the absence of a large external capacitor makes the architecture of the control loop even more important. The load capacitance and the pass-device parasitics define poles that vary with operating conditions, while the power transistor gate can become difficult to drive at high speed. For this reason, the architectural

comparison must explicitly consider how each solution handles bandwidth, output impedance, compensation, static precision, and transient over/undershoot.

1.2 Thesis Organization

The thesis is organized as follows. Chapter 2 introduces voltage regulators and the LDO specifications needed to understand the design problem. Chapter 3 presents the architecture analysis, starting from the state of the art and from single-loop PMOS LDO limitations, then motivating the dual-loop FVF solution adopted in this work. Chapter 4 develops the circuit design of the selected FVF LDO, analyzing the folded error amplifier, slow loop, fast loop, compensation strategy, and loading non-idealities. Chapter 5 reports the simulation results, including testbenches, DC performance, frequency-domain behavior and stability, time-domain performance, and comparison with the state of the art. Finally, Chapter 6 summarizes the conclusions and discusses possible future developments.

Chapter 2

Voltage Regulators

Voltage regulators generate controlled supply voltages from an available input rail and are essential whenever the load requires a cleaner or more accurate supply than the one provided by the main power distribution network. In integrated systems, this task is particularly relevant because different blocks can have different noise, current, transient, and voltage requirements. In recent years, voltage regulators have become increasingly important in System-on-Chip (SoC) platforms, where many digital, analog, memory, RF, and mixed-signal blocks coexist on the same die and require independent local supply domains. Technology scaling, lower supply voltages, aggressive dynamic power management, and fast load-current variations make the supply network a critical part of the system design rather than a secondary support circuit.

In many power-management systems, the supply rails are generated by a Power Management Integrated Circuit (PMIC). As shown in Fig. 2.1, an LDO is often placed as the final regulation stage of the PMIC chain, after a previous conversion stage, in order to provide a clean and accurately regulated output voltage to the load. This is especially useful when the powered block is sensitive to supply ripple, noise, or fast current variations.

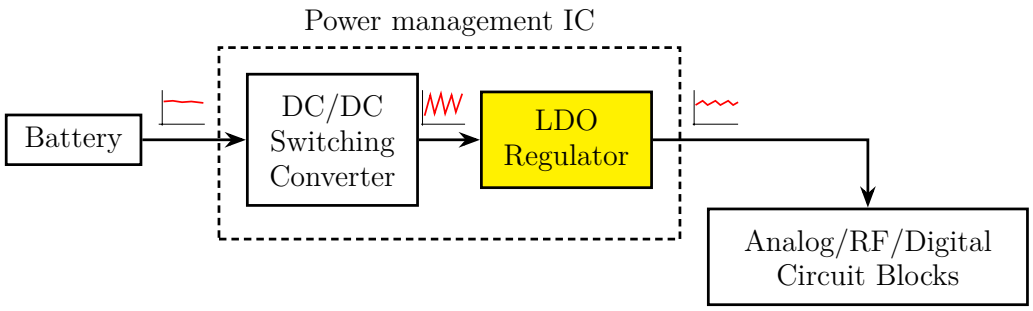


Figure 2.1: Example of an LDO used as the final clean-output stage of a PMIC chain.

When a large voltage step is required, a DC–DC converter is typically used first because its switching operation provides higher conversion efficiency, while the LDO performs the final, smaller voltage drop and provides a clean supply rail. Using an LDO for the entire conversion would lead to significant power dissipation, since the loss is proportional to the input-output voltage difference, $V_{\text{in}} - V_{\text{out}}$, and the load current, I_{out}. Different converter implementations are used inside or around this power chain. Switching converters are preferred when high efficiency and large voltage conversion ratios are required, while charge pumps are useful for inductorless integrated conversion. Linear regulators are instead adopted when low ripple, simple filtering, and accurate local regulation are more important than maximum conversion efficiency. Within this last family, low-dropout regulators (LDOs) are widely used as local post-regulators because they can operate with a small input-output voltage difference and can be placed close to noise-sensitive analog, RF, or mixed-signal loads.

An LDO can be viewed as a feedback-regulated buffered reference, as shown in Fig. 2.2. A voltage reference defines the desired operating point, an error amplifier or control network compares the output with this reference, and a pass device modulates the current delivered to the load. The regulator therefore behaves as a controlled resistance between the input and output rails. When the load current or the input voltage changes, the feedback loop adjusts the pass-device gate or control node so that the output voltage remains close to its nominal value.

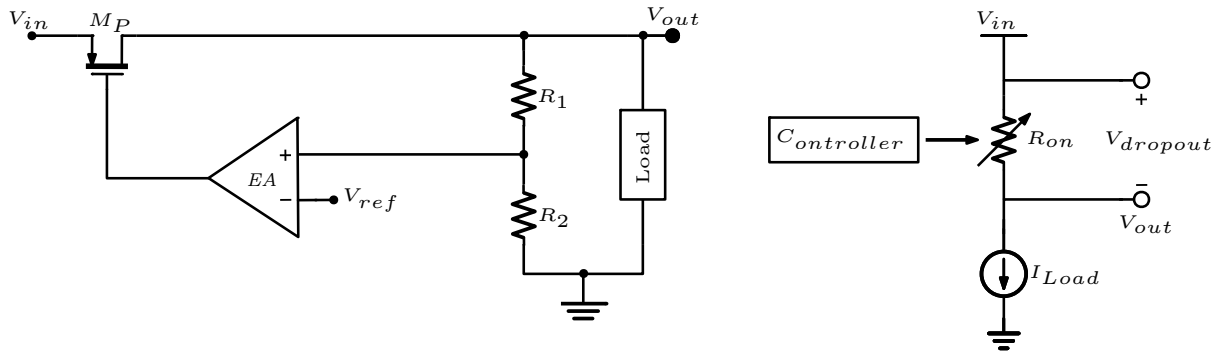


Figure 2.2: Simplified LDO architecture and operating regions.

In this context, fully integrated does not mean that the output node has zero capacitance. Instead, it means that the regulator is designed to satisfy stability and transient requirements without a large off-chip capacitor, relying only on on-chip capacitance, package capacitance, and the parasitic or local decoupling capacitance of the load. This distinction is central to this thesis: once the external capacitor is removed, the design burden shifts from passive charge storage to loop bandwidth, output impedance, pass-device driving capability, and compensation strategy.

Fully integrated LDOs are commonly grouped into three broad categories: analog LDOs, digital LDOs, and hybrid LDOs. Analog LDOs rely on continuous-time feedback and an analog pass-device drive; digital LDOs use sampled or event-driven control with discrete pass devices; hybrid LDOs combine analog and digital regulation paths. Among these topologies, this thesis focuses on the analog LDO case.

The performance of an LDO cannot be described by a single number. Static quantities define the DC operating range and accuracy, while dynamic quantities describe the ability of the regulator to reject disturbances, remain stable, and recover from abrupt changes in load or input voltage. Table 2.1 summarizes the main specifications considered in this thesis.

Specification	Meaning
Dropout voltage	Minimum input-output voltage difference required for regulation
Headroom voltage	Input-output margin required to satisfy a given performance target
Quiescent current	Current consumed internally by the regulator control circuitry
Power and current efficiency	Ratio between useful load power or current and total supplied power or current
Load regulation	DC output-voltage variation caused by load-current changes
Line regulation	DC output-voltage variation caused by input-voltage changes
Load transient response	Output undershoot, overshoot, and recovery after a load step
Line transient response	Output disturbance and recovery after an input-voltage step
Accuracy	Total deviation of the output voltage from its nominal value
PSRR	Attenuation of input-supply ripple at the output
Output impedance	Small-signal impedance seen looking into the regulated output node
Loop stability	Ability of the feedback loop to remain stable over operating conditions

Table 2.1: Main LDO specifications considered in this thesis.

2.1 Dropout Voltage

The dropout voltage is one of the most characteristic specifications of an LDO. Referring to the simplified LDO schematic in Fig. 2.3(a), the regulator can be seen as a controlled pass device placed between the input rail and the output node. The difference $V_{\mathrm{IN}}-V_{\mathrm{OUT}}$ is the voltage left across this pass device. As long as this voltage is sufficiently large, the feedback loop can adjust the pass-device control terminal and keep the output voltage regulated.

The dropout voltage is defined as the minimum input-output voltage difference for which the regulator is still able to maintain the desired output voltage at the specified load current. It is commonly expressed as

$$V_{\mathrm{DO}} = V_{\mathrm{IN,min}} - V_{\mathrm{OUT}}$$

The operating principle shown in Fig. 2.3(b) can be described in terms of the effective resistance of the pass device. As V_{IN} decreases, the feedback loop increases the conduction of the pass device, reducing R_{ON} while keeping V_{OUT} approximately constant. This behavior continues until the on-resistance of the power transistor reaches its minimum value. At that point, the device cannot provide any further increase in conduction, and the LDO enters the dropout region. A further decrease in V_{IN} then causes V_{OUT} to decrease as well. The dropout voltage can be expressed as

$$V_{\mathrm{DO}} = R_{\mathrm{ON}} \times I_{\mathrm{LOAD}}$$

where I_{LOAD} is the load current and R_{ON} is the total resistance across the power path.

This behavior can also be understood by considering the regions of operation of a linear voltage regulator, represented in Fig. 2.4. For large enough input voltage, the regulator operates in the normal regulation region: the output voltage remains almost constant and the excess input-output voltage is dropped across the pass device. When V_{IN} decreases, the voltage available across the pass device decreases. At the dropout boundary, the pass device reaches its maximum conduction capability for the given load current, and the control loop has no additional margin to increase the delivered current. Below this point, the regulator leaves the regulation region and the output voltage starts following the input voltage more directly. It can also be seen that a smaller load current results in a proportionally lower dropout voltage, allowing the regulator to achieve higher power efficiency.

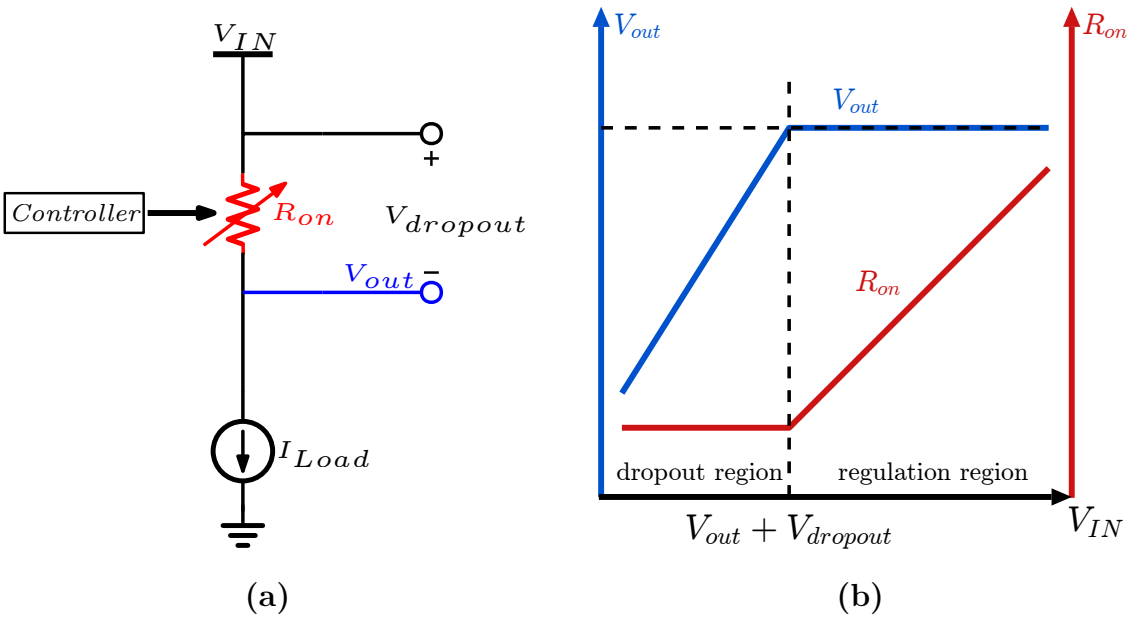


Figure 2.3: Simplified schematic of an LDO and its operating regions.

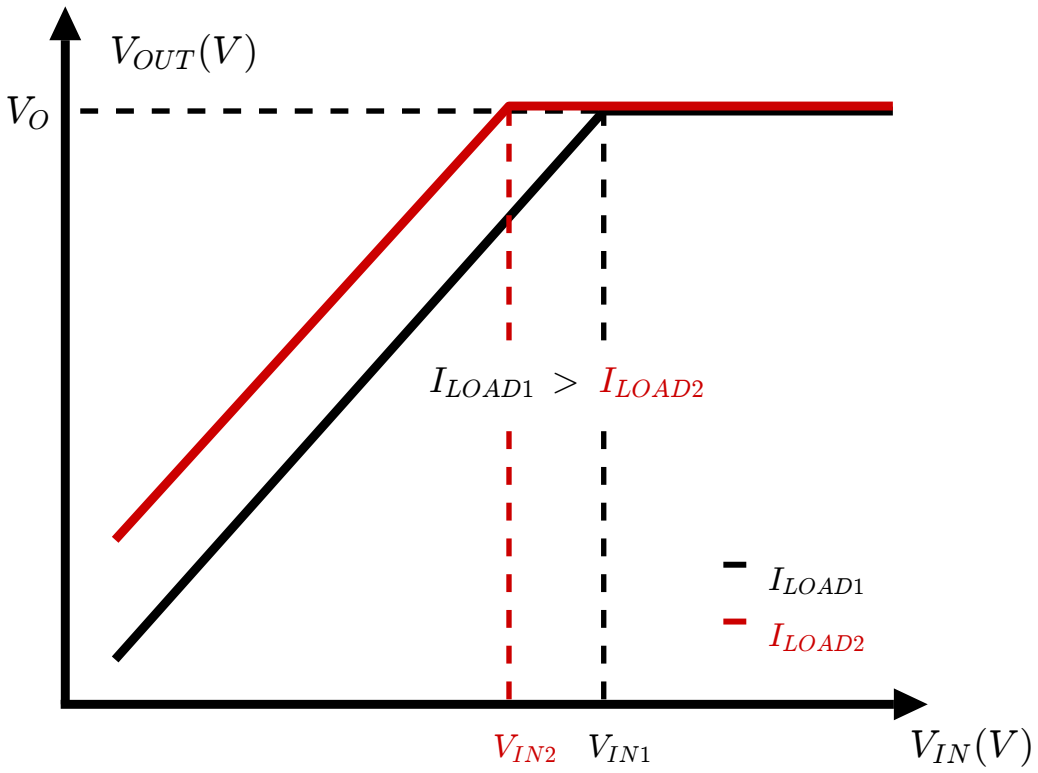


Figure 2.4: Regions of operation of a linear voltage regulator.

In a PMOS LDO, the dropout voltage is strongly related to the on-resistance and sizing of the PMOS pass transistor at the maximum load current. A first-order interpretation is that, near dropout, the pass device behaves like a small resistance and the voltage drop is approximately proportional to the load current. Therefore, reducing

dropout usually requires a larger pass transistor or a stronger gate drive. This improves low-voltage operation but increases the parasitic capacitance at the pass-device gate, which can slow down the regulator and complicate the design of a high-bandwidth fully integrated LDO.

For a fully integrated regulator, low dropout is valuable because it allows the regulated rail to remain close to the available supply voltage. However, the dropout value must not be considered only as a static voltage number: it also affects pass-device area, gate capacitance, transient response, efficiency, and the available headroom for the internal control circuitry.

2.2 Headroom Voltage

Headroom voltage is related to dropout, but it is not necessarily identical to it. Dropout identifies the minimum input-output voltage difference needed to keep the regulator in regulation, whereas headroom is the practical voltage margin left for the internal devices and control circuitry to operate correctly.

In general, a larger headroom gives the regulator more room to control the pass device and preserve its behavior across operating conditions. For this reason, headroom is treated as a broader design margin, while dropout remains the minimum operating limit.

2.3 Quiescent Current

The quiescent current I_{Q} is the current consumed by the regulator itself, excluding the load current. It includes the bias current of the voltage reference, error amplifier, buffers, local feedback devices, and any auxiliary circuits. A low I_{Q} is desirable because it reduces the static power overhead of the regulator, especially at light load.

Quiescent current is directly related to the efficiency of an LDO. Neglecting minor leakage contributions, the input current can be approximated as

$$I_{\mathrm{IN}} \simeq I_{\mathrm{LOAD}} + I_{\mathrm{Q}}$$

Therefore, the current efficiency is

$$\eta_{\mathrm{I}} = \frac{I_{\mathrm{LOAD}}}{I_{\mathrm{LOAD}} + I_{\mathrm{Q}}}$$

while the power efficiency of a linear regulator can be written as

$$\eta_{\mathrm{P}} = \frac{V_{\mathrm{OUT}} \cdot I_{\mathrm{LOAD}}}{V_{\mathrm{IN}} \cdot (I_{\mathrm{LOAD}} + I_{\mathrm{Q}})} = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} \cdot \eta_{\mathrm{I}}$$

These expressions show that efficiency is limited both by the voltage drop across the pass device and by the current consumed internally by the regulator. The effect of I_{Q} becomes especially important at light load, where I_{LOAD} is small and the bias currents can dominate the total power consumption.

From these relations, high efficiency requires both a small input-output voltage difference and a quiescent current that remains small with respect to the load current. Current efficiency is therefore useful to evaluate the bias-current overhead of the regulator, while power efficiency also includes the loss caused by the voltage dropped across the pass device.

In a high-bandwidth capless LDO, quiescent current is tightly connected to speed. Increasing bias currents can improve transconductance, slew rate, pass-device gate driving, and recovery from transients, but it reduces efficiency. The proposed analog FVF-based design must therefore balance low internal consumption against the current needed to satisfy the transient and stability requirements.

2.4 Load Regulation

Load regulation quantifies the DC change in output voltage caused by a change in load current. It can be expressed as

$$\text{Load Regulation} = \frac{\Delta V_{\mathrm{OUT}}}{\Delta I_{\mathrm{LOAD}}}$$

This quantity has the dimension of resistance and is closely related to the low-frequency closed-loop output resistance of the regulator. A smaller value indicates that the output voltage is less sensitive to load-current variations.

For capless operation, load regulation is also a useful static indicator of how effectively the feedback loop controls the output node. The dynamic response to fast load steps is treated separately, but both static load regulation and load transient response depend

on the ability of the loop to lower the effective output impedance.

2.5 Line Regulation

Line regulation measures the DC sensitivity of the output voltage to variations of the input voltage. It is typically written as

$$\text{Line Regulation} = \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}}$$

A low line-regulation value means that slow changes in the supply are rejected by the control loop and do not significantly shift the regulated output voltage.

In integrated systems, the input rail of a local LDO can be affected by IR drops, switching activity, and neighboring power domains. Good line regulation is therefore required to preserve the DC accuracy of the local supply. Unlike PSRR, which is frequency dependent, line regulation describes the low-frequency or static component of input-supply sensitivity.

2.6 Load Transient Response

Load transient response describes the output-voltage deviation that occurs when the load current changes abruptly. The main quantities are undershoot, overshoot, settling or recovery time, load-step amplitude, and load-step edge time. In a capless LDO, the output capacitor cannot supply or absorb a large amount of charge during the transient, so the control loop must react quickly.

The initial voltage deviation is influenced by the available output capacitance, the load-step slew rate, and the effective output impedance at high frequency. The recovery behavior depends on loop bandwidth, slew rate at the pass-device control node, and stability margins. A typical load-transient waveform reports the applied current step together with the corresponding output-voltage response, so that the maximum undershoot, maximum overshoot, and settling time can be identified. The worst case usually occurs for fast load steps and small output capacitance, because the control loop has very little stored charge available at the output node. As can be seen in Fig. 2.5, the output voltage first deviates from its nominal value and then returns to the regulated level after the loop reaction.

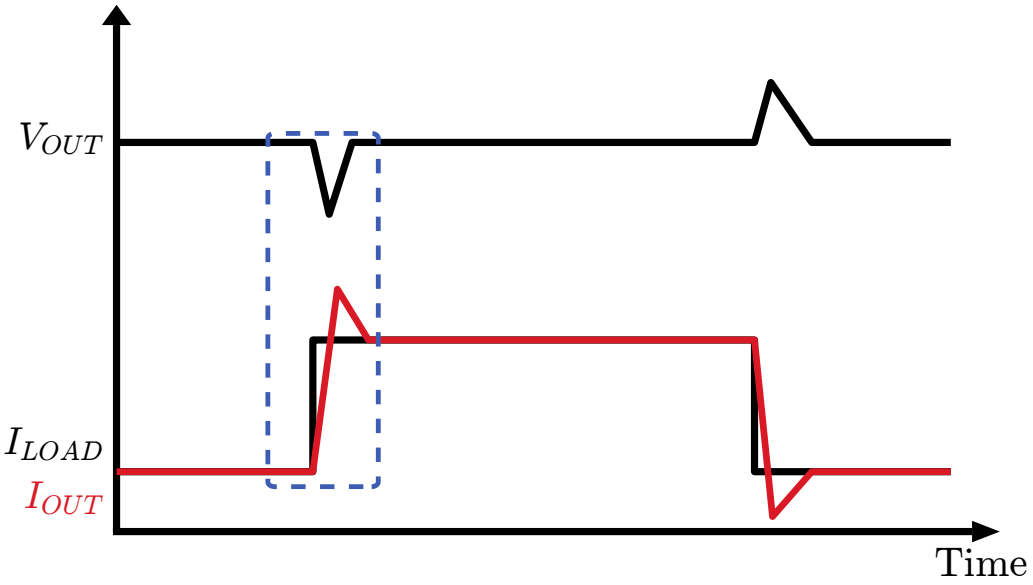


Figure 2.5: Typical load-transient response of an LDO.

For this thesis, load transient response is one of the central metrics because the target regulator must limit both undershoot and overshoot while operating without an external output capacitor.

2.7 Line Transient Response

Line transient response evaluates the output-voltage disturbance caused by a rapid change in the input voltage. While line regulation describes the final DC shift, line transient response includes the temporary output spike, dip, and recovery behavior. It therefore depends on the direct feedthrough from input to output, the pass-device parasitics, and the speed of the feedback loop. A line transient test is usually performed by applying a voltage step at the input and observing how much of this disturbance appears at the regulated output before the loop restores the nominal value. As can be seen in Fig. 2.6, the output response is characterized by an initial disturbance followed by a recovery interval.

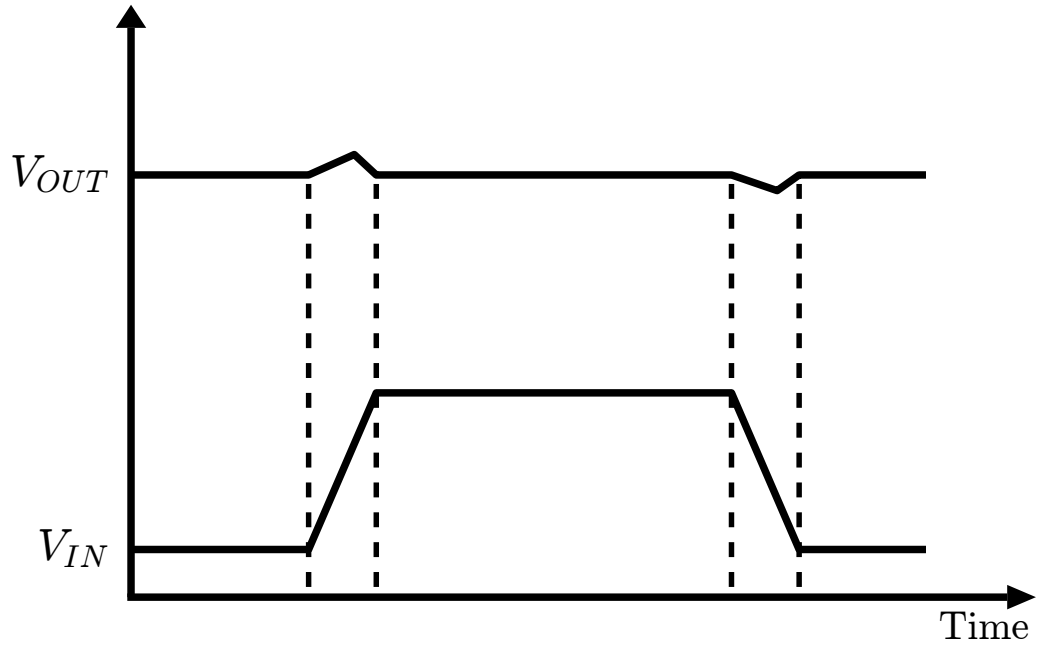


Figure 2.6: Typical line-transient response of an LDO.

This specification is relevant because a fully integrated LDO often receives its input from a noisy shared supply or from a preceding switching converter. The regulator must prevent input-voltage steps from becoming excessive output disturbances, especially when powering sensitive analog or RF blocks.

2.8 Accuracy

Accuracy error measures the deviation of the actual output voltage from its target value. It is usually expressed as a percentage of the target output voltage and can include reference error, feedback-ratio error, amplifier offset, finite loop gain, load regulation, line regulation, parasitic effects, and process, voltage, and temperature (PVT) variations. Interconnect, bonding, and package parasitics can also contribute to the error because the voltage sensed by the regulator may not be exactly equal to the voltage effectively delivered to the load. Series resistances introduce load-dependent voltage drops, while parasitic capacitances and inductances can couple disturbances or modify the transient behavior of the regulated node.

For an LDO with nominal output voltage $V_{\mathrm{OUT,nom}}$, the relative accuracy error can be written in compact form as

$$\epsilon_{\mathrm{ACC}} = \frac{|V_{\mathrm{OUT}} - V_{\mathrm{OUT,nom}}|}{V_{\mathrm{OUT,nom}}} \cdot 100\,\%$$

In this thesis, the overall output accuracy target is used as a system-level constraint: each design choice that affects the regulated DC value contributes to the final error budget.

2.9 Power Supply Rejection Ratio

The power supply rejection ratio (PSRR) describes the ability of a voltage regulator to reject disturbances present on its input supply. In practical systems, the input rail of an LDO is not ideal: it can contain ripple generated by a previous switching converter, voltage fluctuations caused by other blocks, or noise coupled through the package and power distribution network. PSRR measures how much of this disturbance is transferred to the regulated output.

It is commonly defined in decibels as

$$\mathrm{PSRR}(f) = 20 \log_{10} \left| \frac{v_{\mathrm{in}}(f)}{v_{\mathrm{out}}(f)} \right|$$

A higher PSRR means that a given input ripple produces a smaller output ripple. This is important when the LDO supplies noise-sensitive analog or RF circuits, where residual supply ripple can degrade gain accuracy, noise, jitter, phase noise, or linearity.

PSRR is not a constant value, but a frequency-dependent specification. At low frequency, the feedback loop can usually suppress input variations if sufficient loop gain is available. At higher frequency, the loop gain decreases and direct feedthrough paths through the pass device, parasitic capacitances, bias circuits, and substrate or package coupling become more important. Therefore, a regulator can show good rejection in one frequency range and poor rejection in another.

In an LDO, PSRR is shaped by the interaction between the feedback loop and the uncontrolled ripple paths from input to output. In a PMOS capless LDO, the pass-device gate, local feedback path, output capacitance, and bias network can all affect how supply ripple is converted into output ripple. For this reason, PSRR cannot be treated as an isolated number: it must be evaluated together with bandwidth, stability, load condition, and the expected spectrum of supply disturbances.

2.10 Output Impedance

The output impedance Z_{OUT} describes the small-signal impedance seen looking into the regulated output node of the LDO. It links a variation of load current to the corresponding variation of output voltage and indicates how close the regulator is to an ideal voltage source. A low output impedance means that the output voltage is weakly affected by load-current variations.

As commonly done in small-signal analysis, Z_{OUT} can be calculated by applying a test current at the output node and measuring the resulting output voltage variation, with the independent signal sources set to AC ground:

$$Z_{\mathrm{OUT}}(s) = \left| \frac{v_{\mathrm{out}}(s)}{i_{\mathrm{test}}(s)} \right|$$

At low frequency, Z_{OUT} is related to load regulation, since a DC change in load current produces a finite output-voltage variation. At higher frequency, it strongly influences the initial voltage deviation during load transients because the loop may not react instantaneously.

In an LDO, the output impedance is reduced by the feedback loop over the frequency range where sufficient loop gain is available. When the loop gain decreases, the impedance rises and the output becomes more sensitive to fast load changes. For fully integrated and capless LDOs, maintaining a low output impedance over a wide frequency range is particularly important because the output capacitance is small and cannot provide large charge storage during a transient event.

2.11 Loop Stability

Loop stability determines whether the feedback system returns to its operating point after a perturbation without sustained oscillation. In an LDO, the output voltage is controlled by a feedback loop; therefore, the regulator must be fast enough to correct disturbances but must also preserve sufficient stability margins. If the loop is not properly compensated, the output voltage can show ringing, excessive overshoot, or even sustained oscillations.

Following the usual small-signal approach, stability is evaluated by opening the feedback loop and studying the loop gain $T(s)$. Its frequency response is represented with a Bode plot, where the magnitude and phase of $T(j\omega)$ are shown as a function of

frequency. A typical gain and phase plot is reported in Fig. 2.7.

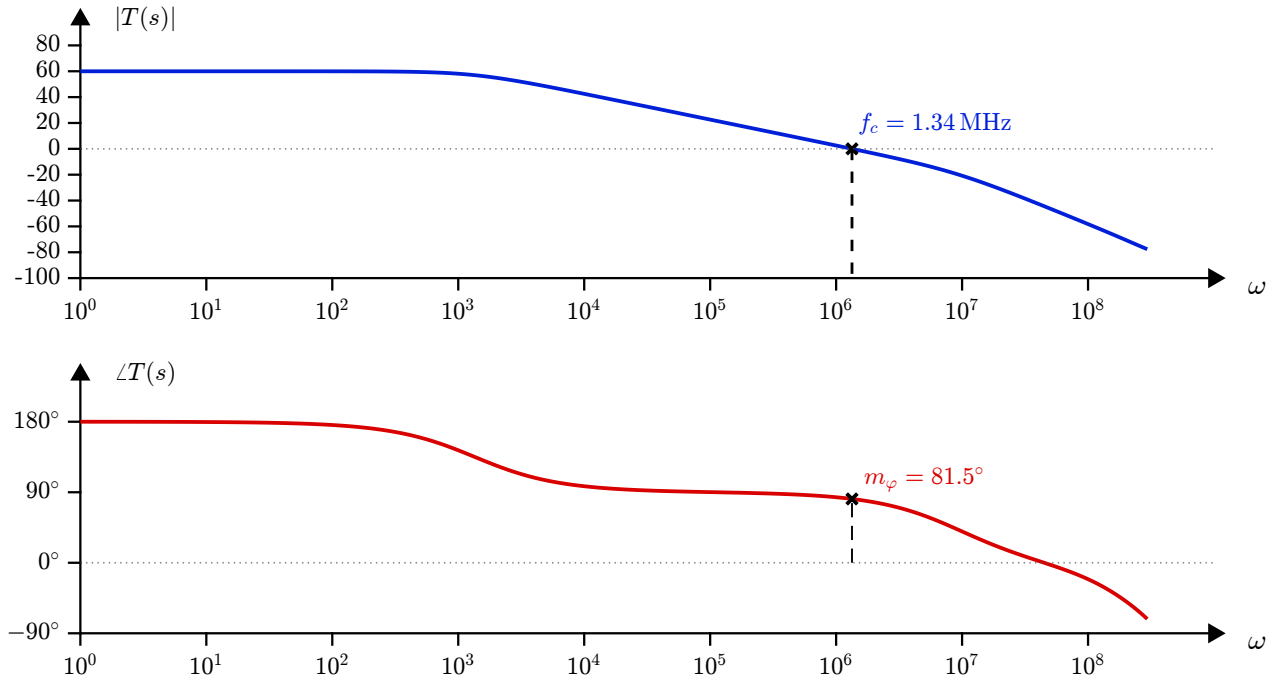


Figure 2.7: Loop gain and phase Bode plot used to evaluate stability.

The main metrics extracted from this plot are the DC gain, the bandwidth, the phase margin, and the gain margin. The DC gain is the low-frequency value of the loop gain and determines how accurately the feedback loop can reduce static output-voltage errors. The bandwidth gives an indication of the frequency range over which the loop can effectively correct output-voltage variations. The phase margin, denoted by m_φ in Fig. 2.7, is evaluated at the frequency where the loop-gain magnitude crosses 0 dB and indicates how far the system is from the condition that can produce oscillation. In practice, a phase margin of about 45° is usually considered a minimum acceptable value, while values around 60° or higher are generally preferred to obtain a more damped transient response with limited ringing. The gain margin is evaluated at the frequency where the loop phase crosses 0°, assuming that the plotted phase starts from 180°, and indicates how much the loop gain can increase before losing stability. A stable LDO must preserve sufficient margins across load current, output capacitance, input voltage, temperature, and process corners.

Capless LDOs are challenging from a stability point of view because the output pole can move significantly with load current and output capacitance, while the large pass device introduces additional internal poles. Compensation must ensure that the high bandwidth needed for transient response does not produce excessive phase shift. The FVF-based architecture studied in this thesis is therefore evaluated not only for speed, but also for robust loop stability.

Chapter 3

Architecture Analysis for Fast-Loop Capless LDOs

This chapter develops the architectural path followed to obtain a PMOS capless LDO with fast transient response. The discussion first clarifies the difference between conventional LDOs using a large external output capacitor and fully integrated or capless implementations. It then reviews the state of the art for wide-bandwidth and capless regulators, considers classical single-loop PMOS LDO solutions, and highlights their main limitations. These limitations motivate the adoption of a dual-loop architecture, where a slow high-gain loop ensures DC accuracy and a fast local loop improves the response to load-current transients. The final part of the chapter introduces the two FVF-based architectures considered in this work and motivates the choice of the final solution.

3.1 External-Capacitor and Capless LDOs

The output capacitor is one of the elements that most strongly affects the architecture of an LDO. In the traditional implementation, shown conceptually in Fig. 3.1, the regulator is designed to operate with a relatively large capacitor connected at the output node. This solution was the standard choice in the first generations of integrated LDOs: the regulation circuit could be integrated on chip, while the large output capacitor was placed externally because its value was too high to be efficiently implemented in silicon. Depending on the application, this component can reach values in the order of hundreds of nanofarads or microfarads. Its role is not limited to output filtering: it also stores charge for load-current transients and contributes to the small-signal dynamics of the feedback loop. When the load current suddenly increases, the capacitor can temporarily provide part of the missing current while the control loop changes the pass-device operating point. When the load current decreases, it can absorb part of

the excess current and reduce the output-voltage overshoot.

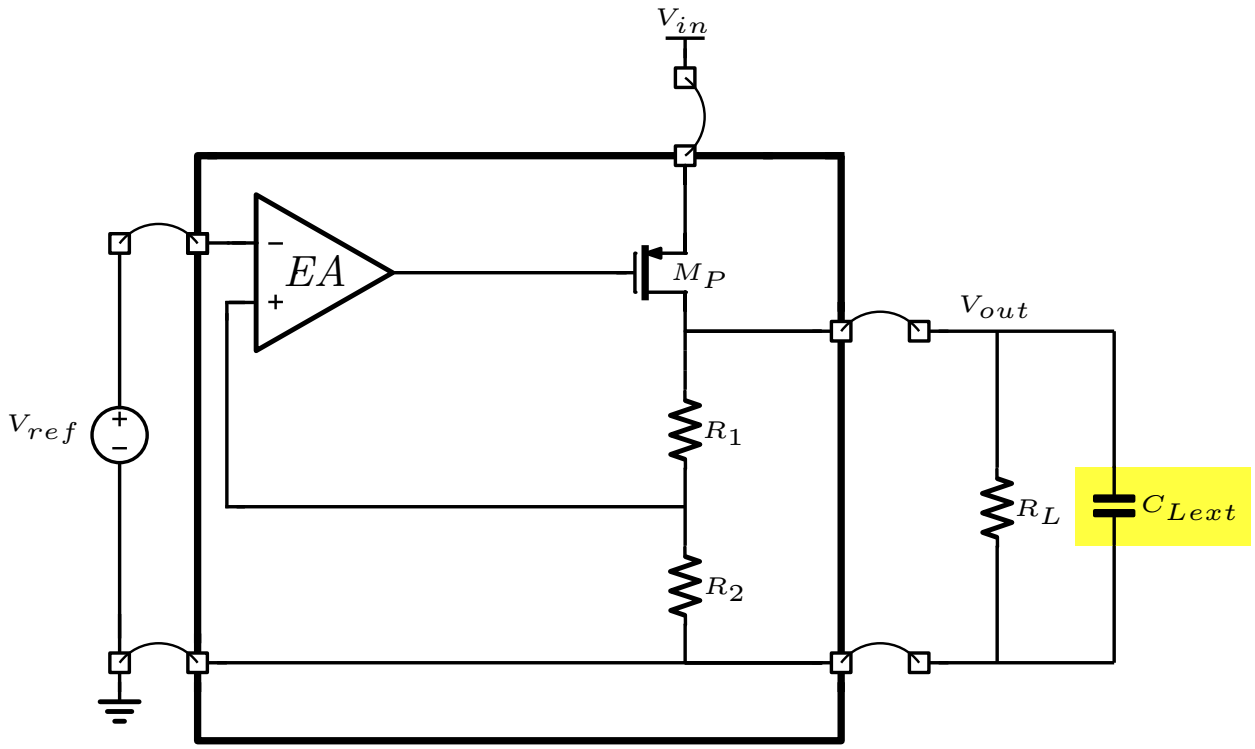


Figure 3.1: Conceptual implementation of an LDO using an external output capacitor.

This behavior makes the external-capacitor LDO robust. The output pole is often intentionally placed at low frequency, and the equivalent series resistance (ESR) of the capacitor can introduce a zero that improves the phase margin. In this case, the dominant pole is usually located at the output node because the external capacitor is much larger than the internal capacitances of the regulator. The large output capacitance also lowers the high-frequency output impedance, attenuates ripple, and reduces the immediate voltage deviation caused by a load step. For these reasons, LDOs with external capacitors are convenient when board area is available and when the load requires a quiet supply with relaxed integration constraints.

The same capacitor, however, becomes a limitation in highly integrated systems. As electronic devices have become smaller and the number of local supply domains inside a chip has increased, the area and cost associated with external passive components have become increasingly undesirable. An off-chip capacitor increases the bill of materials, occupies printed-circuit board area, introduces package and interconnect parasitics, and prevents the regulator from being replicated many times as a compact local supply cell. As discussed in the literature on fully integrated LDOs, a regulator intended for System-on-Chip power management should ideally avoid large external passive components and rely only on on-chip, package, and local load capacitances [1]. This is

the motivation behind capless or output-capacitorless LDOs.

In this thesis, the term capless does not mean that the output node has zero capacitance. In the capless implementation represented in Fig. 3.2, the regulator must satisfy stability and transient requirements without relying on a large external output capacitor. The remaining capacitance is therefore limited to parasitic capacitances, possible small on-chip capacitors, package contributions, and the capacitance already present at the load.

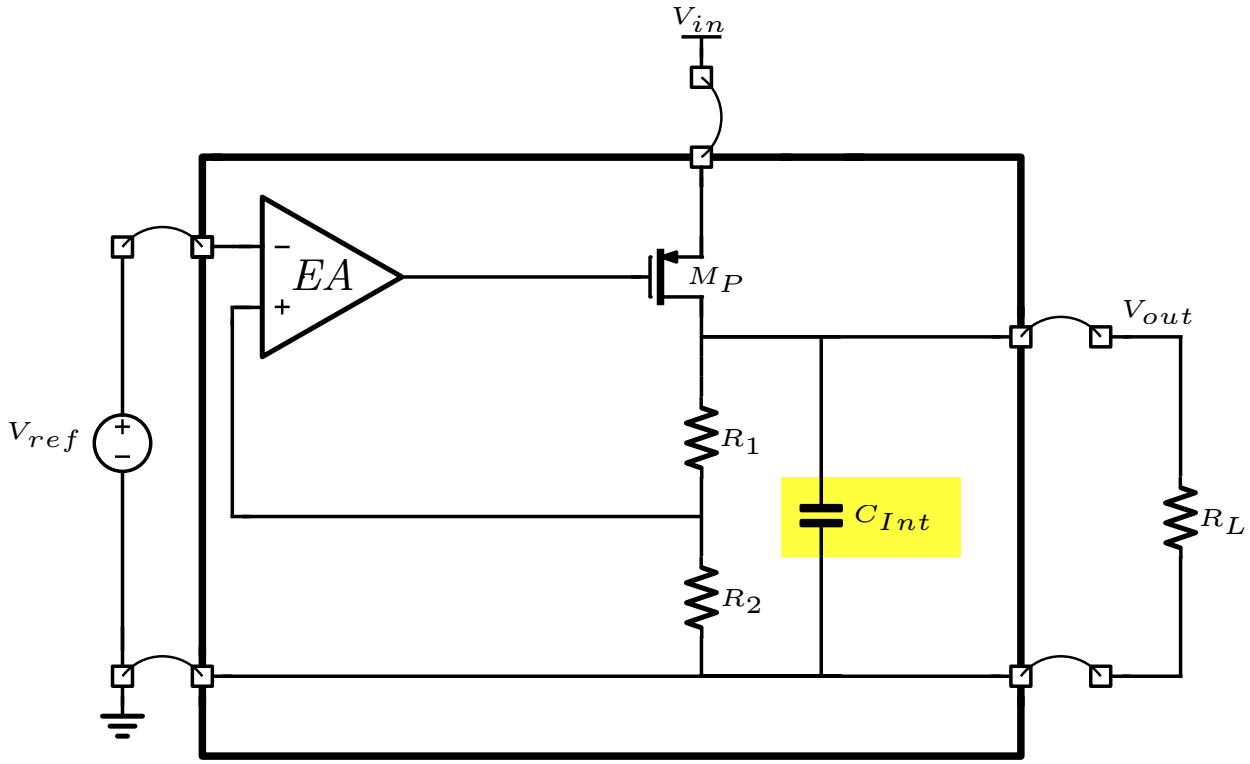


Figure 3.2: Conceptual implementation of a capless or fully integrated LDO.

Removing the external capacitor introduces new design problems. The charge stored at the output node is no longer large enough to mask the finite reaction time of the feedback loop, so load-step undershoot and overshoot depend more directly on the effective output impedance, the available local capacitance, and the speed of the pass-device driving path. At the same time, the output pole is no longer fixed by a large external capacitor. Its position varies with load current and output capacitance, while the dominant pole must be intentionally set by the designer through the architecture, biasing, internal compensation, and placement of the relevant high-impedance nodes. The smaller output capacitance can also make PSRR more difficult to preserve, especially at frequencies where loop rejection is limited. For this reason, capless LDOs require more advanced topologies with faster and more carefully compensated regulation paths than conventional capacitor-assisted LDOs.

The main advantage of a capless architecture is integration. A fully integrated LDO can be placed close to the circuit block it supplies, reducing the distance between regulator and load and enabling fine-grained power distribution. This is especially attractive for RF, analog, mixed-signal, and digital subsystems that need local regulation but cannot afford a dedicated external capacitor for each supply domain. The absence of the external component also reduces system cost and makes the power-management network more scalable.

The price paid for this integration is a more demanding analog design. A capless LDO usually requires higher loop bandwidth, lower output impedance, stronger or more dynamic pass-device gate driving, and a carefully controlled pole-zero distribution. These requirements can increase circuit complexity and quiescent current. They can also reduce design margins because the regulator must remain stable when the load current varies over a wide range and when the output capacitance is small or poorly defined. Table 3.1 summarizes the main differences that guide the architecture choice in this work.

Aspect	LDO with external capacitor	Capless or fully integrated LDO
Output energy buffer	Large external capacitor supplies or absorbs transient current	Only small on-chip, package, and load capacitances are available
Integration	Requires an off-chip component and board area	Suitable for compact local regulation and repeated supply domains
Stability approach	Dominant pole naturally located at the output node; ESR zero can assist phase margin	Dominant pole selected by the designer through architecture and internal compensation
Transient response	Capacitor reduces the initial voltage deviation	Response depends strongly on loop speed, output impedance, and gate driving
Design complexity	Generally more tolerant to loop-speed limitations	More demanding bandwidth, slew-rate, and pole-zero trade-offs
System scalability	Less convenient for many local regulators	Better suited to SoC and point-of-load integration

Table 3.1: Main architectural differences between external-capacitor and capless LDOs.

For the target of this work, the capless option is the relevant one because the regulator is intended as a fully integrated PMOS LDO. The rest of the chapter therefore focuses on architectures that compensate for the missing external energy buffer by reducing output impedance and accelerating the regulation path. This leads naturally to wide-bandwidth solutions, local feedback, and FVF-derived fast-loop structures.

3.2 State of the Art for Wide-Bandwidth Capless LDOs

Modern integrated systems require local voltage regulators able to react quickly to abrupt load-current variations while occupying a small silicon area. Several approaches have been proposed to obtain wide bandwidth, small transient deviation, good PSRR, and stable operation without a large output capacitor. The following discussion presents the most relevant aspects of representative papers in this field, highlighting the specific design choices adopted in each case and the corresponding advantages and limitations. This comparison is useful to identify recurring strategies and trade-offs in the development of capless LDOs.

In [2], a dual-loop FVF-LDO with differential error amplifier and push-pull super source follower (PPSSF) is proposed for fast transient response. The regulator schematic is shown in Fig. 3.3. The PPSSF drives the pass device with low control-path impedance and both sourcing and sinking transient current, leading to about 56 mV overshoot and 74 mV undershoot for a 0 to 20 mA load step with 10 ps edge time.

The main drawback is the increased design difficulty: the SSF becomes an active push-pull stage coupled with the FVF loop and the differential EA, so several internal nodes affect the small-signal dynamics. Compensation is therefore more delicate, and the Bode plots reported in the paper do not show a phase margin consistently above the usual 60° design target.

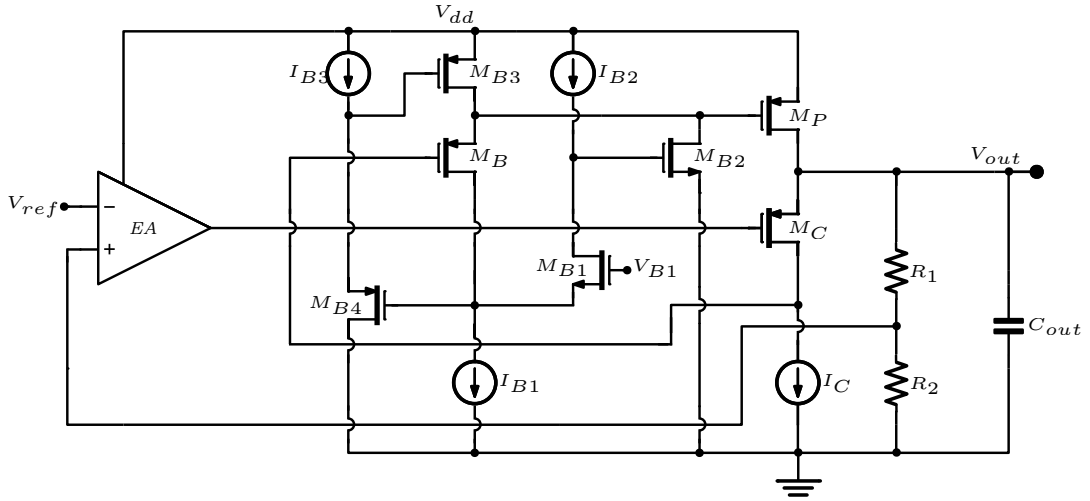


Figure 3.3: Qualitative schematic of the FVF-LDO with PPSSF presented in [2].

Push-pull driving is also used in [3], where a push-pull buffer reduces the impedance at the pass-device gate and improves the transient response. However, the regulator still relies on a single control loop, so the same loop must provide both DC accuracy and fast transient correction.

In [4], an enhanced super source follower (ESSF) is used in an FVF-based LDO for noise-sensitive UWB circuits, as shown in Fig. 3.4. The ESSF is a relatively simple way to reduce the buffer output impedance and obtain a very fast transient response, reported as 312 ps. For a load-current step from 0.1 to 10 mA with 30 ps edge time, the reported undershoot and overshoot are 26 mV and 21 mV, respectively. However, the design sets the dominant pole at the output node, and therefore requires high current to push the internal poles above the UGF. This also leads to stability concerns due to the high-bandwidth loop.

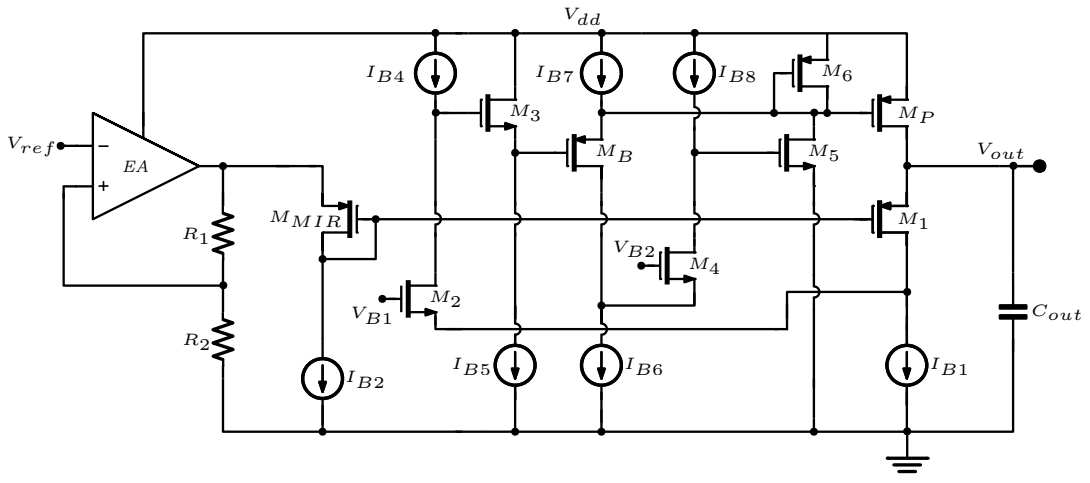


Figure 3.4: Qualitative schematic of the FVF-LDO with ESSF presented in [4].

In [5], an FVF structure with a three-stage gain-enhanced loop and adaptive biasing is proposed. The adaptive bias tracks load variations, increasing the available current during transients while keeping the quiescent current low at light load. For a load step from 100 μA to 10 mA with 300 ns edge time, the reported overshoot and undershoot are about 25.06 mV and 38.73 mV, with 11 μA quiescent current.

This solution combines low-power operation, reduced voltage spikes, and good PSRR, but its performance depends on the adaptive bias path and on the compensation of the multi-stage FVF loop. Since the dominant pole is related to the pass-device gate capacitance, the design must address the slew-rate limit of this node and uses Miller compensation to preserve stability.

In [6], a capacitorless NMOS LDO uses pole-tracking compensation and adaptive feedforward ripple cancellation (FFRC) to improve bandwidth and PSR, as shown in Fig. 3.5, with 83 mV undershoot and 10 mV overshoot for a 1 to 100 mA load step. Although the pole-tracking and FFRC techniques are effective, the architecture is not based on a dual-loop regulation principle, shows limited stability margin, and requires a relatively complex implementation.

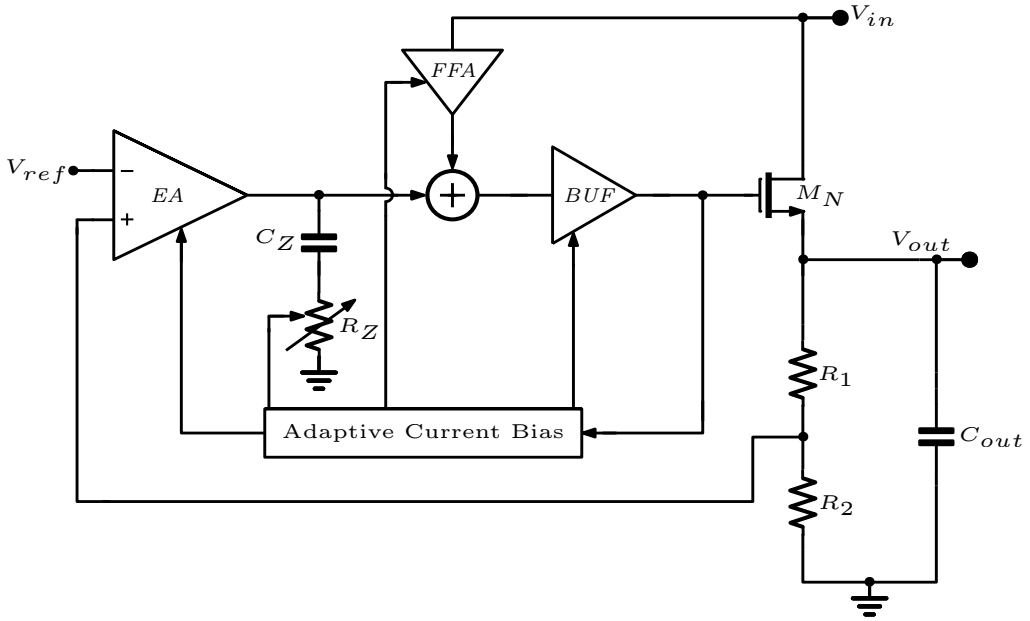


Figure 3.5: Qualitative schematic of the capacitorless NMOS LDO presented in [6].

Similarly, in [7], a fully integrated LDO uses a form of pole tracking based on differentiator-based active-zero compensation and adaptive biasing to follow the output-pole movement and extend the unity-gain bandwidth. This improves bandwidth with low area and low quiescent current, but it relies on an active compensation network that must remain controlled over load and process variations.

Finally, the work in [8] develops an N-type capless FVF-LDO for radio applications using a multi-loop approach, as shown in Fig. 3.6. The design combines a slow loop for accurate DC regulation with a fast FVF-based loop, and adopts a zero-pole tracking compensation strategy to preserve stability as the load current changes. The reported load-current range extends from 100 μA to 200 mA. For the 20–80 mA and 70–160 mA load-current steps, the undershoot/overshoot values are about 60.3/36.0 mV and 82.8/40.5 mV, respectively. The main drawback is the difficulty of stabilizing the fast FVF-based loop over the full load-current range.

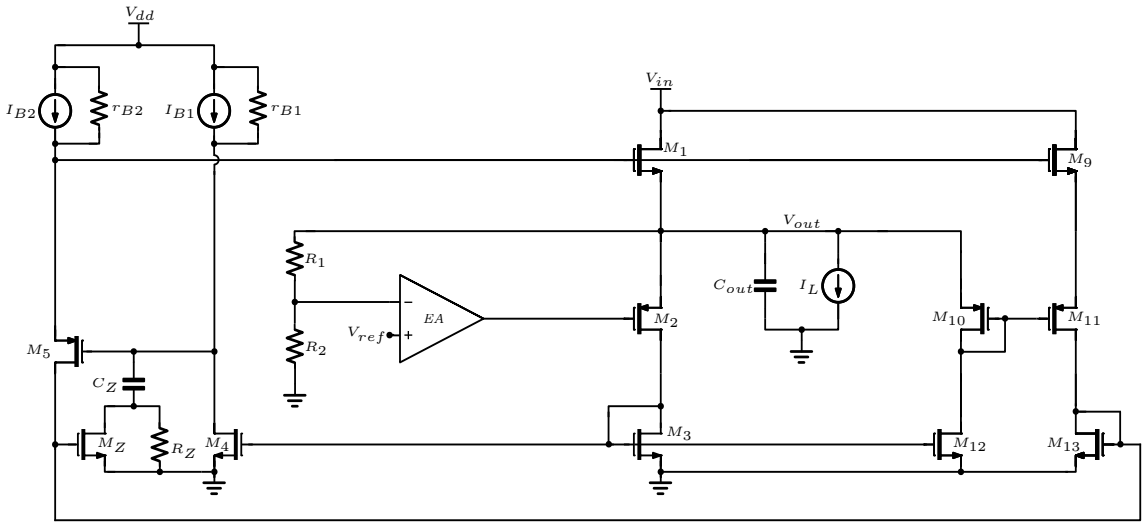


Figure 3.6: Qualitative schematic of the N-type capless FVF-LDO presented in [8].

Table 3.2 summarizes the main advantages, limitations, and numerical values of the most relevant recent works considered for the architecture selection.

Work	Main values	Advantages	Limitations	Main technique
[2]	0–20 mA, 10 ps edge, 74 mV US, 56 mV OS	Simple FVF idea, high bandwidth, strong pass-gate drive	Stability margin not always high; several active internal nodes	FVF, PPSSF, dual loop
[3]	0–50 mA, 100 ns edge, $C_L = 100$ pF, 230 mV US and 170 mV OS	Good bandwidth, good stability, simple push-pull gate drive	Transient spikes remain high	Push-pull buffer
[4]	0.1–10 mA, 30 ps edge, 26 mV US, 21 mV OS, 312 ps response	Very fast response, compact ESSF buffer	Output dominant pole requires high current; stability can be critical	FVF, ESSF buffer
[5]	0.1–10 mA, 300 ns edge, 38.73 mV US, 25.06 mV OS, 11 μA Iq	Low quiescent current, adaptive transient boost, good PSRR	Multi-stage FVF compensation depends on adaptive biasing	FVF, adaptive biasing
[6]	1–100 mA, 83 mV US, 10 mV OS, about 100 MHz bandwidth	High bandwidth and improved PSR	Complex implementation; limited stability margin	Pole tracking, FFRC
[7]	0–25 mA, 1.6–24.2 μA Iq, 2.5–23 MHz UGB	Higher bandwidth with small area and low current	Difficult implementation	Active-zero compensation
[8]	20–80 mA: 36.0 mV OS, 60.3 mV US; 70–160 mA: 40.5 mV OS, 82.8 mV US	Large load range, dual-loop separation, zero-pole tracking	Stability can be critical	FVF, dual loop, zero-pole tracking

Table 3.2: Concise comparison of recent capless LDO architectures used to guide the proposed design.

The reviewed literature shows some recurring techniques for obtaining high bandwidth in capless LDOs. A first trend is the use of multi-loop regulation, where a slow loop preserves DC accuracy while a faster local loop reacts to load transients. This approach appears in several FVF-based solutions [2, 4, 5, 8, 9].

A second trend is the use of low-impedance buffer stages to drive the large gate capacitance of the pass transistor. Enhanced source followers, super source followers, and push-pull buffers are used in [2], [3], and [4] to push the pass-gate pole to higher frequency and improve the transient response. The cost is usually higher current consumption, additional internal nodes, or more difficult compensation.

A third trend is the use of adaptive or tracking compensation. Adaptive biasing, Miller compensation, active-zero compensation, and pole tracking are used in [5], [6], [7], and [8] to maintain bandwidth and stability as the load-dependent poles move. These techniques are effective for high-bandwidth operation, but they make the small-signal behavior more dependent on operating conditions and require careful stability verification.

Overall, state-of-the-art high-bandwidth capless LDOs combine fast local correction, strong pass-device driving, and adaptive compensation. This confirms the need to separate DC accuracy from transient correction, motivating the dual-loop direction

adopted in the following sections.

3.3 Single-Loop PMOS LDO Architectures

A classical PMOS LDO is based on a voltage reference, an error amplifier, a feedback network, and a PMOS pass transistor. The error amplifier compares the feedback voltage with the reference voltage and drives the gate of the PMOS pass device so that the output voltage reaches the desired value. The same loop is therefore responsible for DC accuracy, load regulation, line regulation, and transient recovery.

The first single-loop implementation, shown conceptually in Fig. 3.7, represents the most straightforward solution.

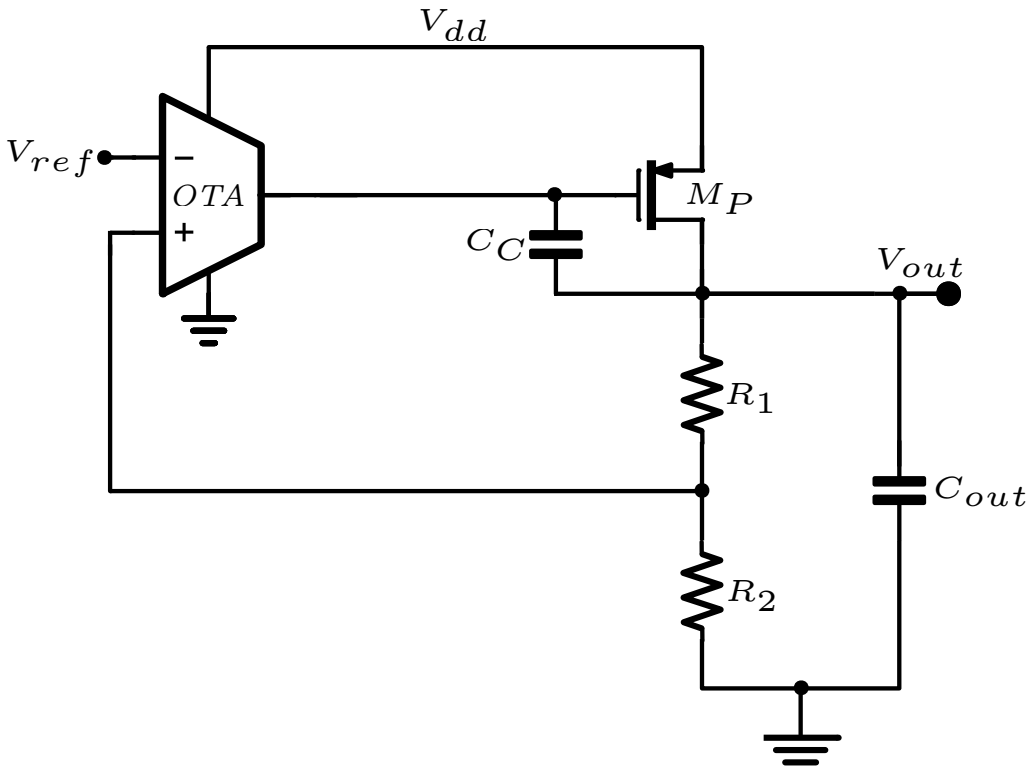


Figure 3.7: Simplified single-loop PMOS LDO architecture considered in this work.

It can provide good static accuracy if the error amplifier has sufficient DC gain. However, this simple architecture cannot provide a sufficiently large bandwidth to obtain a fast enough transient response. In a capless regulator, the output capacitor is not large enough to hide the finite time required by the loop to charge and discharge the large PMOS gate capacitance, so load-current steps can produce significant undershoot,

overshoot, or long settling time.

The second single-loop implementation, represented in Fig. 3.8, was investigated as a possible way to improve the dynamic performance.

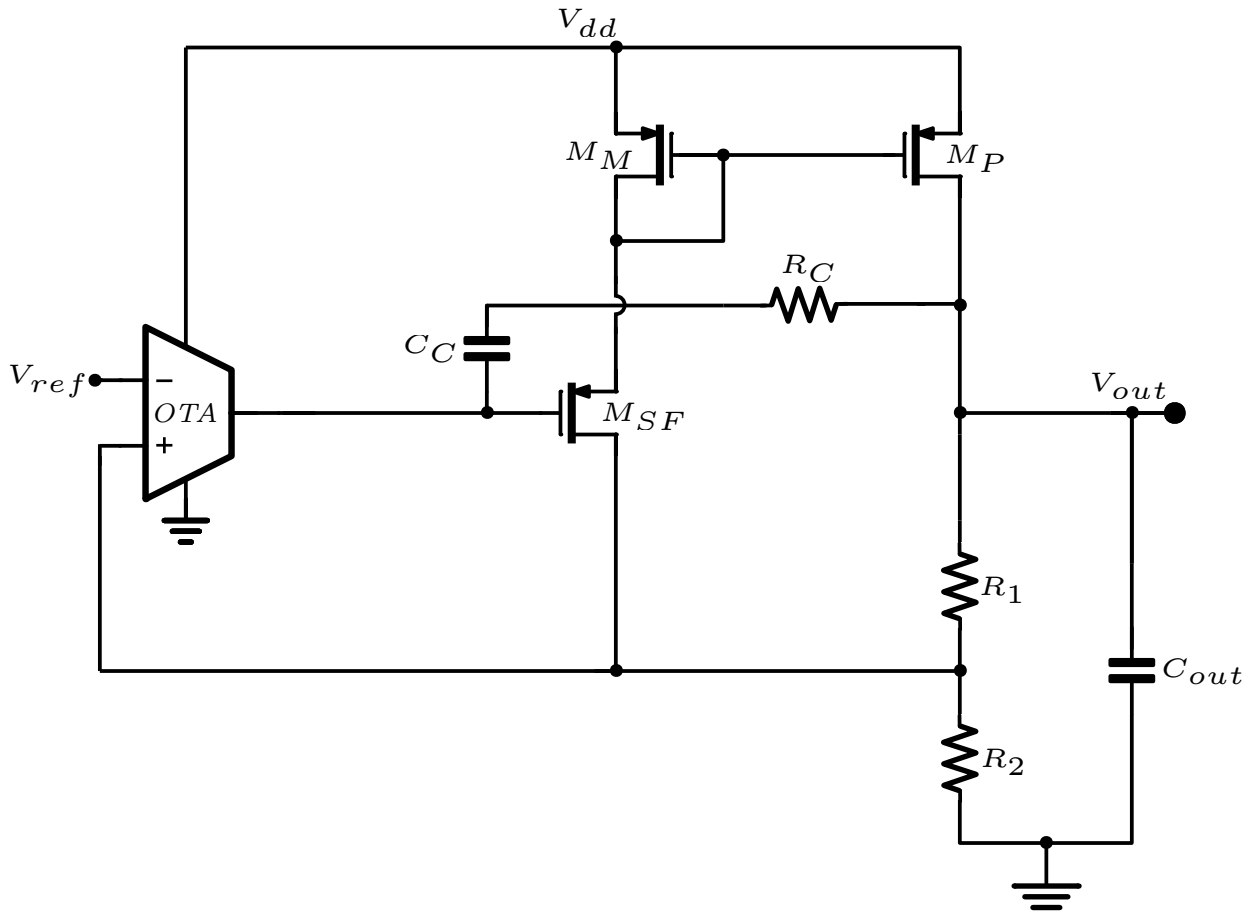


Figure 3.8: Second single-loop PMOS LDO architecture considered in this work.

In this version, a buffer implemented as a source follower was added together with a current mirror. This modification increased the loop bandwidth, as shown by the comparison between Fig. 3.9 and Fig. 3.10: the cutoff frequency increased from about 1.2–1.3 MHz to about 3.8 MHz, corresponding to an improvement of approximately 3x.

However, it was still not sufficient to reach the desired performance targets. Nevertheless, the architecture still relies on a single feedback loop to satisfy both high DC accuracy and fast transient correction. This creates a fundamental trade-off: increasing the loop bandwidth improves the response to load steps, but also makes compensation more critical because the output pole, the pass-device gate pole, and internal amplifier poles all contribute phase shift.

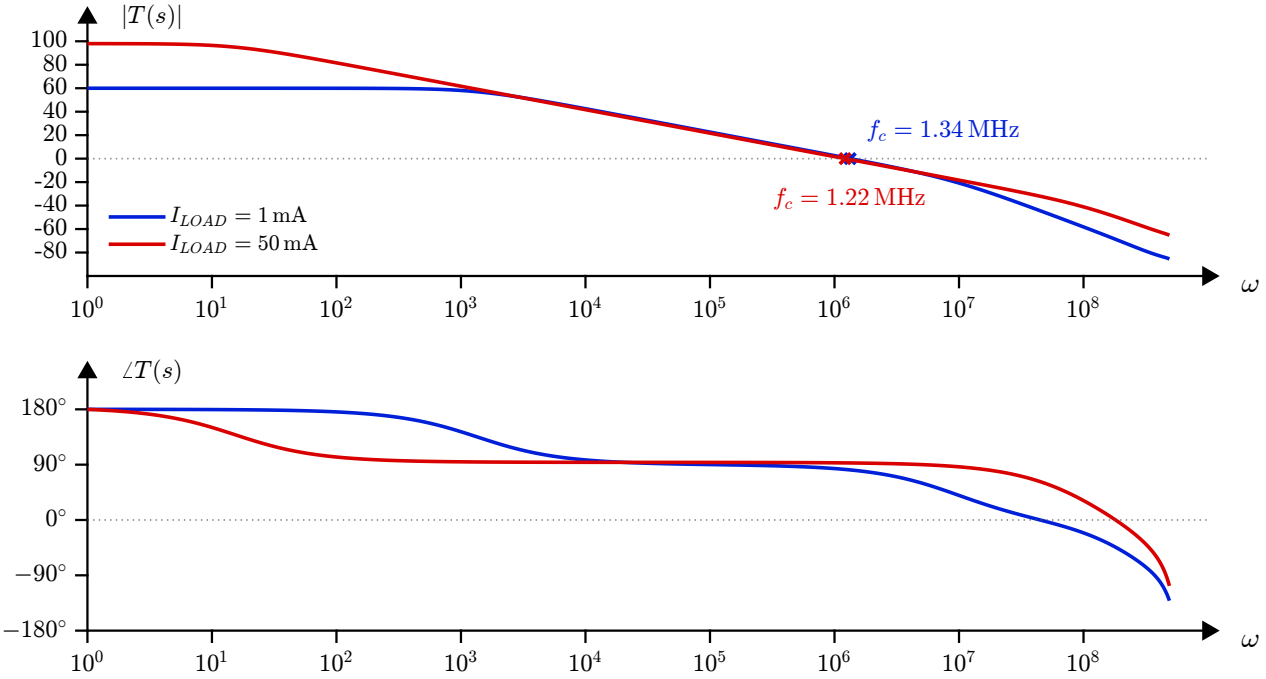


Figure 3.9: Loop-gain Bode plot of the first single-loop PMOS LDO architecture.

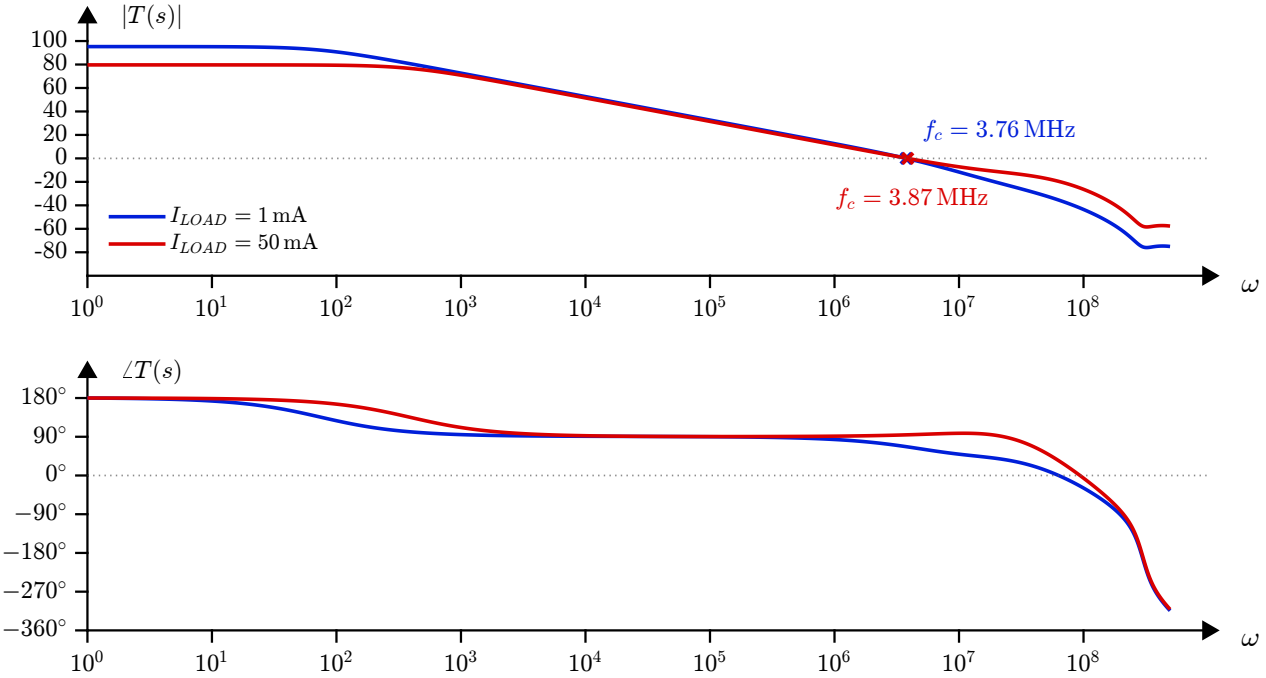


Figure 3.10: Loop-gain Bode plot of the second single-loop PMOS LDO architecture.

These observations motivate a more explicit discussion of the intrinsic limits of single-loop PMOS LDOs before moving toward alternative architectures.

3.4 Limits of a Single-Loop Solution

The main limitation of a single-loop PMOS LDO is that the same feedback path must provide accurate DC regulation, sufficient loop gain, fast transient correction, and stable operation. These requirements pull the error amplifier in opposite directions. A large DC gain is needed to reduce the static error and improve line and load regulation, while a large bandwidth and slew rate are needed to move the pass-device gate quickly during load-current steps. Meeting both targets with the same error amplifier generally requires larger bias currents, because the gain-bandwidth product and slew rate are directly linked to the available transconductance and charging current. In first approximation, the slew-rate limit at a high-impedance internal node can be written as

$$SR \simeq \frac{I_{EA}}{C_{G,P}}$$

where I_{EA} is the current available from the error amplifier to charge or discharge the PMOS gate capacitance $C_{G,P}$. Since the pass device must be large enough to sustain the maximum load current at the required dropout voltage, $C_{G,P}$ is not negligible. A faster gate movement therefore requires more available current, which directly increases the quiescent current. Therefore, improving the dynamic response of a single-loop regulator tends to reduce one of the main advantages expected from an integrated LDO.

Another practical issue observed in the single-loop candidates was the high leakage current of the pass device in hot process-temperature corners. This effect was amplified by the very large device dimensions required for dropout and load-current capability, together with the adopted CMOS technology. Consequently, a higher quiescent current budget was needed to keep robust biasing and regulation than the one finally adopted in the FVF-based solution.

The output node makes this trade-off more severe in a capless implementation. With a large external capacitor, part of a load transient can be supplied or absorbed by the capacitor while the loop reacts. In a fully integrated regulator, the available capacitance is much smaller, so the output-voltage deviation is more directly related to the load-current variation, the output capacitance, and the closed-loop bandwidth. This dependence can be summarized as

$$\Delta V_{OUT} \approx \frac{\Delta I_{LOAD}}{C_{OUT} \cdot BW_{CL}}$$

which shows why a small C_{OUT} must be compensated by a sufficiently large closed-loop

bandwidth to keep undershoot and overshoot limited. When the load current suddenly increases, the PMOS gate must be discharged fast enough to provide the extra current and limit the undershoot. When the load current decreases, the opposite correction must occur quickly enough to avoid overshoot. If the loop bandwidth is too low, these voltage deviations and the settling time become excessive.

Simply increasing the bandwidth of the loop is not a complete solution. The output pole, the pass-device gate pole, and the internal poles of the error amplifier all move with operating point and load current, so an aggressive single-loop design can lose phase margin and exhibit ringing or instability. This is the central reason why the single-loop approach is not ideal for the target of this thesis: the regulator must achieve good DC accuracy, fast load-transient recovery, and low quiescent current at the same time. A more effective solution is therefore to separate these tasks, assigning low-frequency accuracy and fast local correction to different but cooperating paths.

3.5 Dual-Loop Regulation Principle

In a dual-loop LDO, the regulation task is divided into a slow loop and a fast loop. The slow loop includes the reference, the error amplifier, and the low-frequency feedback path. Its main role is to define the correct DC operating point and reduce static output-voltage errors. Since this loop does not need to provide the entire transient correction by itself, it can be designed with emphasis on gain, offset, and robust operating range.

The fast loop is instead designed to react directly to output-voltage variations caused by load-current steps. Its purpose is to reduce the effective output impedance and quickly modify the current delivered by the pass device. During a load-current increase, the fast loop must enhance the PMOS conduction to limit undershoot. During a load-current decrease, it must reduce the delivered current to limit overshoot.

This separation is useful because it avoids forcing a single loop to be both a high-gain accuracy path and a very wide-band transient path. The design problem then becomes the coordination of the two loops: the fast loop must be quick enough to improve the transient response, while the slow loop must restore the accurate output value without destabilizing the overall regulator.

3.6 Flipped Voltage Follower as Fast Loop

The Flipped Voltage Follower (FVF) has emerged as the dominant building block for high-performance LDO regulators, particularly in capless implementations. As shown in Fig. 3.11, the cell consists of a common-drain transistor M_1, acting as a source follower, and a local shunt feedback branch in which M_2 provides the voltage gain. This local feedback loop senses a variation at the output node and converts it directly into a gate-drive correction on the pass device, producing an immediate response to load-current disturbances before the slower high-gain error-amplifier loop has completed its correction.

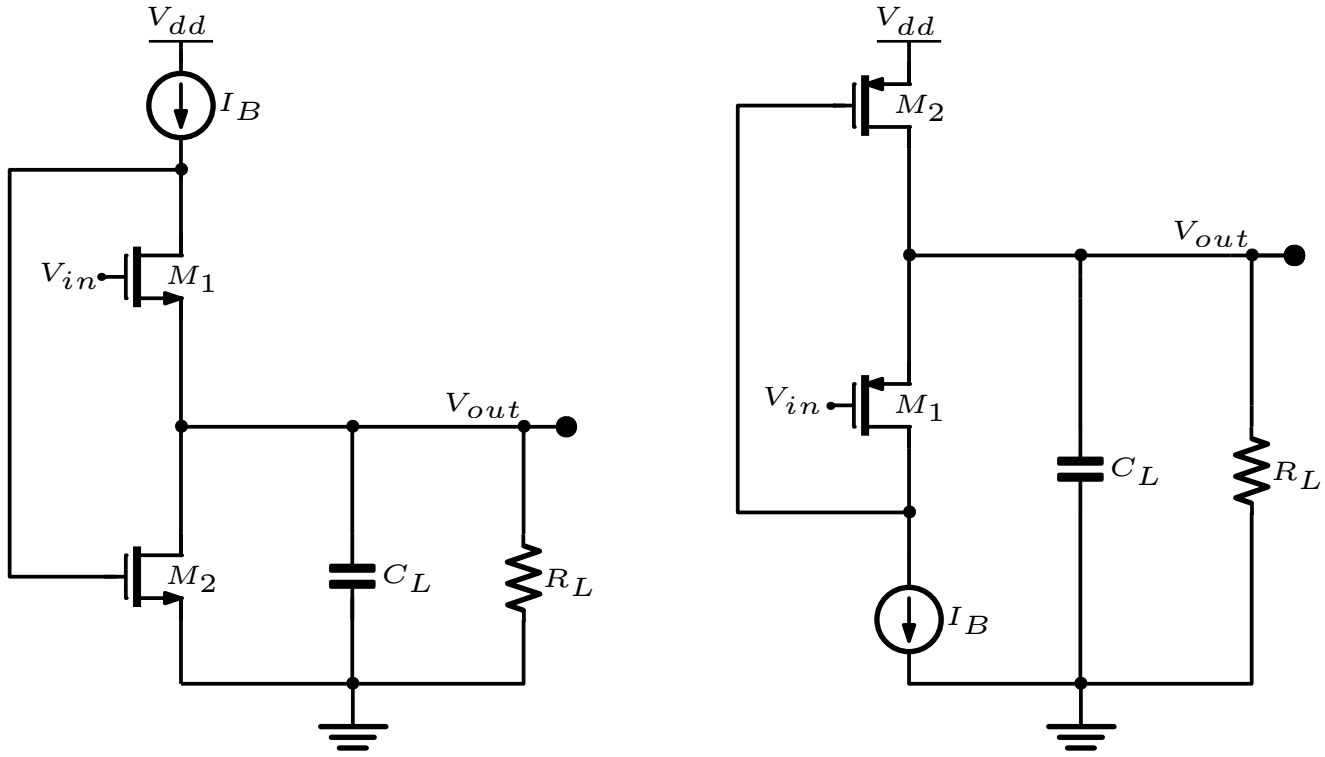


Figure 3.11: Basic NMOS and PMOS Flipped Voltage Follower (FVF) cells.

The FVF can be understood as a source-follower-based cell with local feedback applied at the output node. If the load current suddenly changes, V_{OUT} starts moving immediately because the output capacitance is small. The local FVF path detects this movement and modifies the current delivered by the pass device, opposing the disturbance. In this sense, the FVF does not replace the global loop; it provides a low-impedance dynamic path that reacts faster than the main error amplifier.

The small-signal effect of this local feedback can be interpreted through the output impedance. If the open-loop output impedance of the regulating path is $Z_{\text{out,open}}$ and

the local loop gain is T_{local}, the effective output impedance can be approximated as

$$Z_{\text{out,FVF}} \approx \frac{Z_{\text{out,open}}}{1 + T_{\text{local}}}$$

This relation is only a first-order representation, but it captures the main idea: the local loop reduces the impedance seen by load-current disturbances. For a capless regulator this is crucial, because a smaller output impedance means that a given current step produces a smaller voltage variation before the main loop settles.

In a PMOS implementation, the polarity of the correction must be carefully arranged. When the load current increases, V_{OUT} tends to decrease and the fast path must pull the PMOS gate downward, increasing $|V_{GS}|$ and delivering more current to the load. When the load current decreases, V_{OUT} tends to rise and the gate drive must be relaxed so that the pass device supplies less current. The FVF path is therefore useful only if it is both fast and able to drive the pass-device gate with the correct sign.

This mechanism also introduces practical design constraints. The local loop adds internal nodes, poles, and bias branches, so its bandwidth cannot be increased independently of the pass-device gate pole and of the slower accuracy loop. In addition, buffers used to strengthen the gate drive require current and voltage headroom. The FVF should therefore be seen as a redistribution of the regulation task rather than as a simple gain increase: the slow loop defines the accurate DC operating point, while the FVF path lowers the dynamic output impedance and provides the first correction during load transients. This principle motivates the FVF-based architectures analyzed in the following sections.

3.7 FVF-Based Considered Architectures

The first FVF-based solution introduces a PMOS FVF path with source-follower buffering. The source follower helps drive the high-capacitance gate of the pass device and reduces the impedance of the internal control node. Compared with the single-loop architectures, this solution provides a more direct path from output voltage variation to pass-current correction.

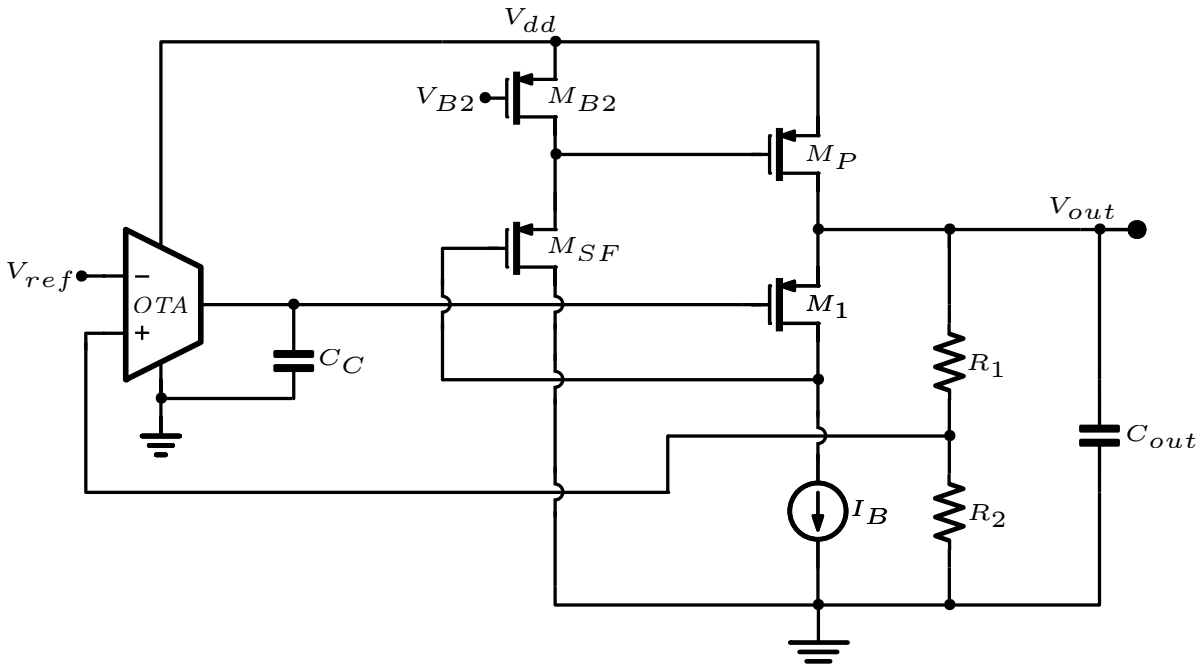


Figure 3.12: PMOS FVF architecture with source-follower buffering.

The architecture in Fig. 3.12 improves the transient behavior, but it also introduces additional internal nodes and poles. The buffer consumes bias current, requires voltage headroom, and interacts with the slow regulation loop. Therefore, its PVT behavior must be evaluated over load current, output voltage margin, input voltage, temperature, and process corners. Although this architecture can provide the desired fast-loop performance in terms of bandwidth and load-transient undershoot/overshoot, it was not selected because of a clear headroom limitation, as shown in Figs. 3.13 and 3.14. Under some critical operating conditions, the pass-device gate must rise close to $V_{DD} = 1.8\,\mathrm{V}$. As a consequence, the buffer gate and the drain of the second PMOS in the FVF path (M_1) are also pushed to a high voltage. Since the source of M_1, V_{OUT}, is fixed at 1.2 V, this condition can push M_1 out of saturation, as shown in Fig. 3.14 when $V_{DS} - V_{DSAT}$ drops below 0 V. As a result, the output voltage is no longer regulated with the required accuracy, as reflected by the deviations visible in Fig. 3.13.

The PVT response of this architecture is summarized in the next two figures. Figure 3.13 reports the output-voltage behavior across temperature for different load currents and process corners, while Fig. 3.14 reports $V_{DS} - V_{DSAT}$ of M_1 under the same conditions.

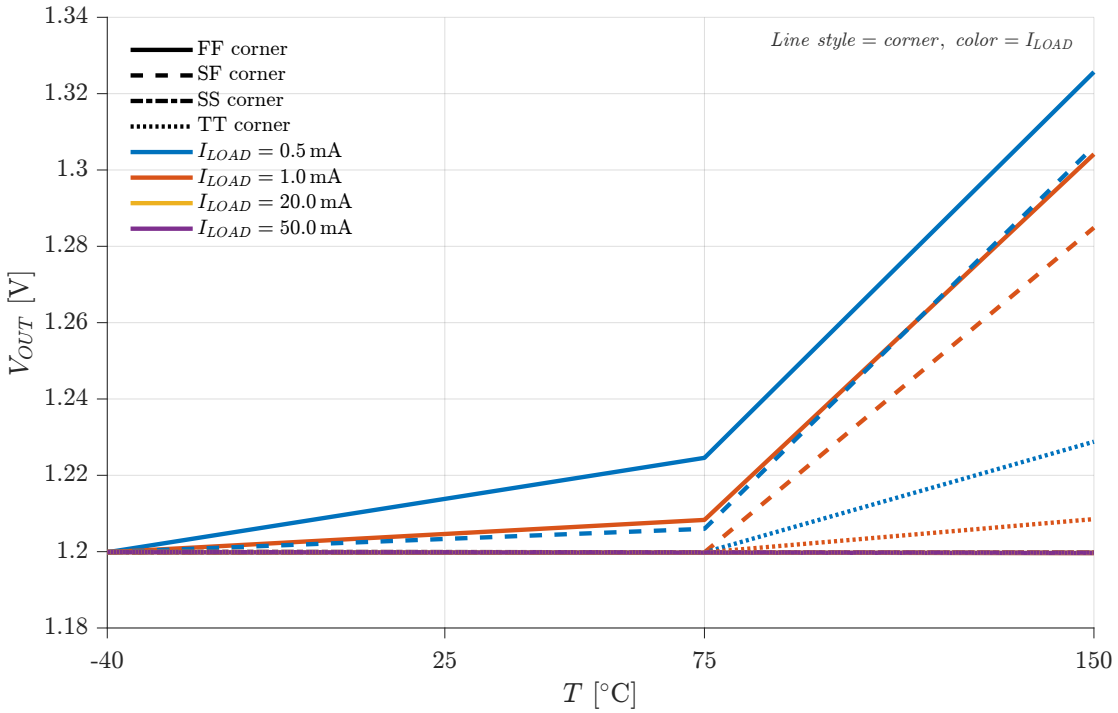


Figure 3.13: Output-voltage variation of the proposed PMOS FVF SF architecture versus temperature for different load currents and process corners.

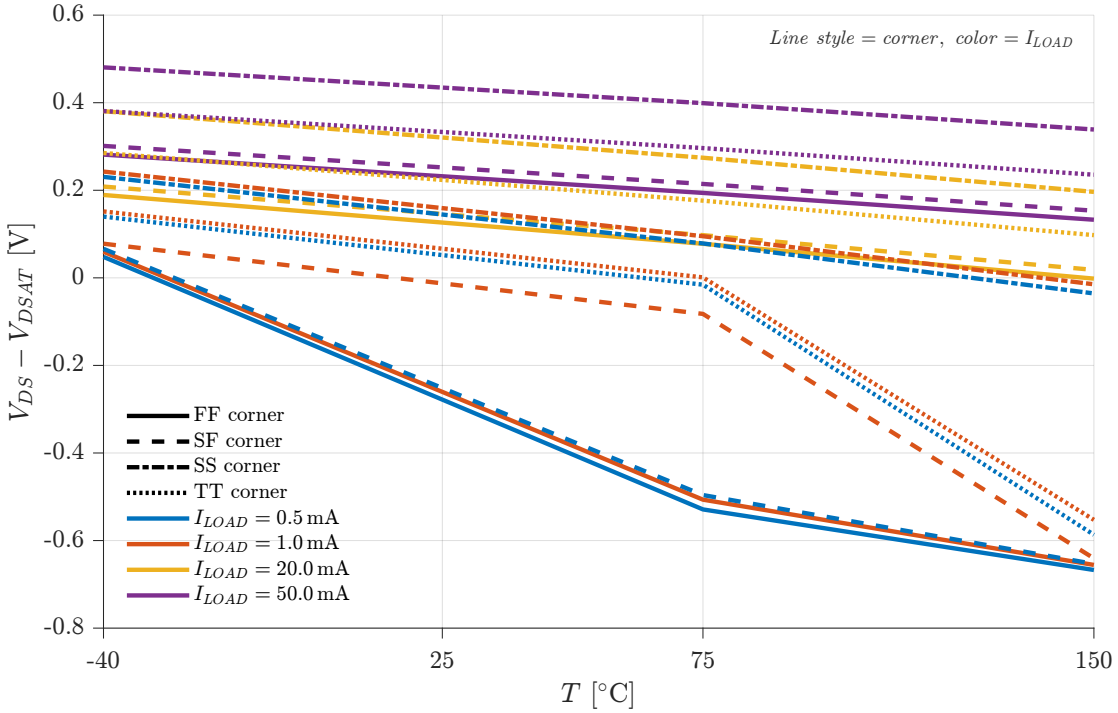


Figure 3.14: $V_{DS} - V_{DSAT}$ of M_1 (second PMOS transistor in the FVF path) versus temperature for different load currents and process corners.

The second FVF-based solution, adopted as the final architecture in this thesis, is an evolution of the first FVF solution in which an additional common-gate device,

M_{CG}, is inserted between the source-follower buffer and the drain of M_1, as shown in Fig. 3.15. Thanks to this common-gate stage, the architecture can preserve the dual-loop FVF advantages while maintaining correct operation in the critical corners.

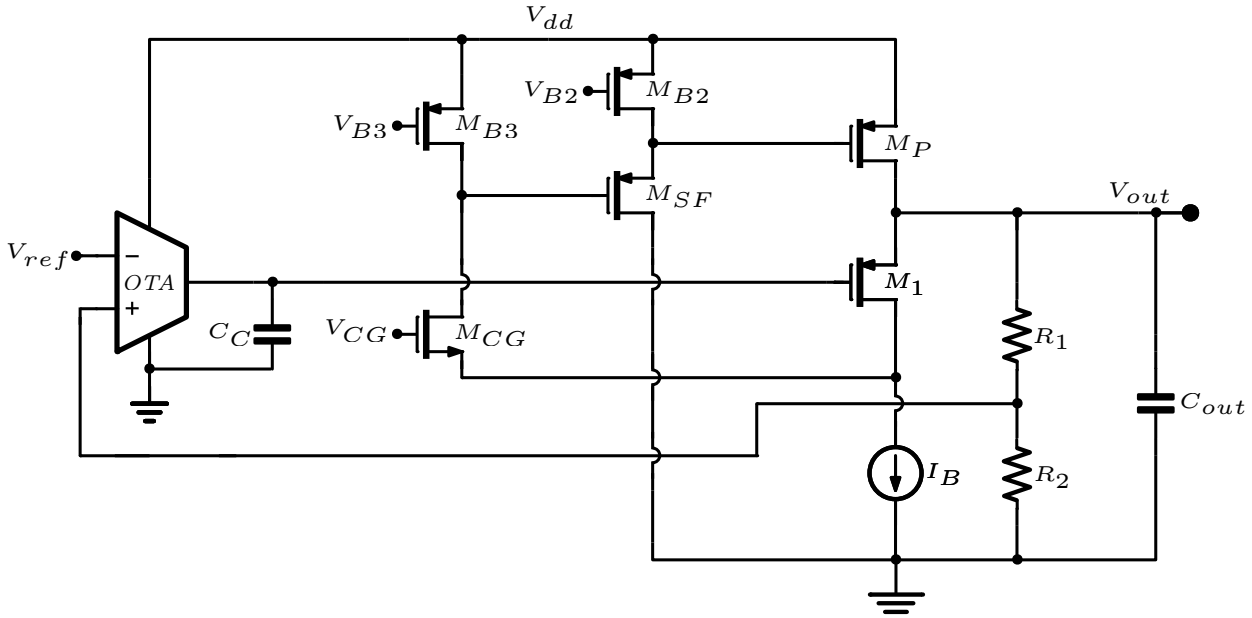


Figure 3.15: Final FVF architecture selected for this work.

Starting from the topology of Fig. 3.15, the design can be tuned to reach the target fast-loop bandwidth while preserving stable interaction with the slow accuracy loop. This makes the final FVF architecture a suitable basis for implementation; the detailed transistor-level design, biasing strategy, and compensation approach are presented in the next chapter.

Chapter 4

FVF LDO Design

This chapter presents the design of the final PMOS FVF architecture selected at the end of Chapter 3. The design starts from the pass-device sizing, which must guarantee saturation even in the worst operating corners. The remaining degrees of freedom are then constrained by the implementation of the two control loops, which are also analyzed from a theoretical point of view to identify the sizing choices and compensation strategies required for stable operation. Simulation validation is deferred to the next chapter. Finally, this chapter also presents the adopted error amplifier and explains the main design choices behind it.

4.1 Pass Device

The pass device adopted in this design is a PMOS transistor. This choice is convenient for an LDO output stage because the PMOS can be driven directly by the control loops without requiring a charge pump, while still enabling low dropout operation.

The main drawback is that hole mobility is lower than electron mobility, so for the same delivered current a PMOS must be larger than an equivalent NMOS. In this design, the pass-device dimensions were iteratively increased until corner simulations confirmed that the device remained in saturation even under worst-case operating conditions.

Figure 4.1 shows $|V_{DS}| - V_{DSAT}$ of the pass PMOS with its final sizing versus temperature for sweeps of I_{LOAD} and other design parameters, showing the most significant traces among the many simulated cases. A PMOS transistor is in saturation when $|V_{DS}| > |V_{GS}| - |V_{TH}|$; in this work $V_{DSAT} \equiv |V_{GS}| - |V_{TH}|$, so $|V_{DS}| - V_{DSAT} > 0$ indicates saturated operation. Therefore, to ensure saturation in all simulated

conditions, every trace must remain above 0. In Fig. 4.1, the minimum point reached under the worst-case conditions is explicitly highlighted, with $(|V_{DS}| - V_{DSAT})_{\min} = 40.4\,\text{mV}$.

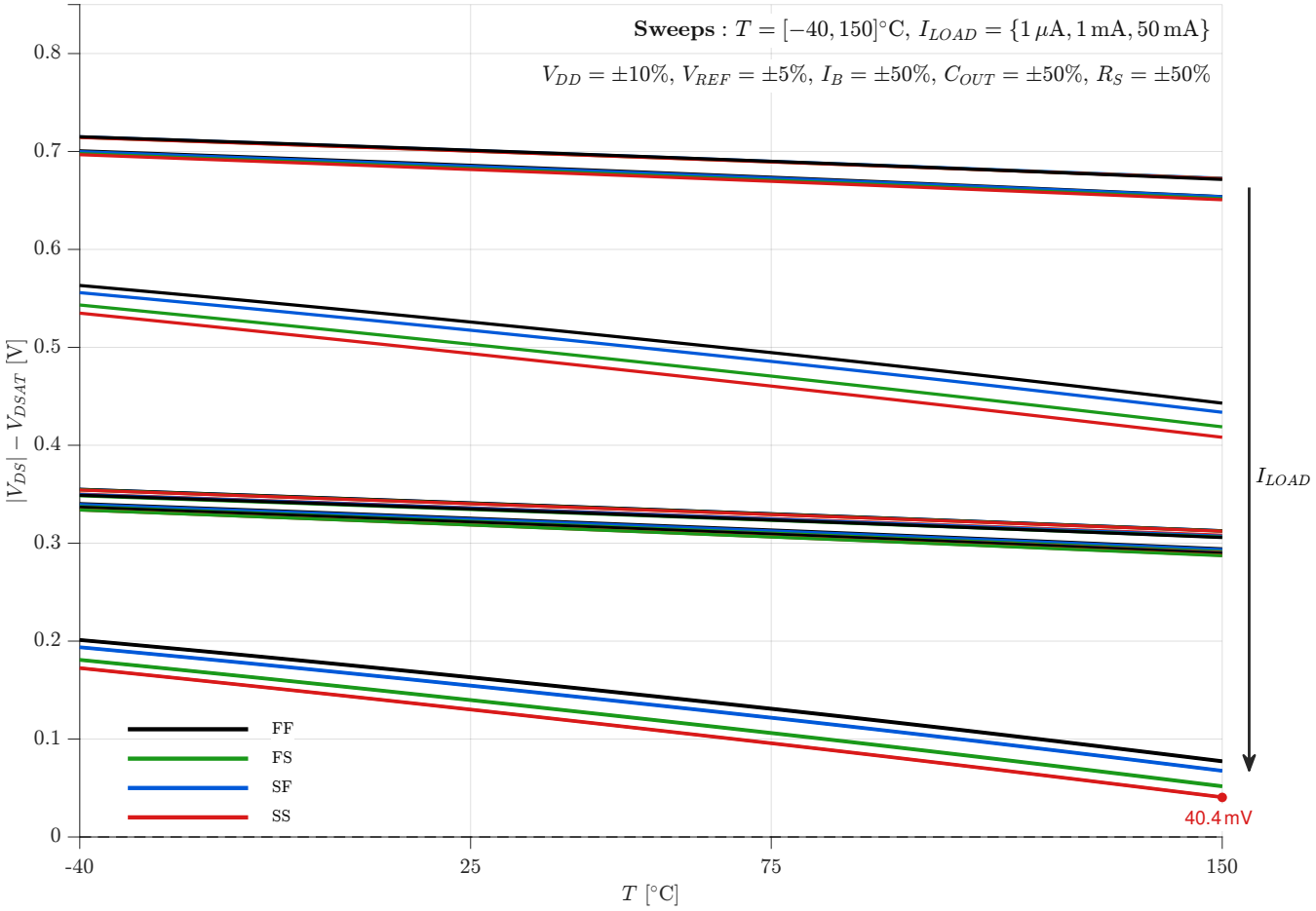


Figure 4.1: Pass-device $|V_{DS}| - V_{DSAT}$ versus temperature.

4.2 LDO Implementation

Figure 4.2 shows the architecture reached at the end of the discussion in Chapter 3 and adopted for the final design. As already anticipated in the previous chapter and visible in the figure, the regulator is a dual-loop architecture.

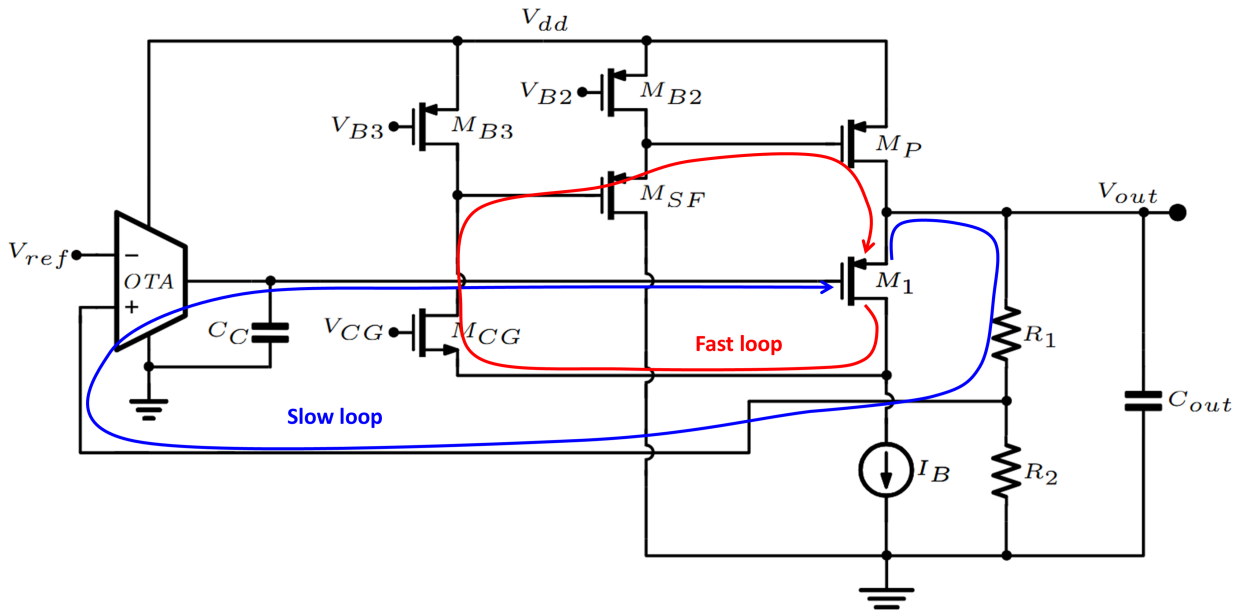


Figure 4.2: Dual-loop FVF LDO.

The slow loop is realized with the OTA, the resistive feedback network, and M_1, which acts as a source follower to regulate the DC output voltage. The fast loop is responsible for reacting to fast ac variations of V_{out}, and it is implemented through a negative-feedback action that drives the pass device. It is composed of M_1, which behaves as a common gate and samples the variation of V_{out}, M_{CG}, which is also a common-gate device, and finally the M_{SF} buffer, which drives the pass device M_P.

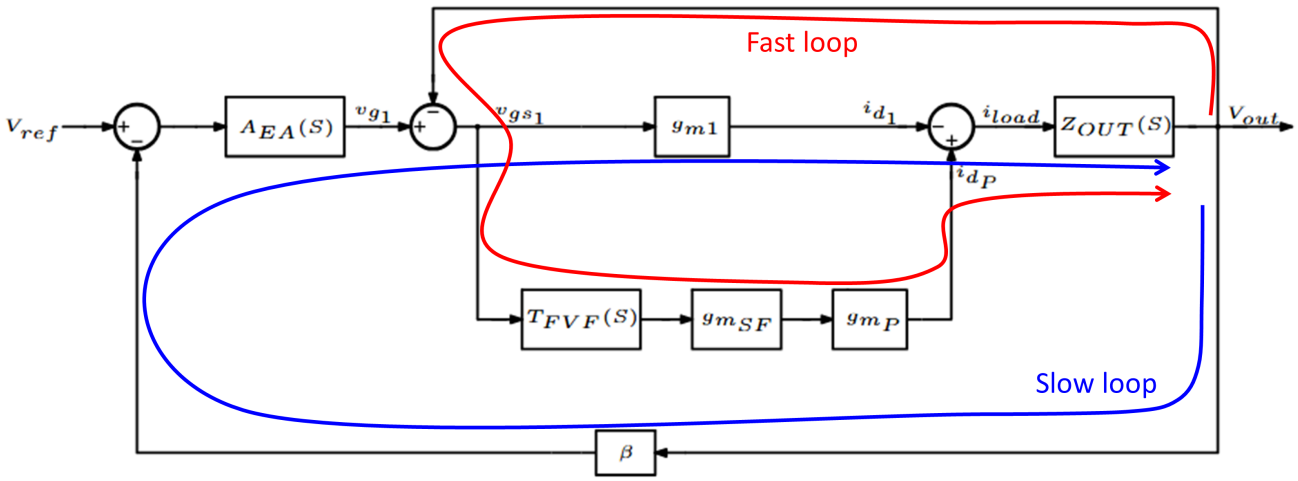


Figure 4.3: Flow diagram of the dual-loop LDO.

As also shown in Fig. 4.3, the LDO is composed of two loops. The blue loop, the slow loop, compares the output with the reference and acts on the gate of M_1. The red loop, the fast loop, acts directly on the gate of the pass device.

4.3 Fast Loop Analysis

The fast loop is based on the PMOS FVF principle described in Chapter 3. Its function is to sense rapid output-voltage deviations and quickly modify the current delivered by the pass device. During a load-current increase, the fast loop must enhance the PMOS conduction to limit undershoot. During a load-current decrease, it must reduce the delivered current to limit overshoot.

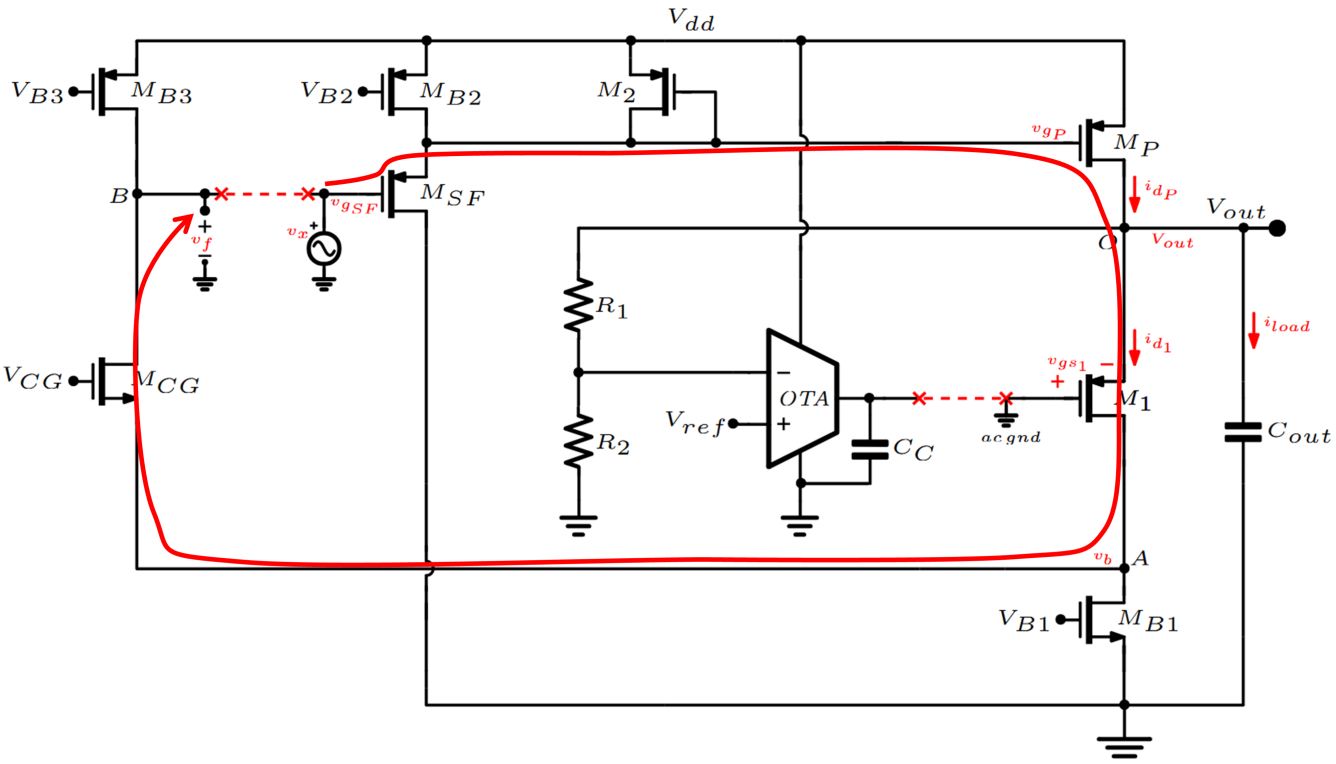


Figure 4.4: Fast Loop Schematic.

In the case of a sudden drop in the load current, i_{load}, V_{out} increases. Therefore, i_{d_1} must be increased and i_{d_P} of the pass device must be decreased. The fast-loop action can be summarized, using the signal names of Fig. 4.4, as follows:

Fast loop: $v_{out} \uparrow\ v_{gs_1} \uparrow\ i_{d_1} \uparrow\ v_b \uparrow\ v_{g_{SF}} \uparrow\ v_{g_P} \uparrow\ i_{d_P} \downarrow$

In the opposite case, after a sudden increase in i_{load}, V_{out} decreases:

Fast loop: $v_{out} \downarrow\ v_{gs_1} \downarrow\ i_{d_1} \downarrow\ v_b \downarrow\ v_{g_{SF}} \downarrow\ v_{g_P} \downarrow\ i_{d_P} \uparrow$

Since the fast-loop bandwidth is much larger than the slow-loop bandwidth, it is reasonable to assume the gate of M_1 as an ac ground during fast-loop analysis. The slow loop reacts sufficiently slowly compared with the fast-loop reaction time that it

can be treated as approximately constant:

$$\omega_{ug,\text{Slow Loop}} \ll \omega_{ug,\text{Fast Loop}}$$

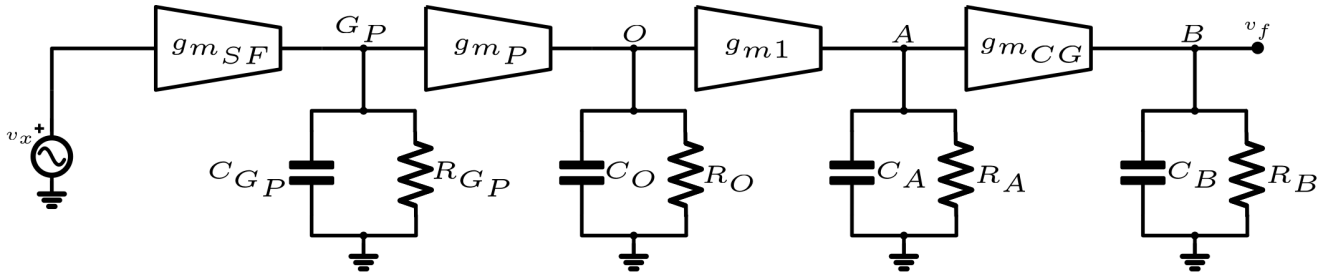


Figure 4.5: Small-signal model of the fast loop.

The fast-loop gain transfer function can be calculated by opening the loop at node B, located at the gate of the buffer, and applying the return-ratio method, as shown in Fig. 4.4, although equivalent loop openings at other nodes are also possible. The resulting transfer function is:

$$\begin{aligned} T_{FVF}(s) &= \frac{g_{mP} \cdot R_O \cdot g_{m1} \cdot R_A \cdot g_{mCG} \cdot R_B}{(1 + sR_{G_P}C_{G_P})\,(1 + sR_OC_O)\,(1 + sR_AC_A)\,(1 + sR_BC_B)} \\ &= \frac{g_{mP} \cdot R_O \cdot g_{m1} \cdot R_A \cdot g_{mCG} \cdot R_B}{(1 + s/\omega_{p_{G_P}})(1 + s/\omega_{p_O})(1 + s/\omega_{p_A})(1 + s/\omega_{p_B})} \end{aligned}$$

The resistance and capacitance values associated with each node can be approximated as follows:

$$\begin{aligned} R_{G_P} &= \frac{1}{g_{mSF}} \parallel r_{oB2} \parallel r_{o2} \approx \frac{1}{g_{mSF}} \\ C_{G_P} &= C_{gdP} + C_{gsP} + C_{gd2} + C_{gs2} + C_{gsSF} + C_{sbSF} + C_{gdB2} \approx C_{gdP} + C_{gsP} \\ R_O &= R_L \parallel r_{oP} \parallel R_F \parallel \frac{r_{oB1} + r_{o1}}{1 + g_{m1} \cdot r_{o1}} \qquad R_F = R_1 + R_2 \\ C_O &= C_L \\ R_A &= \frac{r_{oB3} + r_{oCG}}{1 + g_{mCG} \cdot r_{oCG}} \parallel r_{oB1} \parallel r_{o1} \\ C_A &= C_{gdB1} + C_{gsCG} + C_{gd1} \\ R_B &= r_{oCG} \parallel r_{oB3} \approx r_{oCG} \\ C_B &= C_{gsSF} + C_{gdSF} + C_{gdB3} + C_{gdCG} \approx C_{gsSF} + C_{gdSF} \end{aligned}$$

The DC gain is directly given by the numerator of the transfer function:

$$T_{FVF}(0) = g_{mP} \cdot R_O \cdot g_{m1} \cdot R_A \cdot g_{mCG} \cdot R_B$$

Since both g_{mP} and R_O depend on the load current i_L, the DC gain also changes with the load condition.

The denominator also provides the four poles of the fast loop. Under the first-order approximation used above, each pole is associated with one of the four relevant nodes, namely G_P, O, A, and B, and its approximate frequency is given by

$$\omega_{p_i} \simeq \frac{1}{R_i C_i}, \qquad i \in \{G_P, O, A, B\}$$

The following analysis qualitatively discusses the position of these poles and their effect on the fast-loop frequency response.

The pole associated with node G_P, namely $\omega_{p_{G_P}}$, is expected to be a high-frequency pole. The equivalent resistance at this node is very low because it is driven by the buffer M_{SF}, and can therefore be approximated as $R_{G_P} \approx 1/g_{mSF}$. The equivalent capacitance C_{G_P} is mainly determined by the parasitic capacitances of the pass device, in particular C_{gdP} and C_{gsP}. Although these capacitances can be relatively large, they are still intrinsic parasitic capacitances, so the pole remains in the GHz range. The pole frequency can therefore be approximated as

$$\omega_{p_{G_P}} = \frac{1}{R_{G_P} C_{G_P}} \approx \frac{g_{mSF}}{C_{G_P}}$$

The pole associated with node A, ω_{p_A}, is expected to be a medium-high-frequency pole. The equivalent resistance at this node is mainly determined by the output resistance of M_1 in parallel with the resistance seen looking into the source of the common-gate transistor M_{CG}. Using the expressions introduced above, it can be written as

$$R_A \approx \frac{r_{oB3} + r_{oCG}}{1 + g_{mCG} \cdot r_{oCG}} \parallel r_{o1}$$

The equivalent capacitance is relatively small because it is determined only by parasitic capacitances, namely C_{gdB1}, C_{gsCG}, and C_{gd1}, associated with M_{B1}, M_{CG}, and M_1, respectively. Therefore, the pole frequency is given by

$$\omega_{p_A} = \frac{1}{R_A C_A} = \frac{1}{\left(\dfrac{r_{oB3} + r_{oCG}}{1 + g_{mCG} \cdot r_{oCG}} \parallel r_{o1} \right) C_A}$$

The pole associated with node B, ω_{p_B}, is expected to be a medium-low-frequency pole. This node is characterized by a quite high equivalent impedance, with the resistance mainly determined by the output resistances of the common-gate transistor

and the upper biasing transistor M_{B3}. Therefore,

$$R_B = r_{oCG} \parallel r_{oB3} \approx r_{oCG}$$

The capacitance at node B is determined by the parasitic capacitances of the source-follower transistor, the common-gate transistor M_{CG}, and the upper biasing transistor M_{B3}. It can be written as

$$C_B = C_{gsSF} + C_{gdSF} + C_{gdB3} + C_{gdCG} \approx C_{gsSF} + C_{gdSF}$$

Consequently, the pole frequency is

$$\omega_{p_B} = \frac{1}{R_B C_B} \approx \frac{1}{r_{oCG}\left(C_{gsSF} + C_{gdSF}\right)}$$

Finally, the pole associated with the output node O, ω_{p_O}, is a load-dependent pole. Its frequency changes with the load current i_L, mainly through the equivalent resistance at the output node. This resistance is given by

$$R_O = R_L \parallel r_{oP} \parallel R_F \parallel \frac{r_{oB1} + r_{o1}}{1 + g_{m1} \cdot r_{o1}}, \qquad R_L \simeq \frac{V_{out}}{i_L}$$

For the maximum load current, R_L is relatively small and dominates the parallel combination, so the output resistance can be approximated as

$$R_O\Big|_{i_{L,\max}} \approx R_L$$

Since $C_O = C_L$, the corresponding output pole is

$$\omega_{p_O}\Big|_{i_{L,\max}} \approx \frac{1}{R_L C_L}$$

Conversely, for the minimum load current, R_L becomes large and its effect on the parallel combination can be neglected. In this case,

$$R_O\Big|_{i_{L,\min}} \approx R_F \parallel \frac{r_{oB1} + r_{o1}}{1 + g_{m1} \cdot r_{o1}}$$

The corresponding output pole is therefore

$$\omega_{p_O}\Big|_{i_{L,\min}} \approx \frac{1}{\left(R_F \parallel \dfrac{r_{oB1} + r_{o1}}{1 + g_{m1} \cdot r_{o1}}\right) C_L}$$

As i_L increases, the output pole shifts to a higher frequency. This behavior is critical

for the compensation design and therefore requires a zero-tracking solution able to follow the movement of the output pole.

The uncompensated fast-loop gain Bode plots at the minimum and maximum load currents are reported in Fig. 4.6. The two panels provide a qualitative view of the four pole locations and, in particular, of the movement of ω_{pO} across the load-current range.

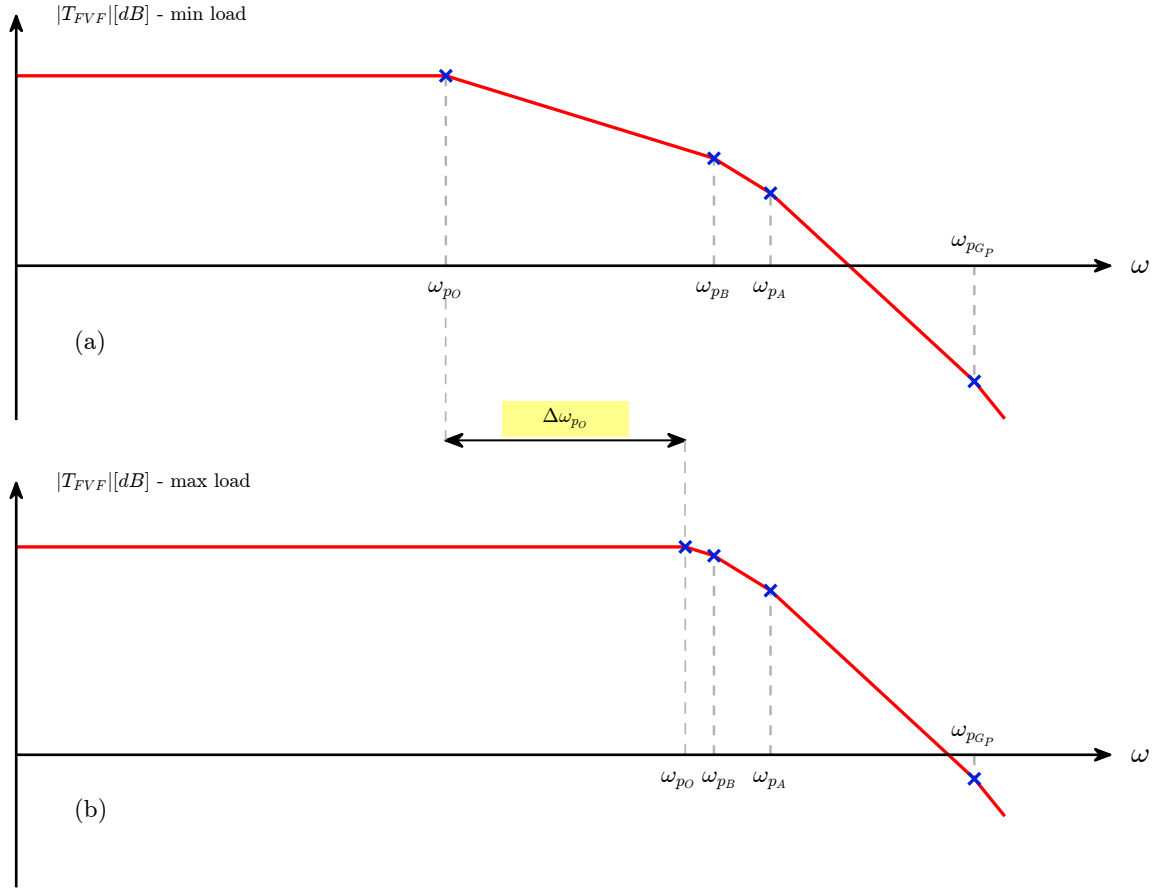


Figure 4.6: Qualitative uncompensated fast-loop gain Bode plots at minimum and maximum load.

4.4 Zero-Pole Tracking Compensation and Fast Loop Design

As can be seen in Fig. 4.6, the uncompensated fast-loop transfer function is not stable over the complete load-current range. Its stability progressively deteriorates as the load current increases, mainly because the output pole ω_{pO} moves toward higher frequency. The pole ω_{pB} is already present in the medium-to-low-frequency range. A first possible compensation strategy is therefore to make this pole dominant by adding a large

capacitance at node B, so that lowering ω_{p_B} also lowers the unity-gain frequency:

$$\omega_{ug} \ll \omega_{p_O}(I_L), \qquad I_L \in [I_{L,\min}, I_{L,\max}]$$

However, as illustrated in Fig. 4.7, this solution would excessively reduce the bandwidth of the fast loop and is therefore not suitable when a wide bandwidth is required.

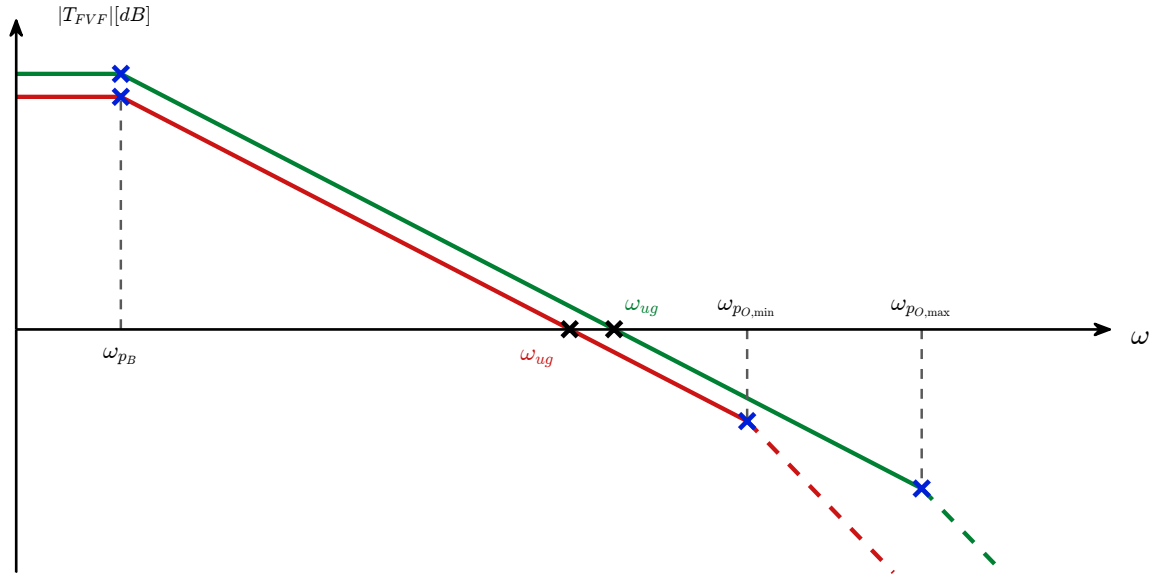


Figure 4.7: Qualitative T_{FVF} Bode plot for the fast loop with dominant pole compensation.

Another possible solution is to introduce a zero at the frequency of the minimum-load output pole, while keeping ω_{p_B} as the dominant pole before $\omega_{p_{O,\min}}$. This arrangement provides a larger bandwidth than the previous solution. However, as I_L increases, the output pole ω_{p_O} moves toward higher frequencies, while the zero remains fixed near $\omega_{p_{O,\min}}$. Given the very high DC gain, the loop is already close to its stability limit under minimum-load conditions. As I_L increases, the output pole moves even further from the fixed zero, eventually making the loop completely unstable, as shown in Fig. 4.8.

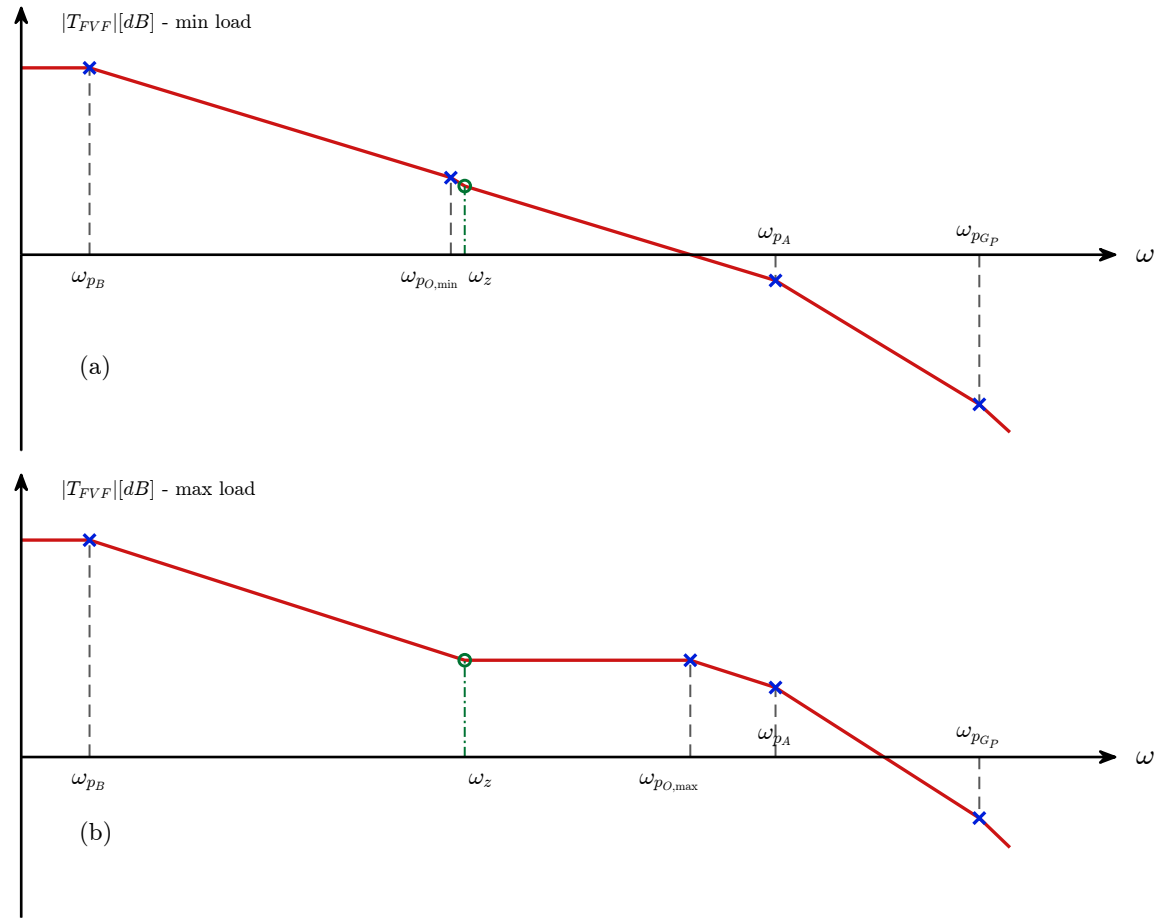


Figure 4.8: Qualitative fast-loop Bode plots with a fixed zero near $\omega_{p_{O,\min}}$: (a) minimum load and (b) maximum load.

Therefore, to compensate the fast loop while ensuring both stability and a wide bandwidth, the compensation zero must be able to track the movement of the output pole ω_{p_O} caused by changes in the load current I_L. As can be seen in Fig. 4.9, the bandwidth can therefore be maximized under both minimum- and maximum-load conditions.

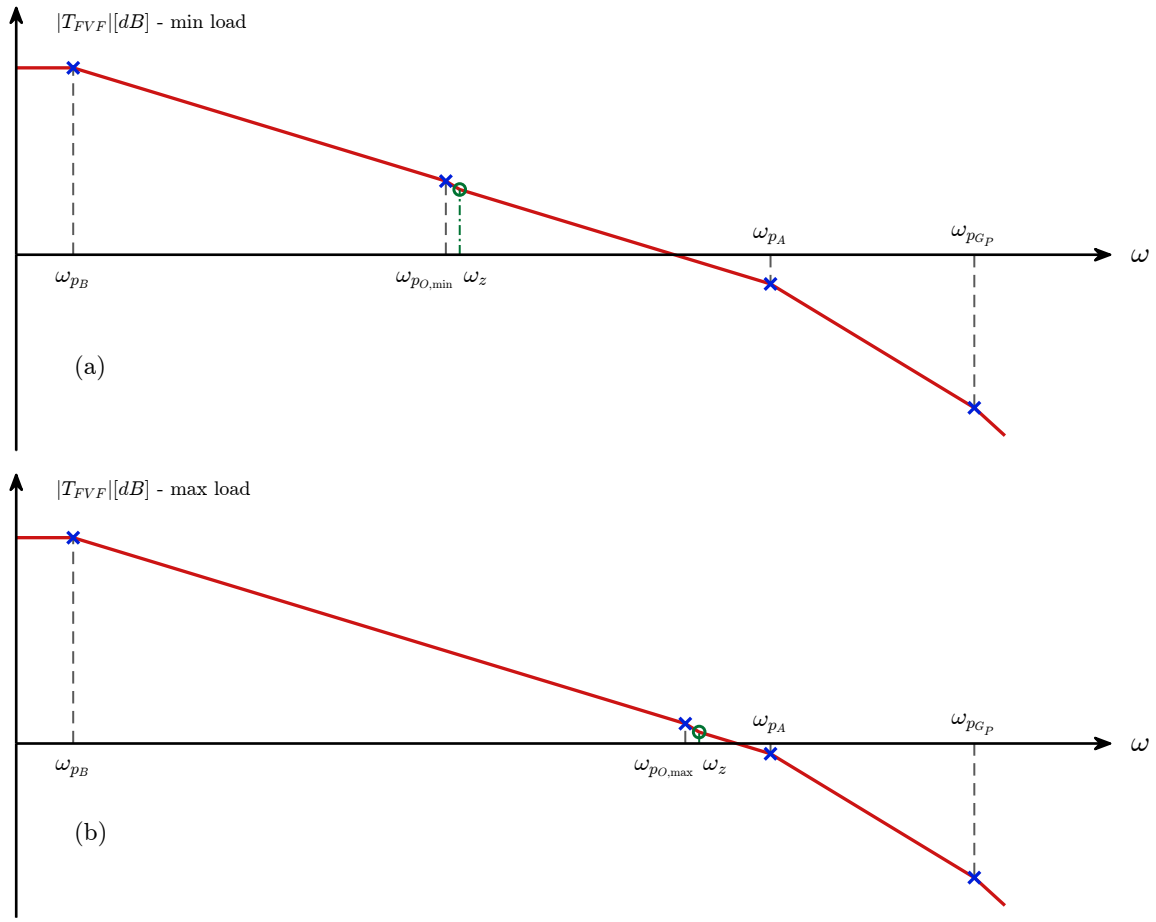


Figure 4.9: Qualitative fast-loop Bode plots with an output-pole-tracking zero: (a) minimum load and (b) maximum load.

Using the compensation technique shown in Fig. 4.10, it is possible to obtain both the compensation zero and set ω_{p_B} as the dominant pole within the same structure, which can be achieved by modifying the impedance seen at node B.

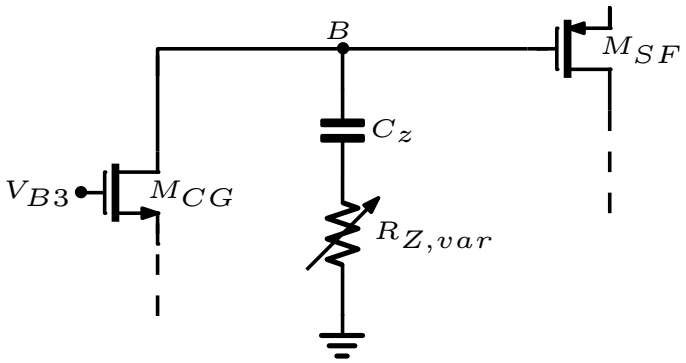


Figure 4.10: Qualitative compensation of node B.

With this modification, the dominant pole at node B can be approximated as

$$\omega_{p_B} \simeq \frac{1}{C_Z \cdot [R_{Z,\text{var}} + r_{oCG}]}$$

The variable resistance $R_{Z,\text{var}}$ also creates a zero at a variable frequency, given by

$$\omega_z = \frac{1}{C_Z \cdot R_{Z,\text{var}}}$$

Therefore, the zero frequency can be controlled by trimming $R_{Z,\text{var}}$. The objective is to make this zero follow the behavior of the output pole ω_{p_O}, which changes with I_{Load}. This requires a circuit capable of making $R_{Z,\text{var}}$ depend on the load current as well.

Using the equivalent output resistance defined above, the output pole can be expressed as a function of the load current as

$$\omega_{p_O} = \frac{1}{R_O \cdot C_L}, \qquad R_O = R_L \parallel r_{oP} \parallel R_F \parallel \frac{r_{oB1} + r_{o1}}{1 + g_{m1} \cdot r_{o1}}$$

To obtain the resistance range required for zero–pole tracking, the zero frequency can be matched to the output pole one load condition at a time. At minimum load, the output resistance is approximated by the parallel combination defined above. Specifically,

$$R_O(I_{L,\text{min}}) \simeq R_F \parallel \frac{r_{oB1} + r_{o1}}{1 + g_{m1} \cdot r_{o1}}$$

Therefore,

$$\omega_{p_{O,\text{min}}} = \frac{1}{\left(R_F \parallel \dfrac{r_{oB1} + r_{o1}}{1 + g_{m1} \cdot r_{o1}}\right) \cdot C_L} = \omega_z(I_{L,\text{min}})$$

Since $\omega_z(I_L) = 1/[C_Z \cdot R_Z(I_L)]$, the corresponding resistance is

$$R_Z(I_{L,\text{min}}) = \frac{\left(R_F \parallel \dfrac{r_{oB1} + r_{o1}}{1 + g_{m1} \cdot r_{o1}}\right) \cdot C_L}{C_Z}$$

At maximum load, the output resistance is approximated by R_L. The corresponding condition is

$$\omega_{p_{O,\text{max}}} = \frac{1}{R_L \cdot C_L} = \omega_z(I_{L,\text{max}})$$

which gives

$$R_Z(I_{L,\max}) = \frac{R_L \cdot C_L}{C_Z}$$

Therefore, the required resistance range is

$$R_{Z,\min} = R_Z(I_{L,\max}) \leq R_Z(I_L) \leq R_Z(I_{L,\min}) = R_{Z,\max}$$

where $R_{Z,\min}$ corresponds to the maximum load current and $R_{Z,\max}$ to the minimum load current. It is therefore necessary to find a circuit that provides a resistance with these characteristics. A simple way to obtain it is to use a fixed resistance $R_{Z,\text{fix}}$ in parallel with a variable resistance $R_Z(I_L)$ that decreases as the load current increases:

$$R_{Z,\text{eq}}(I_L) = R_{Z,\text{fix}} \parallel R_Z(I_L)$$

At minimum load, $R_Z(I_L)$ is much larger than $R_{Z,\text{fix}}$, so the total resistance is approximately set by the fixed branch and is close to $R_{Z,\max}$. As the load current increases, $R_Z(I_L)$ decreases and progressively becomes the dominant branch of the parallel combination. The resulting resistance can therefore be reduced down to $R_{Z,\min}$, allowing the compensation zero to track the movement of the output pole over the full load-current range.

Consequently, the resistance is implemented as shown in Fig. 4.11a, using a fixed resistor in parallel with the MOS transistor M_Z operated in the triode region. The MOS transistor provides the variable contribution $R_Z(I_L)$, so that the total resistance is

$$R_{Z,\text{tot}}(I_L) = R_{Z,\text{fix}} \parallel R_Z(I_L)$$

This pole-tracking compensation scheme works together with the adaptive current-biasing scheme, as shown in Fig. 4.11b. As the load current increases, the sensor voltage V_S increases, reducing the resistance of the MOS resistor M_Z. Because the zero-current condition could also represent an equilibrium point, the start-up transistor M_{B3} was required to prevent the circuit from remaining in this state. Its action guarantees that the zero-tracking mechanism starts correctly and remains functional during operation.

The sizing of the two branches can therefore be determined by analyzing $R_{Z,\text{tot}}(I_L)$.

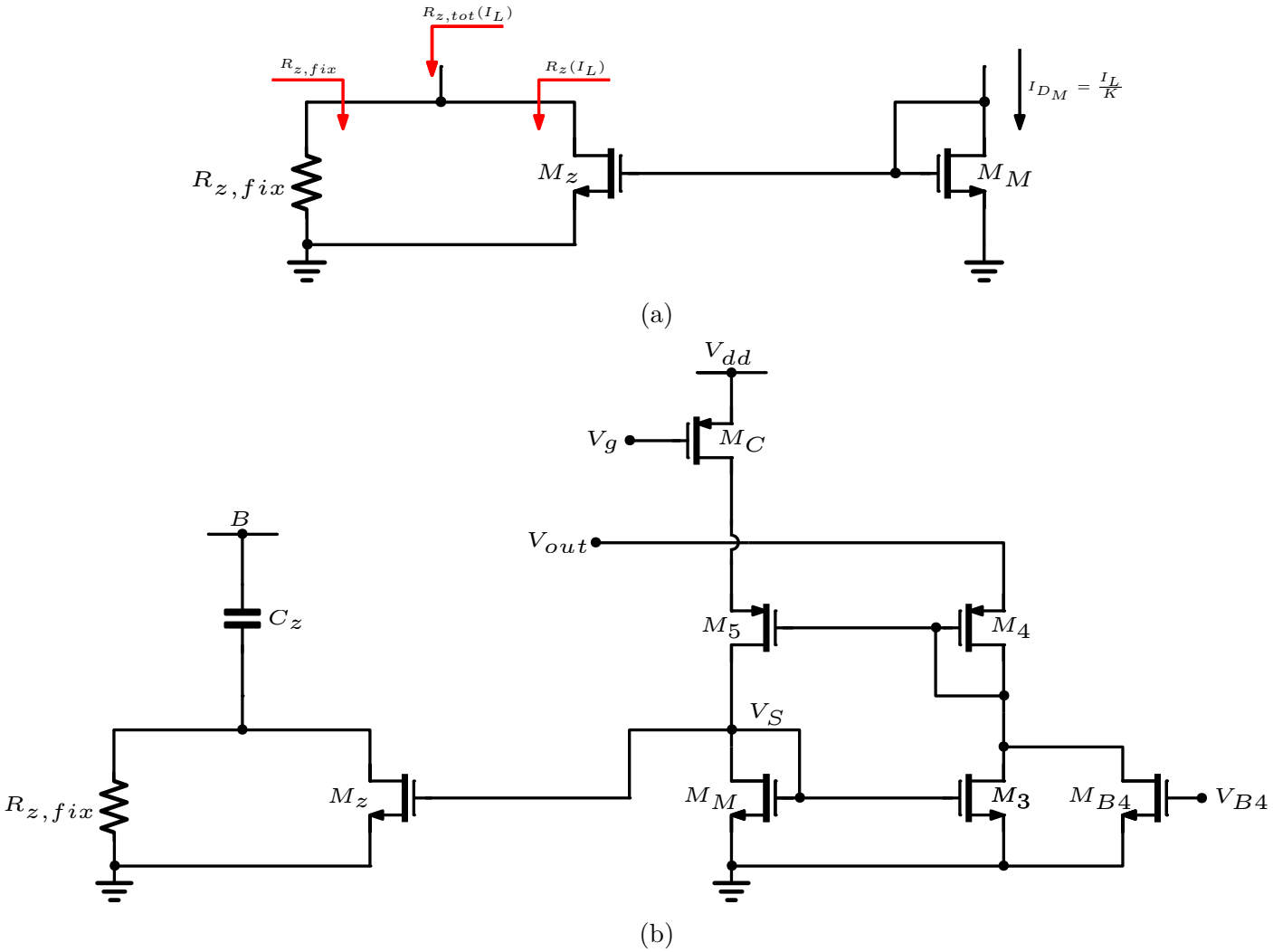


Figure 4.11: Zero-tracking compensation network: (a) variable resistor implementation and (b) complete zero-tracking schematic.

Since the gate-source voltages of M_Z and the current-setting transistor M_M are equal, the required gate voltage can be written as

$$V_{GS,Z} = V_{GS,M} = V_{TH,n} + \sqrt{\frac{2 \cdot I_{D_M}}{K_n' \cdot (W_M/L_M)}}$$

Using this bias condition in the triode-region expression for M_Z gives

$$R_Z(I_L) = \frac{1}{\sqrt{K_n'} \cdot \frac{W_Z}{L_Z} \cdot \sqrt{\frac{2 \cdot I_{D_M}}{W_M/L_M}}} = \frac{\beta}{\sqrt{I_{D_M}}}$$

where the proportionality factor is

$$\beta = \frac{L_Z \cdot \sqrt{W_M}}{W_Z \cdot \sqrt{2 \cdot K_n' \cdot L_M}}$$

The current of the bias transistor is set by the load current according to

$$I_{D_M} = \frac{I_L}{K}$$

This current is generated by the copy transistor M_C, which is a much smaller replica of the pass device M_P. Since M_C and M_P share the same gate voltage V_G, the current through M_C is a scaled replica of the load current, with the scaling factor set by their device dimensions. This replica current is used to provide the adaptive biasing of M_Z as the load current changes. Accordingly, the scaling factor is

$$K = \frac{(W_P/L_P)}{(W_C/L_C)}$$

which reduces to $K = W_P/W_C$ when the two devices have the same channel length.

Therefore, the two free parameters that must be fixed during the design are $R_{Z,\text{fix}}$ and β. By imposing the desired ideal resistance $R_{Z,\text{ideal}}(I_L)$ on the total resistance, the required sizing condition is

$$R_{Z,\text{tot}}(I_L) = R_{Z,\text{fix}} \parallel R_Z(I_L) = \frac{R_{Z,\text{fix}} \cdot \beta}{\beta + R_{Z,\text{fix}} \cdot \sqrt{I_{D_M}}} = R_{Z,\text{ideal}}(I_L)$$

The fixed resistance determines the value of the total resistance at the minimum load. Its value can therefore be obtained by matching the zero generated by the fixed branch to the minimum-load output pole:

$$\omega_z(I_{L,\text{min}}) = \frac{1}{C_Z \cdot R_{Z,\text{fix}}} = \omega_{p_{O,\text{min}}} = \frac{1}{\left(R_F \parallel \dfrac{r_{oB1} + r_{o1}}{1 + g_{m1} \cdot r_{o1}}\right) \cdot C_L}$$

which gives

$$R_{Z,\text{fix}} = \frac{\left(R_F \parallel \dfrac{r_{oB1} + r_{o1}}{1 + g_{m1} \cdot r_{o1}}\right) \cdot C_L}{C_Z}$$

At maximum load, the zero is matched to the maximum-load output pole according to

$$\omega_z(I_{L,\text{max}}) = \frac{1}{C_Z \cdot R_{Z,\text{tot}}(I_{L,\text{max}})} = \omega_{p_{O,\text{max}}} = \frac{1}{R_L \cdot C_L}$$

Therefore,

$$R_{Z,\text{tot}}(I_{L,\max}) = \frac{R_L \cdot C_L}{C_Z}$$

Substituting the total-resistance expression and $I_{D_M} = I_L/K$ gives

$$\frac{R_L \cdot C_L}{C_Z} = \frac{R_{Z,\text{fix}} \cdot \beta}{\beta + R_{Z,\text{fix}} \cdot \sqrt{I_{L,\max}/K}}$$

It is therefore possible to determine the proportionality factor β as

$$\beta = \frac{R_{Z,\text{fix}} \cdot \dfrac{C_L}{C_Z} \cdot \sqrt{I_{L,\max}/K}}{\dfrac{R_{Z,\text{fix}}}{R_L} - \dfrac{C_L}{C_Z}}$$

Ideally, the proportionality factor would be a function of the load current, $\beta = \beta(I_L)$, so that the resistance could track the output pole perfectly over the entire operating range. This is not possible in the present implementation, because β is a proportionality factor fixed by the geometry of the devices, as shown by its definition above. Perfect pole tracking is therefore not achievable. However, the shape of the $R_{Z,\text{tot}}(I_L)$ characteristic can be adjusted by changing the device dimensions and, consequently, the value of β. In this way, the actual characteristic can be made as close as possible to the ideal one, as shown in Fig. 4.12.

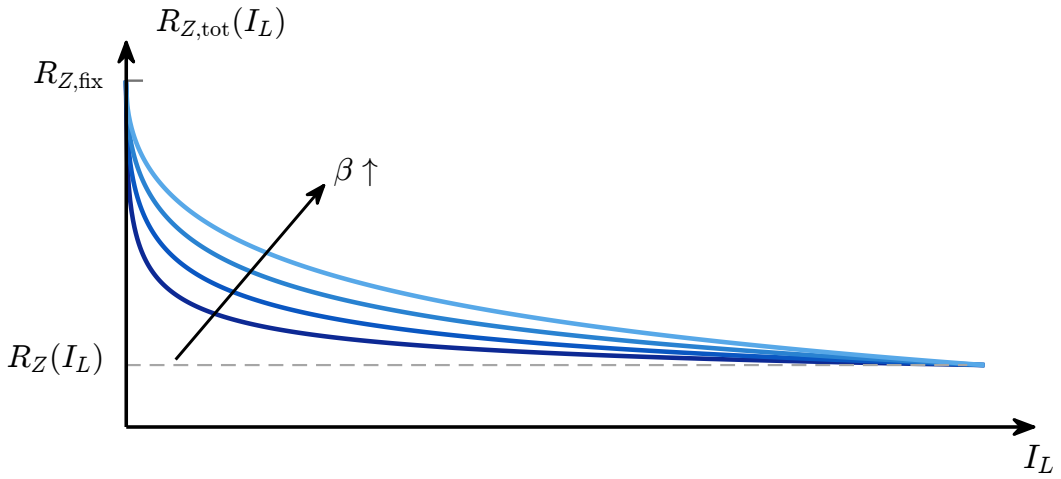


Figure 4.12: $R_{Z,\text{tot}}$ vs I_L for different values of β.

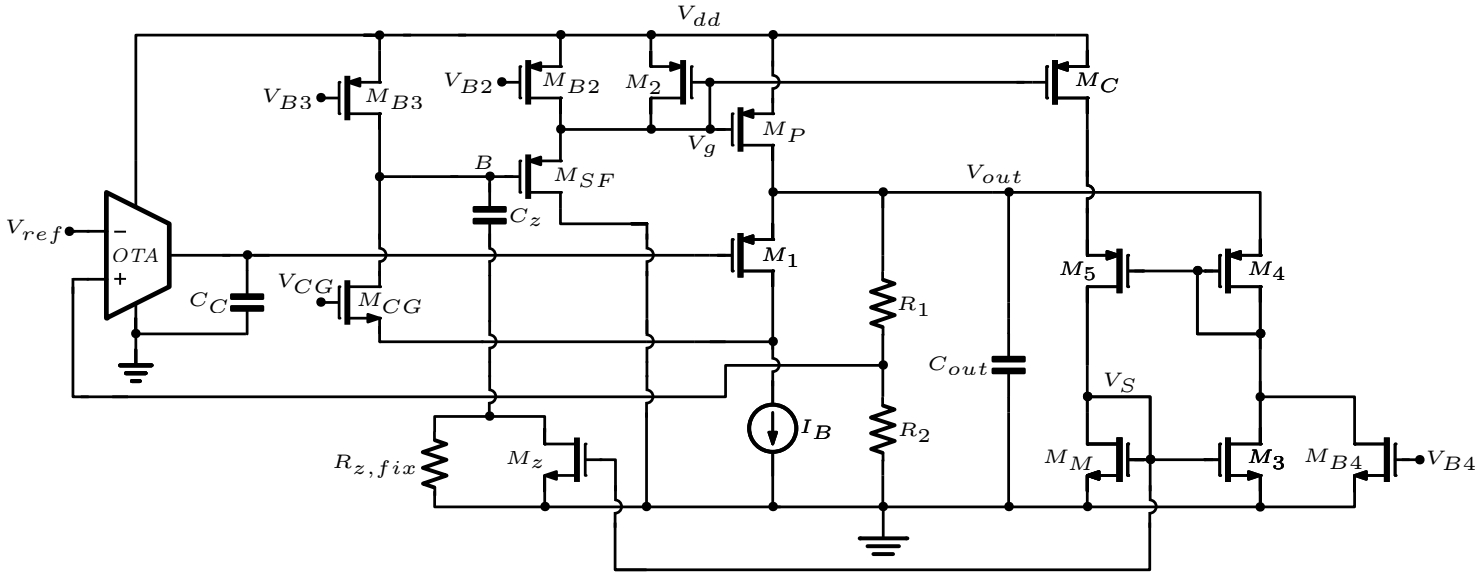


Figure 4.13: Final schematic of the proposed PMOS FVF LDO.

The resulting schematic, including the compensation network, is shown in Fig. 4.13. With this implementation, the design of the fast regulation loop and its compensation is complete.

4.5 Slow Loop Analysis

As already discussed, the slow loop shown in Fig. 4.14 is used to set the DC output voltage. It includes the reference, the folded error amplifier and the resistive divider. At low frequency, the loop gain reduces the effect of reference mismatch, feedback error, finite pass-device output resistance, line regulation, and load regulation. It operates by comparing V_{ref} and V_{out} through the resistive divider. M_1 acts as a source follower with approximately fixed v_{gs1}, so the slow loop behaves as a negative-feedback loop controlled by the error amplifier. Since M_1 is a source follower, the relation can be written as

$$V_{out} = V_{o,ota} + v_{gs1} = V_{ref} \cdot \frac{R_1 + R_2}{R_2}$$

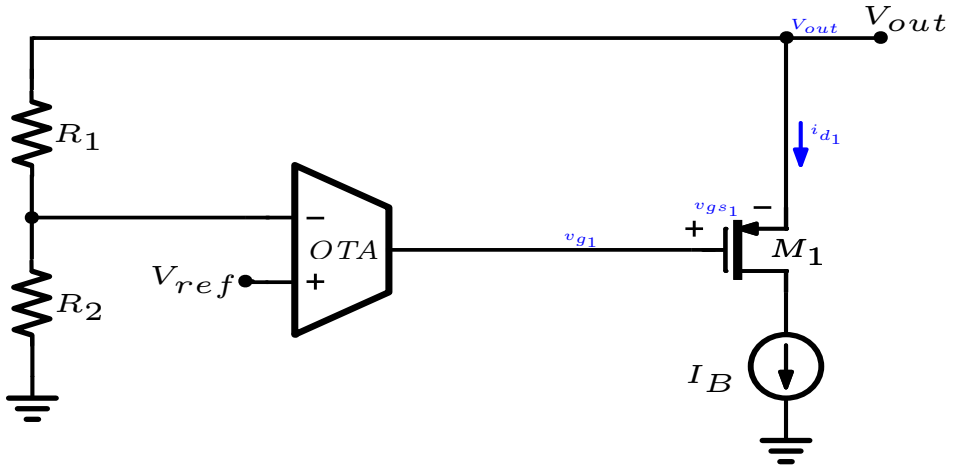


Figure 4.14: Slow-loop path of the dual-loop LDO.

In the case of a sudden drop in the load current, i_{load}, V_{out} increases. Therefore, i_{d1} must be increased and i_{dP} of the pass device must be decreased. The slow-loop action can be summarized, using the signal names of Fig. 4.2, as follows:

Slow loop: $v_{out} \uparrow \; v_{g1} \downarrow \; v_{gs1} \uparrow \; i_{d1} \uparrow$

In the opposite case, after a sudden increase in i_{load}, V_{out} decreases, so it is necessary to increase i_{dP} and decrease i_{d1}:

Slow loop: $v_{out} \downarrow \; v_{g1} \uparrow \; v_{gs1} \downarrow \; i_{d1} \downarrow$

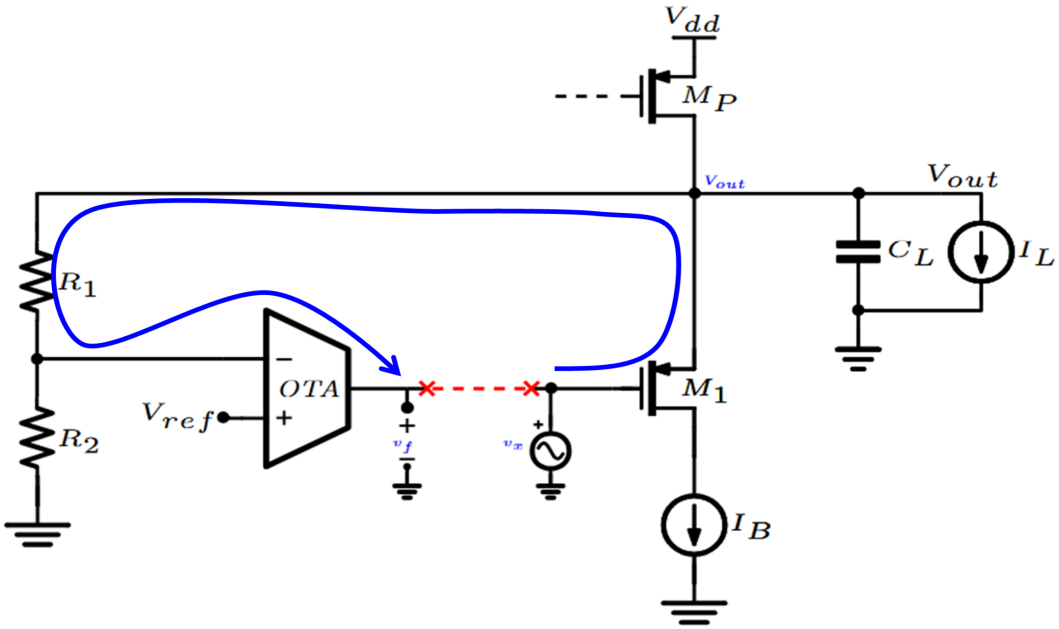


Figure 4.15: Slow-loop schematic.

Starting from the slow-loop scheme in Fig. 4.15, the loop transfer can be written as

$$T_{TOT}(s) = -\frac{v_r}{v_t} = -\frac{v_r}{v_{out}} \cdot \frac{v_{out}}{v_t} = A_{EA}(s) \cdot \frac{R_2}{R_1 + R_2} \cdot \frac{v_{out}}{v_t}$$

It is also possible to derive an expression for v_{out} by applying KCL at the output node:

$$v_{out} = (i_{d1} - i_{dP})\, Z_{OUT,FVF}(s)$$

It is then possible to obtain the following transfer function:

$$T_{TOT}(s) = T_{EA}(s) \cdot \frac{g_{mP} T_{FVF}(s) - g_{m1}}{g_{mP} T_{FVF}(s) - g_{m1} + \frac{1}{Z_{OUT,FVF}(s)}}$$

where $T_{FVF}(s)$ corresponds to the transfer function of the fast loop.

When deriving the slow-loop transfer function $T_{TOT}(s)$, it is important to remember that the fast loop is still active. Its local feedback action reduces the output impedance seen at the regulated node, so $Z_{OUT,FVF}(s)$ must be explicitly included in the derivation.

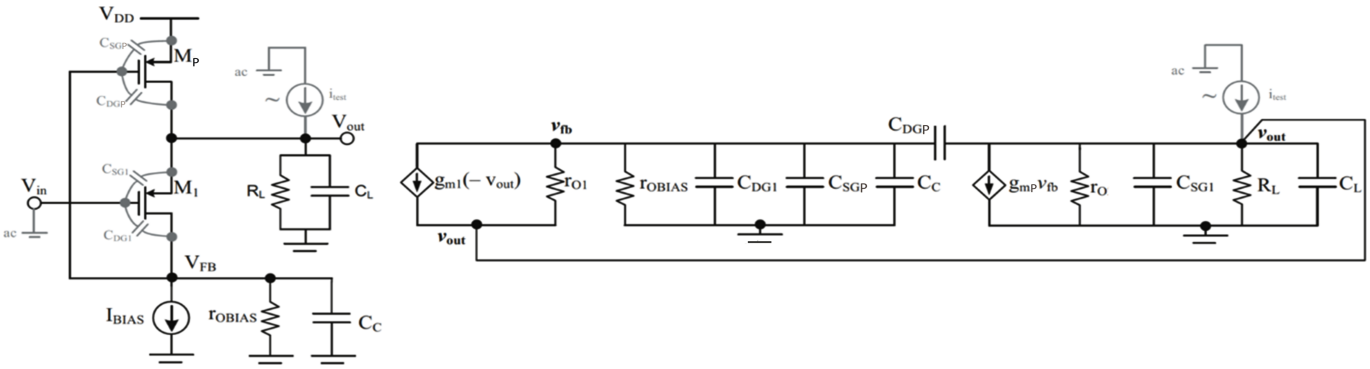


Figure 4.16: Simplified equivalent circuit used to find the FVF output impedance.

Under the assumptions of Fig. 4.16, the FVF output impedance can be approximated as:

$$Z_{out,FVF}(s) \cong \frac{(1 + s\,(r_{O1} \parallel r_{OBIAS})\,(C_{FB} + C_{GDP}))}{g_{m1}\, r_{O1}\, g_{mP}\Big(1 + \Big(\frac{C_{FB}}{g_{mP}} + \frac{C_L}{g_{m1} g_{mP} (r_{O1} \| r_{OBIAS})}\Big)\, s + \Big(\frac{C_{FB} C_L}{g_{m1} g_{mP}}\Big)\, s^2\Big)}$$

For the OTA, a first-order approximation can be used:

$$A_{EA}(s) = \frac{A_{EA,0}}{(1 + sR_{O,EA}C_{O,EA})} = \frac{A_{EA,0}}{(1 + s/\omega_{pg1})}$$

which is a valid model for a well-compensated OTA.

To estimate the DC value of the slow loop, $T_{TOT}(s)$ can be evaluated at zero

frequency ($s = 0$), obtaining the DC slow-loop gain:

$$T_{TOT,0} = T_{EA}(0) \cdot \frac{g_{mP} \cdot T_{FVF,0} - g_{m1}}{g_{mP} \cdot T_{FVF,0} - g_{m1} + \frac{1}{Z_{OUT,FVF}(0)}}$$

with $T_{FVF,0} \equiv T_{FVF}(0)$.

This DC gain is of interest since it determines the steady-state error ε_S of the regulator through the following relation:

$$V_{OUT} = \frac{V_{REF}}{\beta}\left(1 - \frac{1}{1 + T_{TOT,0}}\right) = \frac{V_{REF}}{\beta}\left(1 - \varepsilon_S\right), \qquad \beta = \frac{R_2}{R_1 + R_2}$$

which directly relates the DC loop gain to the steady-state output accuracy. Since the fast loop provides a very high DC gain through its three gain stages, $T_{FVF,0}$ is sufficiently large that

$$g_{mP} \cdot T_{FVF,0} \gg g_{m1}, \qquad g_{mP} \cdot T_{FVF,0} \gg \frac{1}{Z_{OUT,FVF}(0)}$$

Under these conditions, the ratio can be approximated as

$$\frac{g_{mP} \cdot T_{FVF,0} - g_{m1}}{g_{mP} \cdot T_{FVF,0} - g_{m1} + \frac{1}{Z_{OUT,FVF}(0)}} \approx 1$$

and the total DC loop gain can therefore be written as

$$T_{TOT,0} \approx T_{EA}(0) \approx A_{EA,0} \cdot \beta$$

The transfer function $T_{TOT}(s)$ is difficult to treat analytically with respect to the frequency response. It is therefore evaluated numerically. The resulting response exhibits first-order system behavior dominated by the slow-loop pole ω_{pg1} at the output of the OTA, which is the stage providing the high DC gain. The response does not show significant differences between minimum and maximum load current because

$$\omega_{ug,\text{SLOW LOOP}} \ll \omega_{ug,\text{FAST LOOP}}, \qquad \forall\, i_L \in [I_{L,\min}, I_{L,\max}]$$

The qualitative Bode plot of the slow loop is reported in Fig. 4.17.

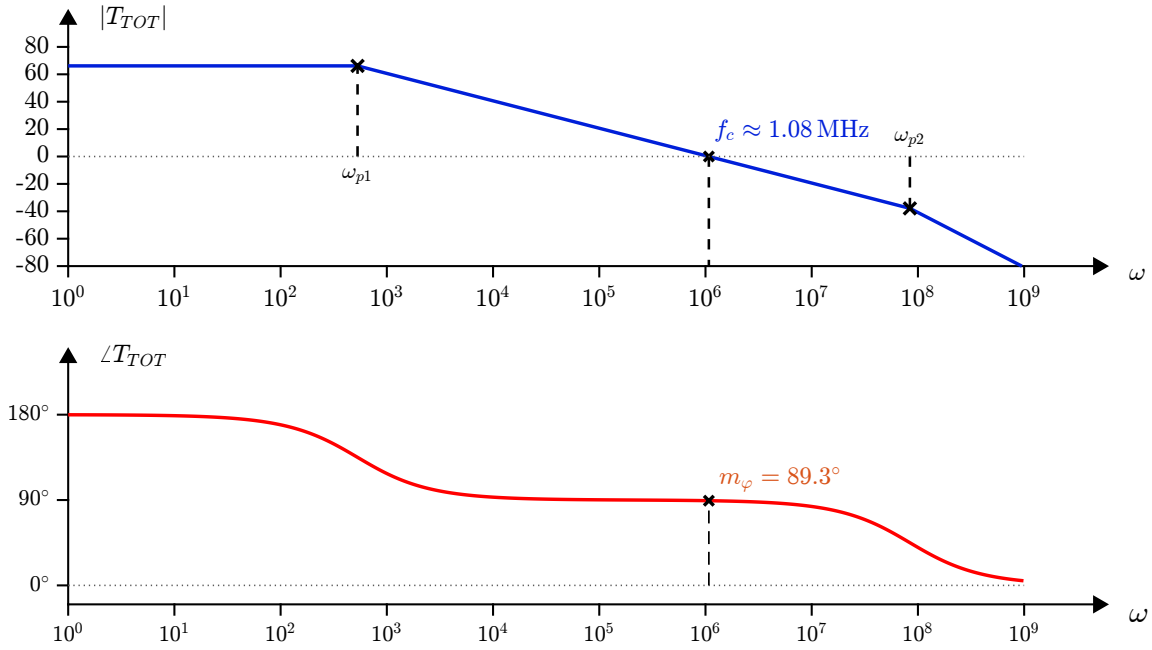


Figure 4.17: Qualitative Bode plot of the slow loop.

4.6 Error Amplifier Analysis

The error amplifier belongs to the slow regulation loop. Its task is to compare the feedback voltage with the reference voltage and to define the long-term gate or control bias required to obtain the nominal output voltage.

The amplifier must provide sufficiently high DC gain to minimize the static output error of the regulator.

For this design, a folded-cascode OTA was selected, as shown in Fig. 4.18.

A folded-cascode topology is attractive because it can provide high voltage gain while accommodating the input common-mode range and output swing constraints of a low-voltage PMOS LDO. At the same time, its power efficiency can remain comparable to that of a current-mirror OTA. With the selected sizing, a DC gain greater than 90 dB was obtained. The main limitation is that all transistors must operate in saturation, which requires

$$|V_{DS}| > |V_{GS}| - |V_{TH}|$$

regardless of whether the devices operate in weak or strong inversion.

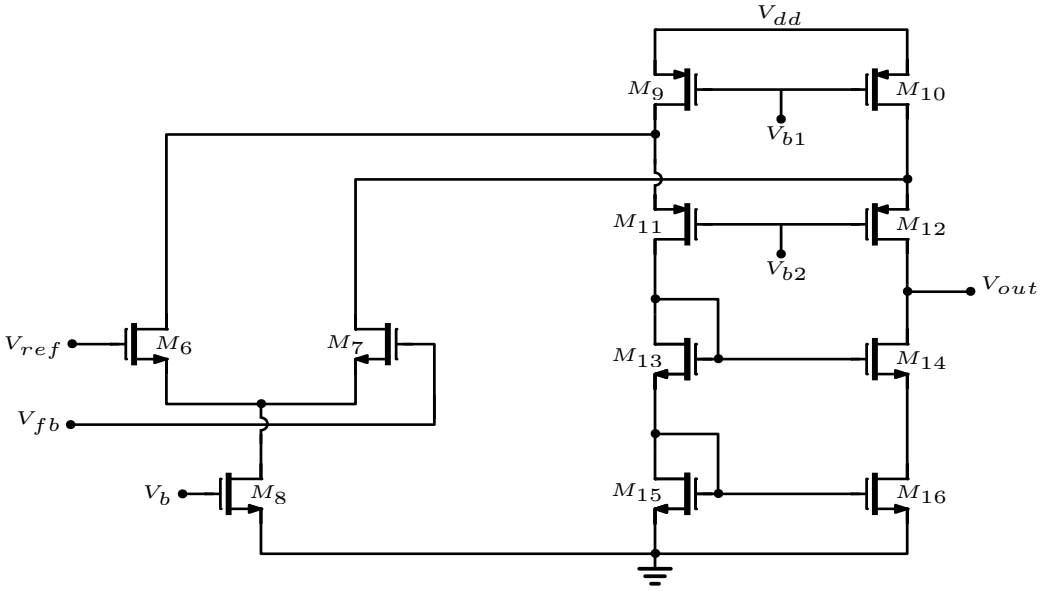


Figure 4.18: Folded-cascode error amplifier schematic.

After sizing the MOSFETs and running corner simulations, it was observed that the PMOS devices M_{11} and M_{12} did not reach saturation in some corners. Therefore, one cascoding structure, formed by M_{15} and M_{16}, was removed from the final implementation to ensure saturation across the considered corners. This change provided a more robust operating point for the error amplifier, at the cost of a reduction in DC gain.

The final implementation of the OTA used in the slow regulation loop is shown in Fig. 4.19.

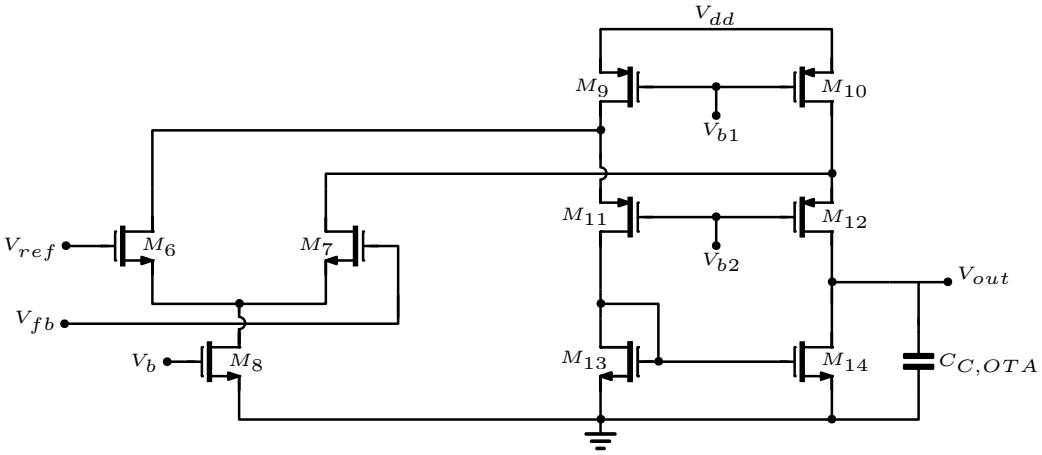


Figure 4.19: Final OTA implementation used in the slow regulation loop.

As discussed in Section 4.5, the DC gain of the slow loop, expressed in linear terms, is approximately three quarters of the OTA DC gain:

$$T_{TOT}(0) \approx 0.75 \cdot A_{EA,0}$$

which corresponds to a reduction of approximately 2.5 dB. Therefore, the folded-cascode OTA was sized to provide a DC gain between approximately 65 and 70 dB, so that the resulting slow-loop DC gain remains within the required range. The DC gain of the OTA can be estimated as

$$A_{DC} \approx g_{m7} \cdot R_{OUT} \qquad R_{OUT} = (g_{m12} \cdot r_{o12} \cdot r_{o10}) \parallel r_{o14} \approx r_{o14}$$

The dominant pole of the OTA is set by the output resistance and capacitance. Using the same first-order approximation, its angular frequency is

$$\omega_{p,\text{out}} \approx \frac{1}{R_{OUT} C_{OUT}}$$

For a single-dominant-pole OTA, the gain-bandwidth product can be estimated as

$$GBW \approx \frac{g_{m7}}{2\pi C_{OUT}}$$

The compensation capacitor $C_{C,\text{OTA}}$ was therefore added to reduce the GBW of the OTA and, consequently, the crossover frequency of the slow loop. This keeps the slow and fast loops sufficiently separated in frequency and prevents them from interfering with each other.

Figure 4.20 reports the simulated loop-gain Bode response of the adopted OTA, used as a reference for the slow-loop design trade-offs discussed in this chapter.

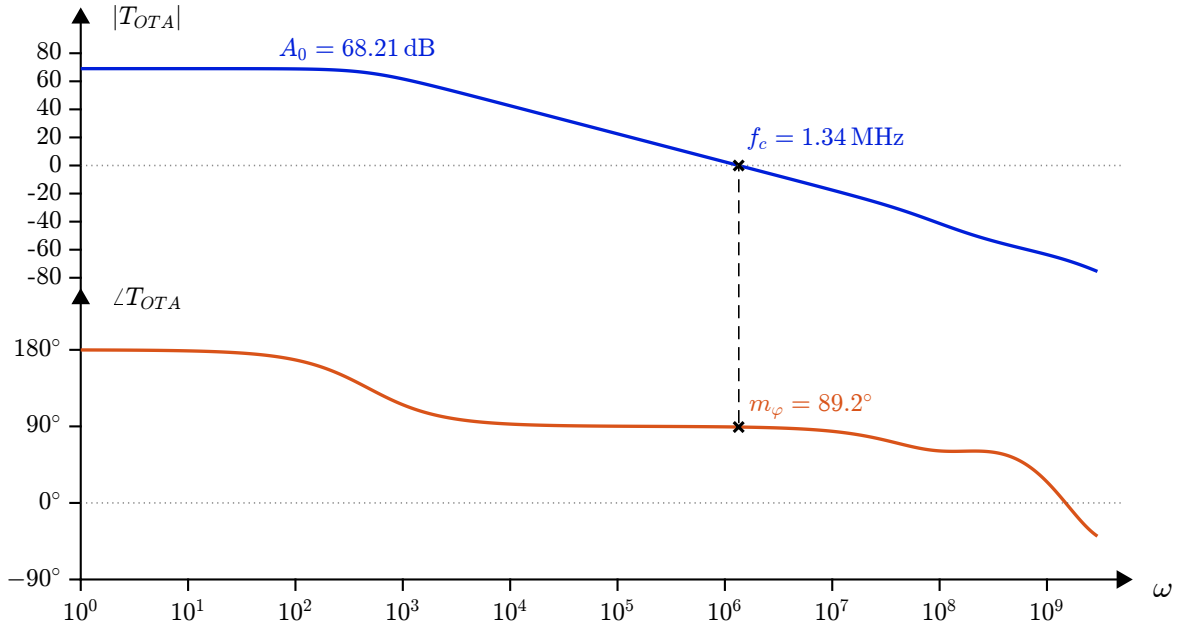


Figure 4.20: Loop-gain Bode plot of the adopted OTA used in the slow regulation loop.

4.7 Parasitics Analysis

The supply terminals of a packaged LDO are connected to the external source through a physical interconnect network rather than ideal voltage sources. Parasitic elements along the path from the board to the die therefore affect the voltage at the on-chip supply pads. This applies to both the positive supply, V_{DD}, and the return path, V_{SS}, since a disturbance at either terminal changes the supply voltage seen by the regulator.

For the V_{DD} path, the current flows from the board supply through the PCB trace and its connection to the package pin, and then from the pin to the corresponding pad on the die. The board-to-pin section contributes the so-called board parasitics, namely trace resistance, inductance, and distributed capacitance to nearby conductors and the reference plane. The pin-to-pad section adds package and bondwire parasitics, including the finite resistance and inductance of the bondwire. Consequently, the external supply is coupled to the integrated circuit through a frequency-dependent impedance rather than through an ideal short circuit.

The V_{SS} connection must be considered in the same way. The return current leaves the on-chip ground pad through the bondwire and package pin, then flows through the board connection and the ground plane before reaching the external source. The resistance of this path produces a current-dependent voltage drop, while its inductance generates a transient voltage when the return current changes rapidly. The resulting ground bounce shifts the local reference of the LDO and can therefore appear as an additional error at both the input and the output of the regulator. The parasitic elements affecting both supply paths are illustrated in Fig. 4.21.

The relative importance of the parasitic components depends on frequency. At low frequency, the resistive elements cause an IR drop that degrades the DC accuracy and dissipates power, reducing the overall efficiency. During fast load transients, the inductive elements of the board parasitics and bondwire parasitics generate voltage disturbances proportional to $L\,\mathrm{d}i/\mathrm{d}t$. The associated capacitances can provide local charge storage, but their interaction with the series inductance may also produce overshoot, undershoot, or ringing. Therefore, the complete parasitic network affects the DC behavior, transient response, and overall efficiency of the LDO.

To mitigate these effects, multiple parallel bond wires can be used for each supply connection. This reduces the effective bondwire resistance and inductance, lowering both the static voltage drop and the transient disturbance seen at the die. The remaining board and package parasitics must nevertheless be included in the final validation, since they determine the actual V_{DD} and V_{SS} conditions applied to the regulator.

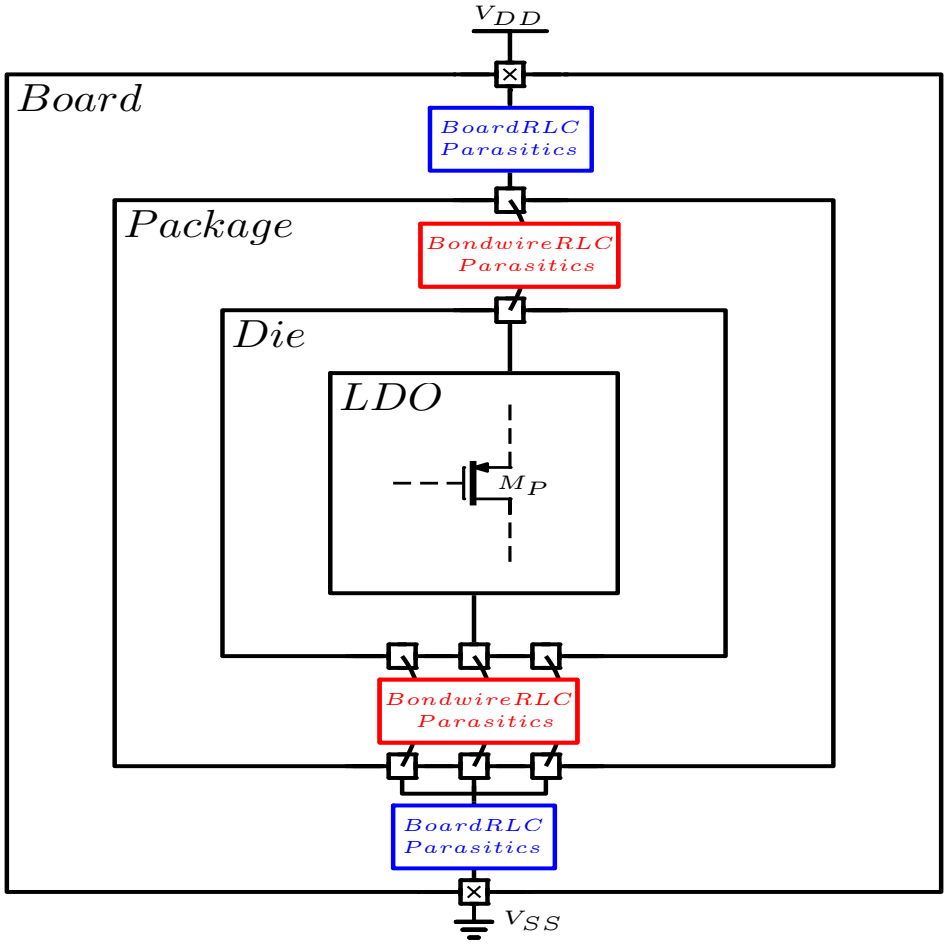


Figure 4.21: Parasitics in the V_{DD} and V_{SS} supply paths of the LDO.

In this work, the board and bondwire parasitics are modeled by the RLC cell in Fig. 4.22, which captures the resistive, inductive, and capacitive effects of the supply interconnect.

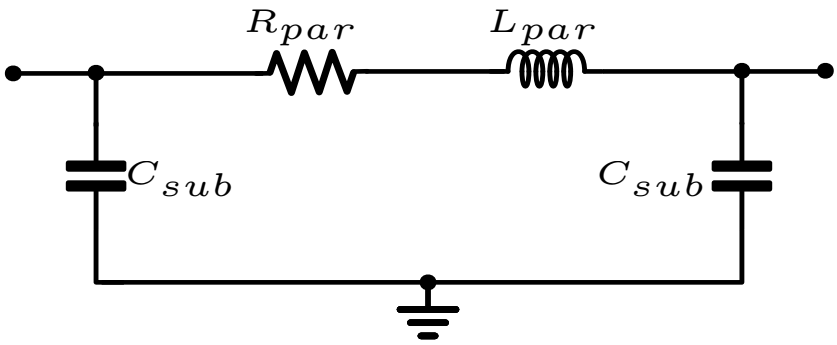


Figure 4.22: Parasitic model.

For the V_{DD} rail, the board and bondwire parasitic elements are combined into the series RLC cell shown above. The total parasitic inductance is estimated as $L_{\mathrm{par}} \approx 4\,\mathrm{nH}$, representing the inductance of the supply-current path from the board to the die. The

associated parasitic resistance is estimated as $R_{\text{par}} \approx 150\,\text{m}\Omega$ and models the resistance of the board, package, and bondwire connections.

For the V_{SS} rail, the resulting parasitic inductance is lower because of the shorter and more direct return path. It is estimated as $L_{\text{par},V_{\text{SS}}} \approx 1.5\,\text{nH}$, while the parasitic resistance is conservatively assumed to be the same as for the V_{DD} path, namely $R_{\text{par},V_{\text{SS}}} \approx 150\,\text{m}\Omega$. The parasitic inductances of the supply and return paths can resonate with the large load capacitance, $C_L = 1\,\text{nF}$. The resonance associated with the path shown in Fig. 4.23 is problematic because its frequency lies below the fast-loop unity-gain frequency.

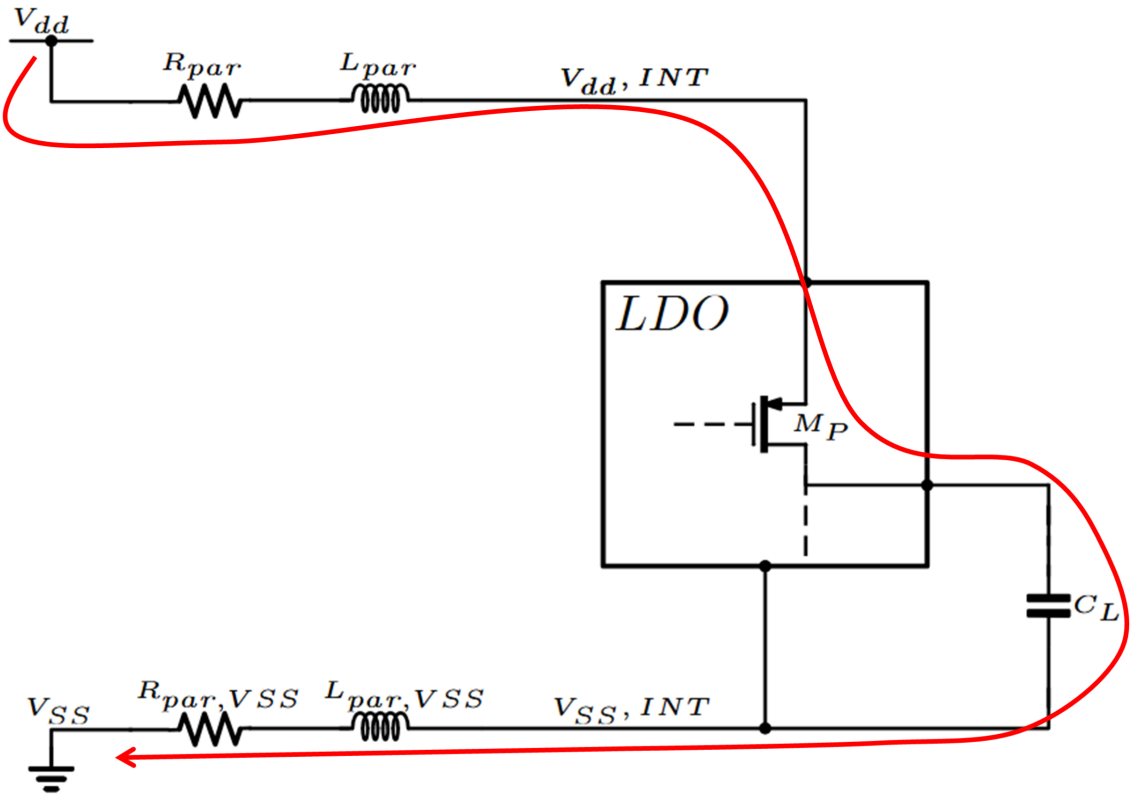


Figure 4.23: Resonance path due to the load capacitance and parasitic inductance.

In this frequency range, the fast loop is active and the resonance can introduce peaking, ringing, and phase degradation, thereby reducing the stability margin. The estimated resonance frequency is $f_{\text{res}} \approx 68\,\text{MHz} < f_{ug,\text{Fast Loop}}$

$$\omega_{\text{res}} \approx \frac{1}{\sqrt{C_L\left(L_{\text{par},V_{\text{DD}}} + L_{\text{par},V_{\text{SS}}}\right)}}$$

The maximum-load fast-loop Bode response with and without parasitic inductance is shown in Fig. 4.24. The parasitic RLC network introduces a resonance that makes the fast loop unstable, as shown in the figure.

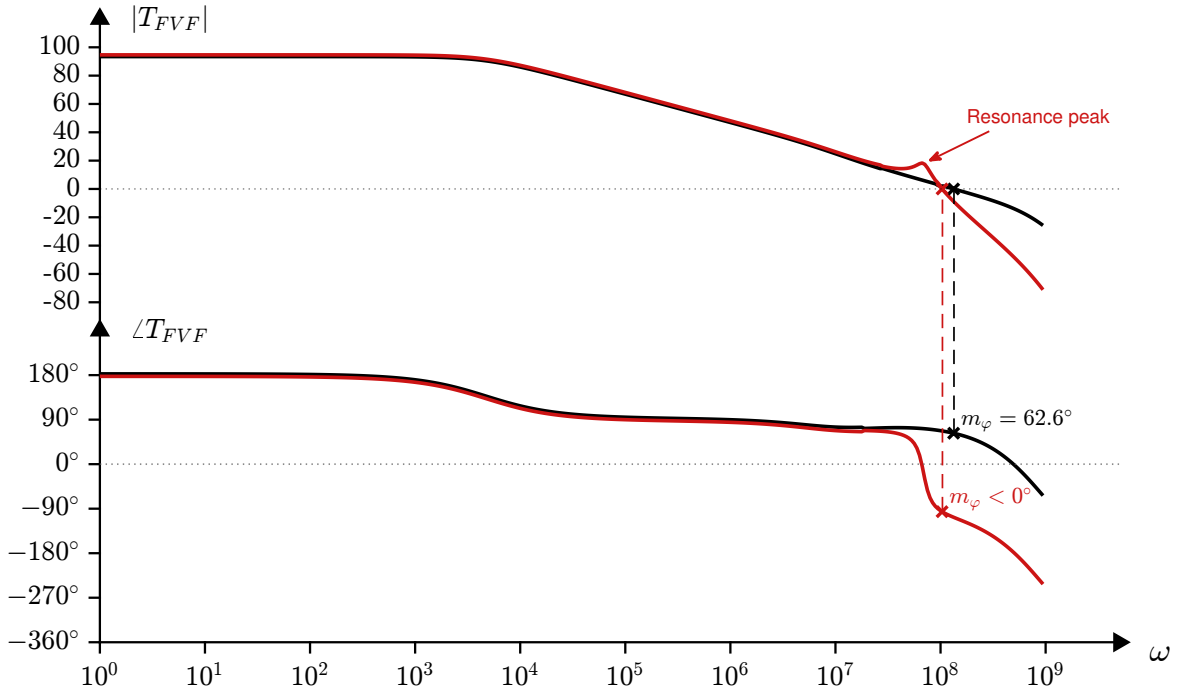


Figure 4.24: Fast-loop Bode response with and without parasitic inductance.

The result in Fig. 4.24 shows that the parasitic resonance must be damped to preserve fast-loop stability. Two complementary solutions were therefore considered. The first solution uses two filter capacitors, C_{F1} and C_{F2}, connected between V_{DD} and V_{SS}. At high frequency, this arrangement allows the two supply rails to oscillate together and reduces the voltage excursion across the parasitic inductances. The two capacitors are deliberately implemented with different damping: C_{F1} is placed in series with R_F, providing a low-Q branch, whereas C_{F2} is used without a series resistor, providing a high-Q branch. As described above, this combination preserves the filtering action of the capacitors while R_F dissipates energy and damps the resonance introduced by the capacitors and the parasitic inductances.

The second solution adds a resistor R_S in series with the load capacitor C_L. This resistor directly increases the damping of the resonance path shown in Fig. 4.23. The corresponding damping factor is

$$\xi = \frac{r_{ds,\mathrm{on},P} + R_S}{2\omega_{\mathrm{res}} L_{\mathrm{par}}}$$

Besides reducing the oscillation amplitude, R_S introduces a zero at

$$\omega_{z_O} = \frac{1}{C_L R_S},$$

which can further improve the stability of the fast loop. These benefits, however, do

not come for free. As shown later by the simulations in Chapter 5, the added series resistors reduce the fast-loop bandwidth. The design therefore involves a trade-off with the transient response: the series resistors can limit how quickly the capacitor can supply charge during abrupt load-current changes, and the transient performance of the LDO is consequently degraded. Thanks to these two solutions, shown in Fig. 4.25, the proposed LDO maintains a stable fast-loop response even in the presence of the parasitic network.

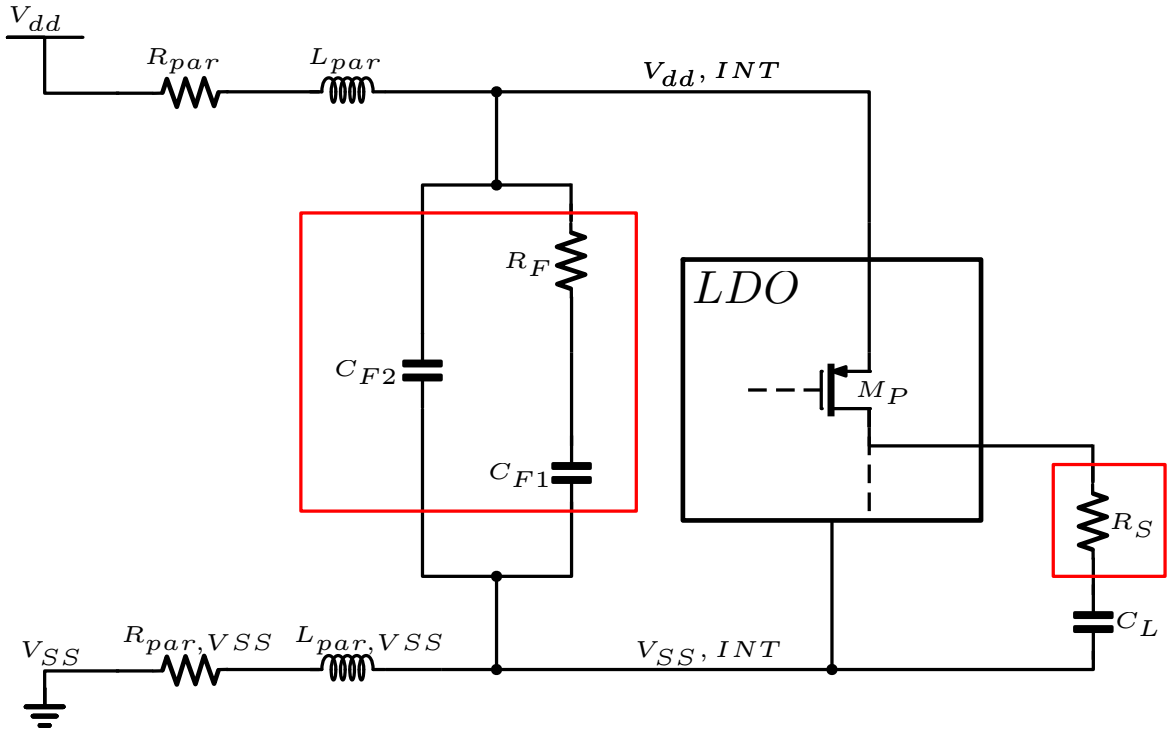


Figure 4.25: Implemented solutions for reducing the effect of the parasitic resonance.

Chapter 5

Simulation Results

The purpose of this chapter is to assess the performance of the proposed PMOS capless FVF LDO and, consequently, to validate the selected architecture. This is done by presenting the results of several simulations carried out under different operating conditions. Section 5.1 first introduces the testbench used for the analyses. The following sections then discuss the results needed to evaluate the robustness and effectiveness of the design.

The DC analysis verifies the main static characteristics of the regulator, including output accuracy, load regulation, and line regulation. The frequency-domain analysis is used to assess stability, the adopted compensation strategy, and the overall behavior of the loop, which is expected to be consistent with the qualitative trends described in Chapter 4. Finally, Section 5.4 investigates the time-domain response of the LDO under different load-current conditions, with particular attention to its dynamic behavior.

For selected analyses, the results are reported both with and without the relevant parasitic elements. The simulations without parasitics make it easier to identify the nominal behavior of the architecture, whereas the complete simulations show how the LDO actually behaves in the presence of the parasitic network. In many papers, especially those dealing with high-bandwidth LDOs, the parasitic elements are not included in the reported results. However, the resonances introduced by these elements can significantly reduce the stability margin and, in severe cases, make the circuit unstable. For this reason, the effect of the parasitics is explicitly assessed here rather than being neglected in the final validation.

PVT analyses are reported throughout the chapter as well. These checks are essential to verify that the LDO remains functional under non-ideal conditions that may arise from manufacturing variations and from changes during operation. The process analysis considers the four combinations of fast and slow NMOS and PMOS devices, namely FF, FS, SF, and SS. The supply-voltage analysis applies a $\pm 10\%$ variation to V_{DD},

while the temperature is swept over $T \in [-40, +150]$ °C.

The results presented here are the outcome of a continuous refinement process that took place throughout the design phase. Each sizing step was followed by additional simulations, parameter sweeps, and checks, allowing the circuit to be progressively optimized toward the required performance.

5.1 Testbench

The testbench used to simulate and characterize the LDO is shown in Fig. 5.1.

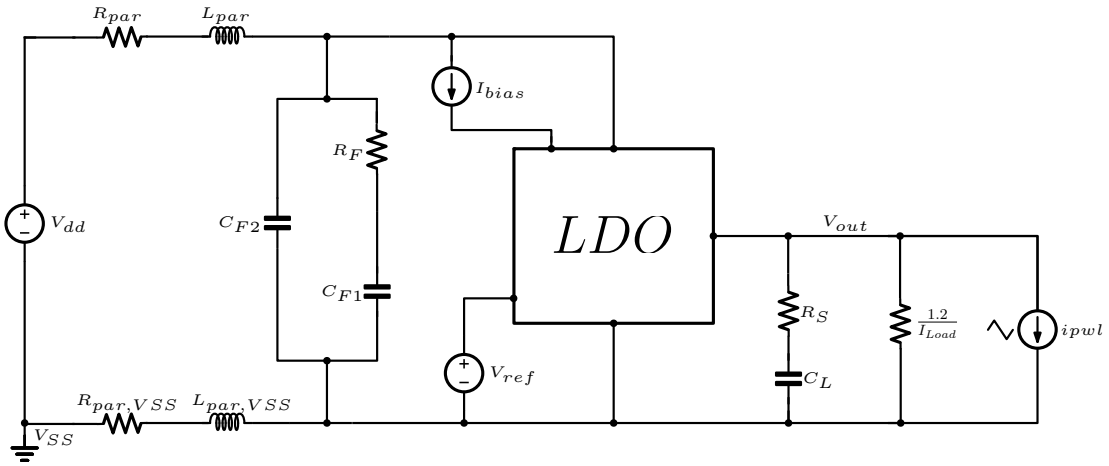


Figure 5.1: Testbench schematic.

In addition to the parasitic network and its associated compensation, discussed in Section 4.7, the testbench includes two ideal voltage sources. These sources provide the voltage reference V_{ref} and the supply voltage V_{DD}, respectively. An additional ideal current source generates I_{bias}, which is used to establish the biasing network of the LDO. The testbench also includes an IPWL source, used to generate the load-current steps required for the time-domain analysis.

For the frequency-domain analysis, the load current is represented by a resistive load. The load resistance is defined as

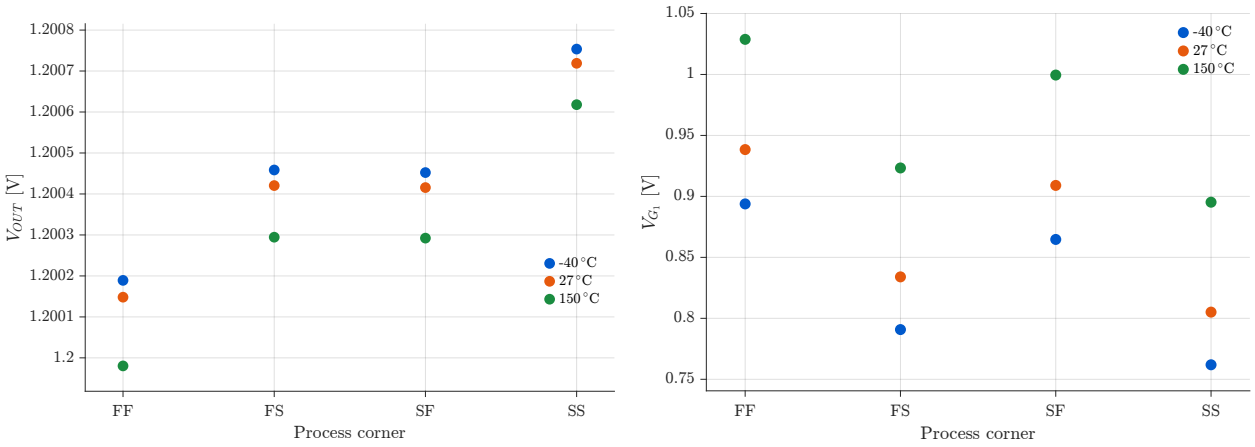
$$R_L = \frac{V_{\text{out}}}{I_{\text{load}}},$$

so that the desired load current is obtained at the nominal output voltage. The loop-break points used for the STB analyses are shown for the slow loop in Section 4.5 and for the fast loop in Section 4.3.

5.2 LDO DC Performance

The DC analysis evaluates the steady-state output accuracy and regulation of the LDO under variations in process, supply voltage, temperature, and load current.

As shown in Fig. 5.2a, the output voltage is less accurate in the slow process corners and at low temperatures. As shown in Fig. 5.2b, the gate voltage of M_1 decreases at lower temperatures and is lowest in the SS corner. To produce this lower control voltage, the finite-gain OTA requires a larger positive difference between the feedback and reference voltages. Consequently, the output settles slightly above its nominal value. The simulations are performed at $I_{LOAD} = 50$ mA and $V_{DD} = 1.8$ V.



(a) Output voltage.

(b) Gate voltage of M_1.

Figure 5.2: DC output voltage and gate voltage of M_1 across process corners and temperature variations.

Figure 5.3 shows the gate voltage of the PMOS pass device, including parasitic effects, as a function of load current for the PVT corners. Each panel corresponds to one temperature, and the four process corners are distinguished by color. Consistent with Fig. 5.2b, the gate voltage is lower in the SS corner and at lower temperatures.

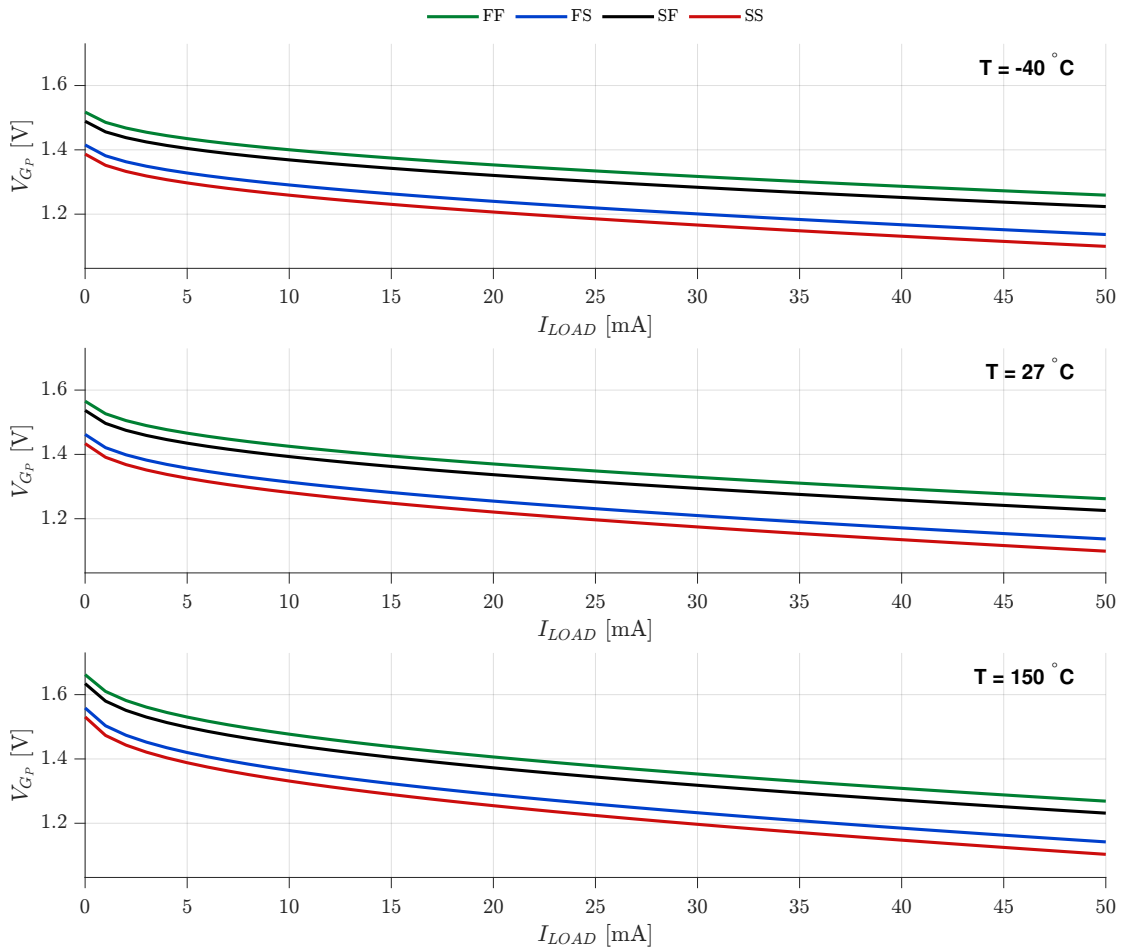


Figure 5.3: PVT variation of the pass-device gate voltage, V_{G_P}, including parasitic effects, versus load current.

Figure 5.4 reports the load-regulation response under nominal conditions. The DC output accuracy is defined as

$$\text{DC accuracy} = \left| \frac{V_{OUT,real} - V_{OUT,ref}}{V_{OUT,ref}} \right| \times 100\%.$$

The LDO maintains an accuracy much better than 1% up to a load current of approximately 340 mA. The PVT load-regulation results are shown in Fig. 5.5. Both plots show the load-regulation response over a load-current range from 0 to 2 A, extending beyond the 50 mA design load to show the loss of regulation at large currents. In the PVT plot, color identifies the process corner and line style identifies the supply voltage.

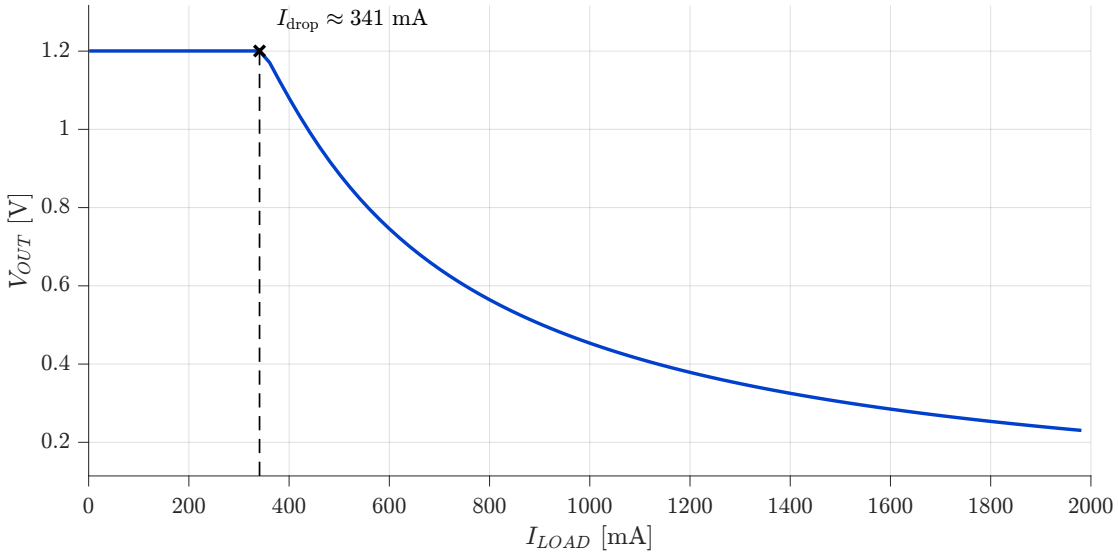


Figure 5.4: Nominal-condition DC load regulation versus I_{LOAD}.

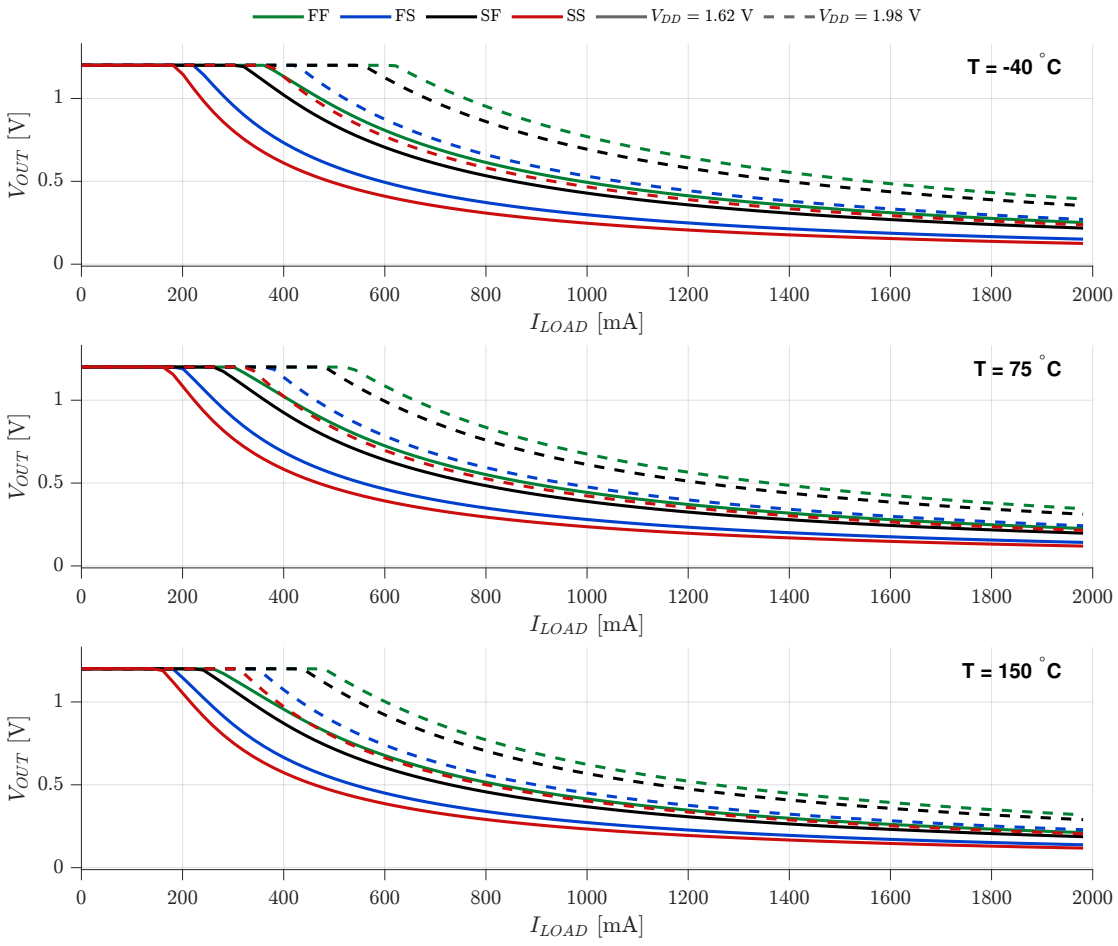


Figure 5.5: PVT variations of DC load regulation versus I_{LOAD}.

Figure 5.6 shows the PVT variation of the LDO DC line regulation. With a 1% output-error criterion, the worst-case minimum input voltage for regulation is

approximately 1.32 V. Considering the worst-case PVT condition, the LDO operates in the dropout region below this voltage; above it, within the tested range, the LDO enters the normal operating region and regulates the output to the desired 1.2 V within the stated accuracy. The use of a PMOS pass device supports low-dropout operation, allowing V_{IN} to approach V_{OUT} while maintaining output regulation.

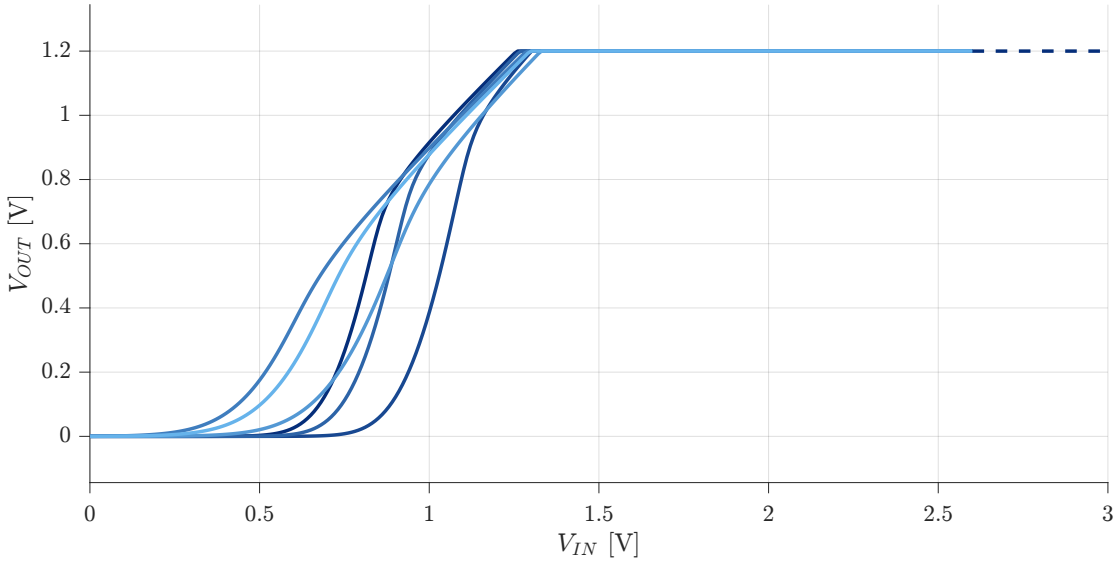


Figure 5.6: PVT variations of DC line regulation at 50 mA.

5.3 LDO Frequency Behavior and Stability

To evaluate the frequency-domain behavior of the LDO, loop-gain simulations were performed to assess the stability and bandwidth of both the fast loop, $T_{\mathrm{FVF}}(s)$, and the slow accuracy loop, $T_{\mathrm{TOT}}(s)$. For these simulations, the loops were opened and tested using the configurations shown in Figs. 4.4 and 4.15, respectively.

As shown in Fig. 5.7, the fast loop was designed to achieve a wide bandwidth so that it can respond rapidly to variations in V_{OUT} or I_L. Under nominal conditions without parasitic effects, the unity-gain bandwidth reaches 133 MHz at the maximum load of 50 mA. At the minimum load of 1 μA, it is 40.3 MHz, still providing a wide bandwidth. The phase margin remains above 60° at both loads, reaching 62.6° and 71.7° at maximum and minimum load, respectively. This is supported by the zero-pole tracking compensation, with a compensation zero that closely follows the load-dependent output pole.

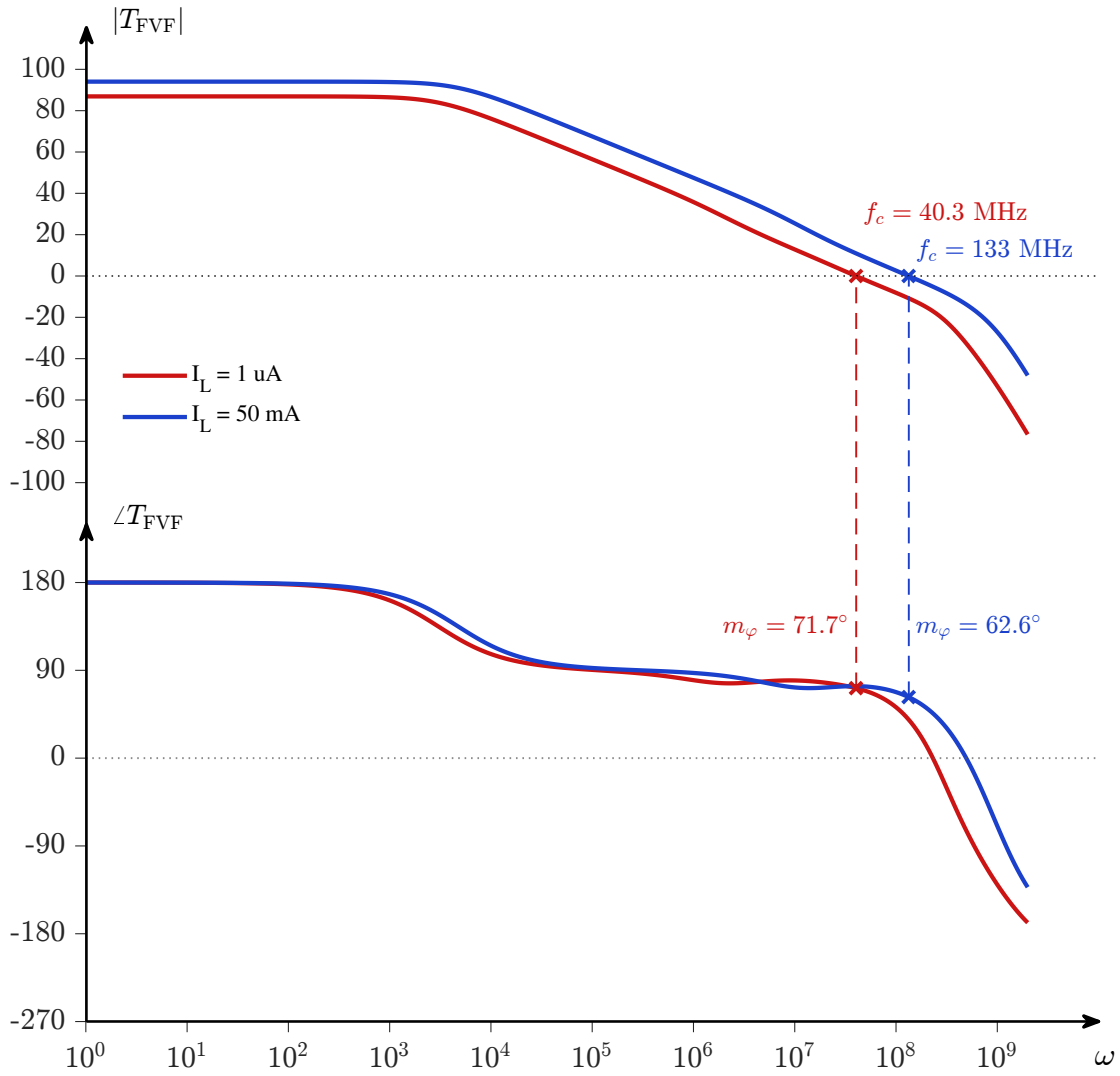


Figure 5.7: Nominal fast-loop Bode responses without parasitic effects at minimum ($I_L = 1$ μA) and maximum ($I_L = 50$ mA) load.

The fast-loop results extracted from the PVT sweeps without parasitic effects are reported in Figs. 5.8–5.11. Figures 5.8 and 5.9 show the gain and phase responses, respectively. Figures 5.10 and 5.11 show the phase margin and output voltage, respectively, as functions of temperature for the investigated load currents and supply voltages.

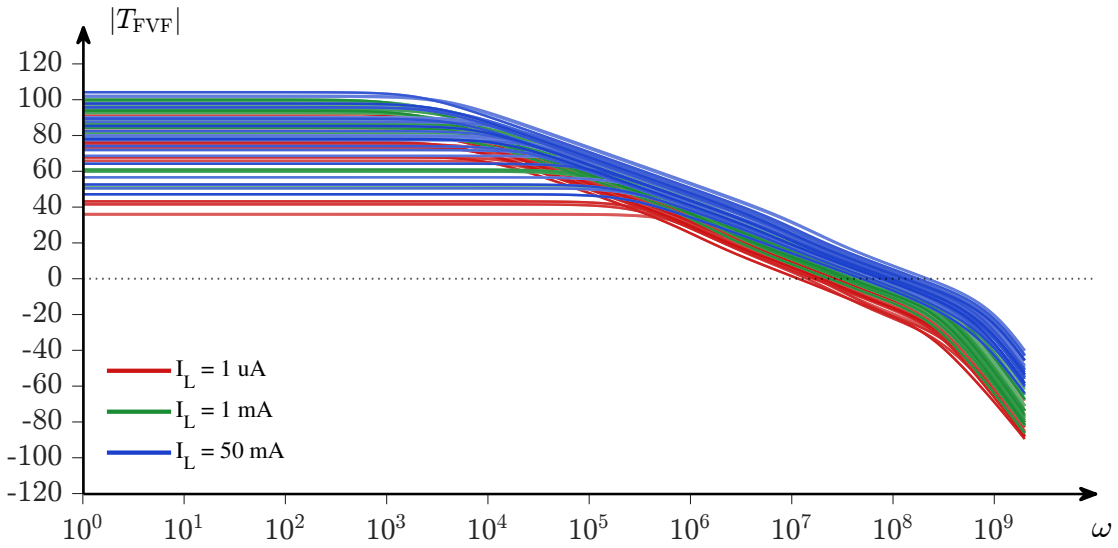


Figure 5.8: Fast-loop PVT gain responses grouped by load current.

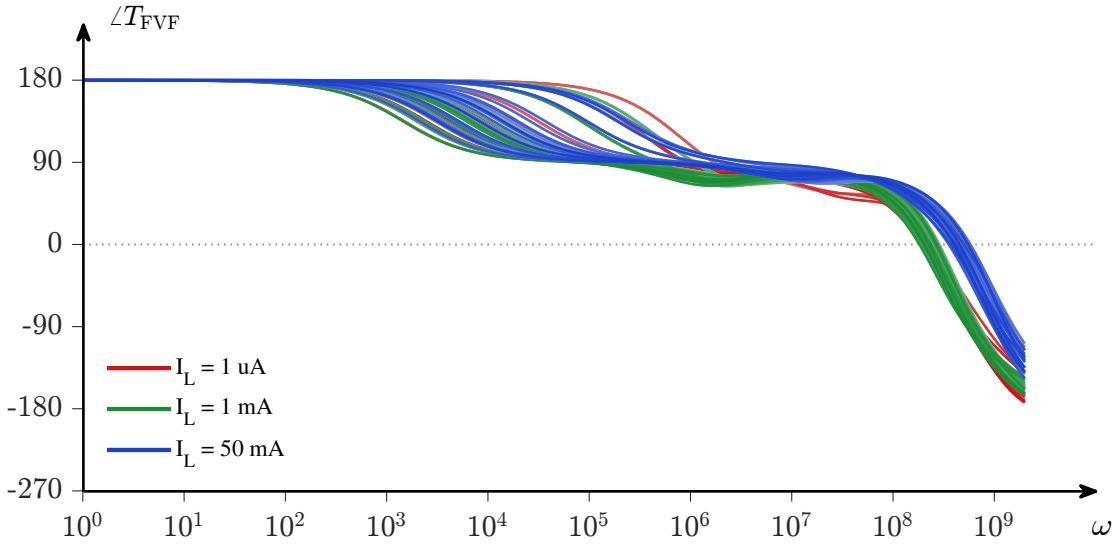


Figure 5.9: Fast-loop PVT phase responses grouped by load current.

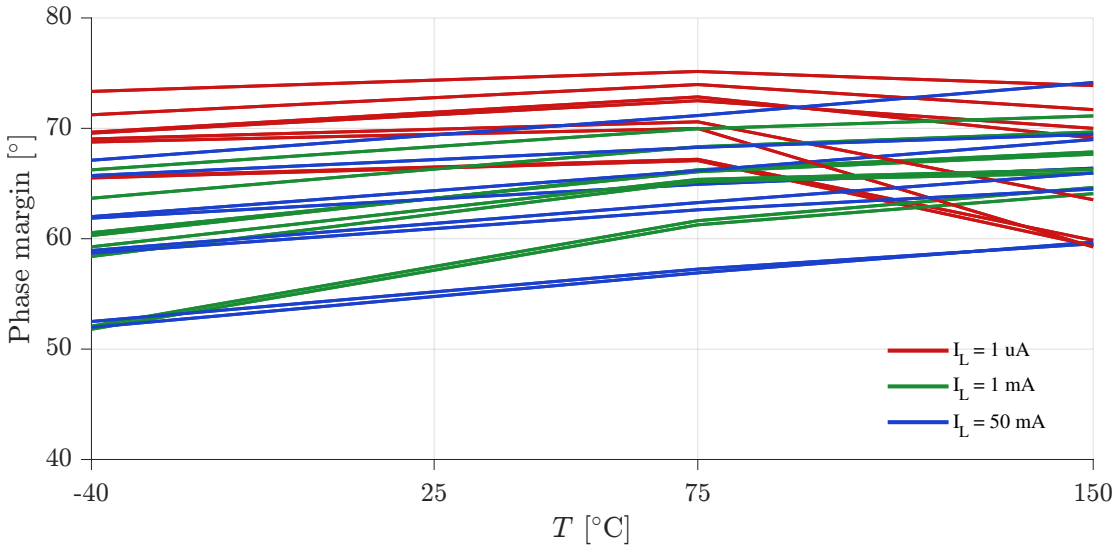


Figure 5.10: Fast-loop PVT phase margin grouped by load current.

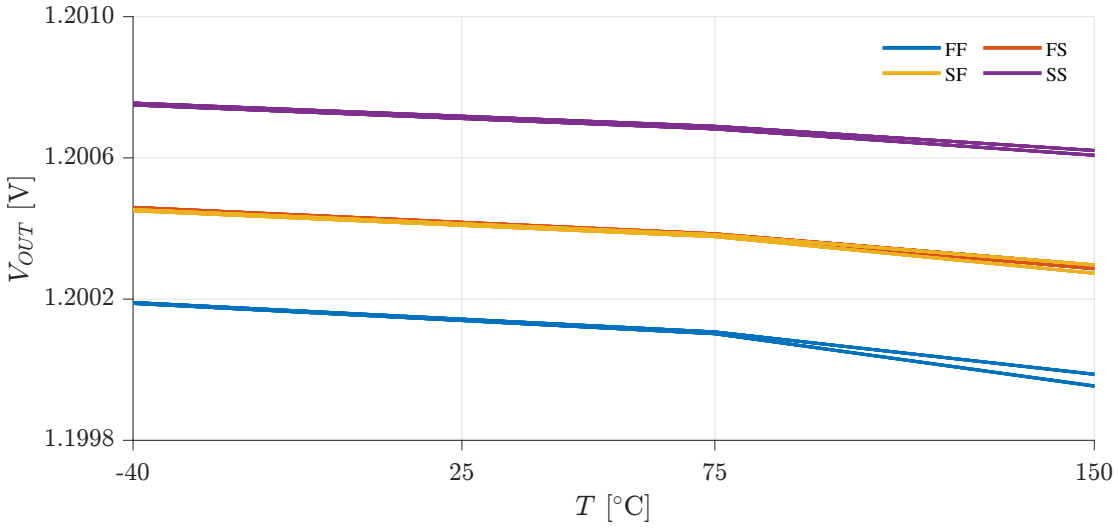


Figure 5.11: Fast-loop PVT output voltage grouped by process corner.

The nominal fast-loop response including the parasitic effects is shown in Fig. 5.12. At maximum load, the unity-gain bandwidth is reduced from 133 MHz without parasitic effects to 81.9 MHz. As discussed in Section 4.7, this reduction is due to the introduction of the parasitic network and the damping solutions adopted to preserve stability. At minimum load ($I_L = 1$ μA), the phase margin increases to 86.7°, benefiting from the additional zero introduced by R_S in series with C_L. At maximum load ($I_L = 50$ mA), the phase margin is 62.8°.

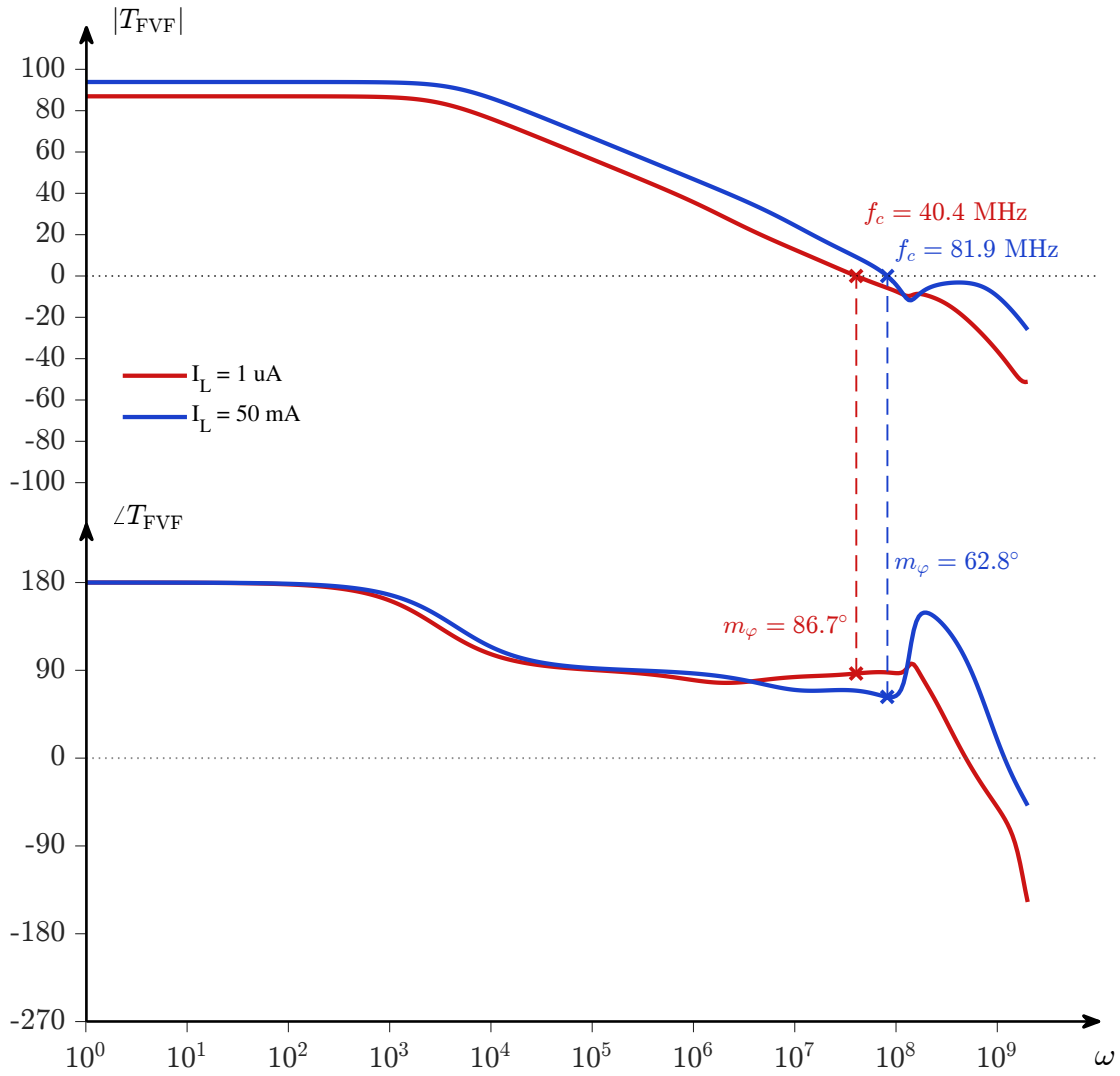


Figure 5.12: Nominal fast-loop Bode responses including parasitic effects at minimum ($I_L = 1$ μA) and maximum ($I_L = 50$ mA) load.

With parasitic effects included, the PVT gain and phase responses of the fast loop are presented in Figs. 5.13 and 5.14, respectively. The corresponding phase margin and output voltage are shown in Figs. 5.15 and 5.16, respectively.

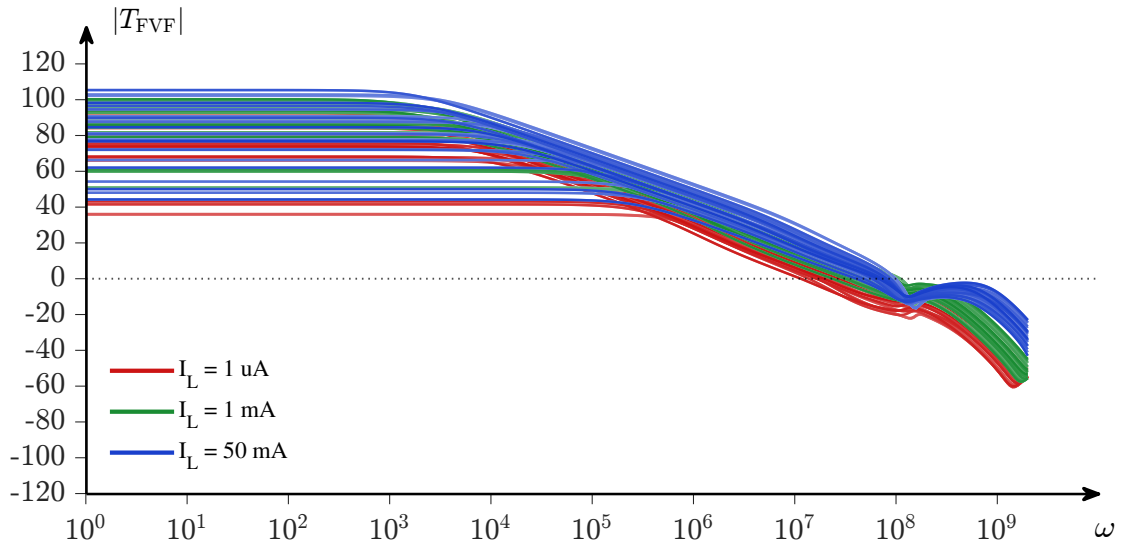


Figure 5.13: Fast-loop PVT gain responses including parasitic effects, grouped by load current.

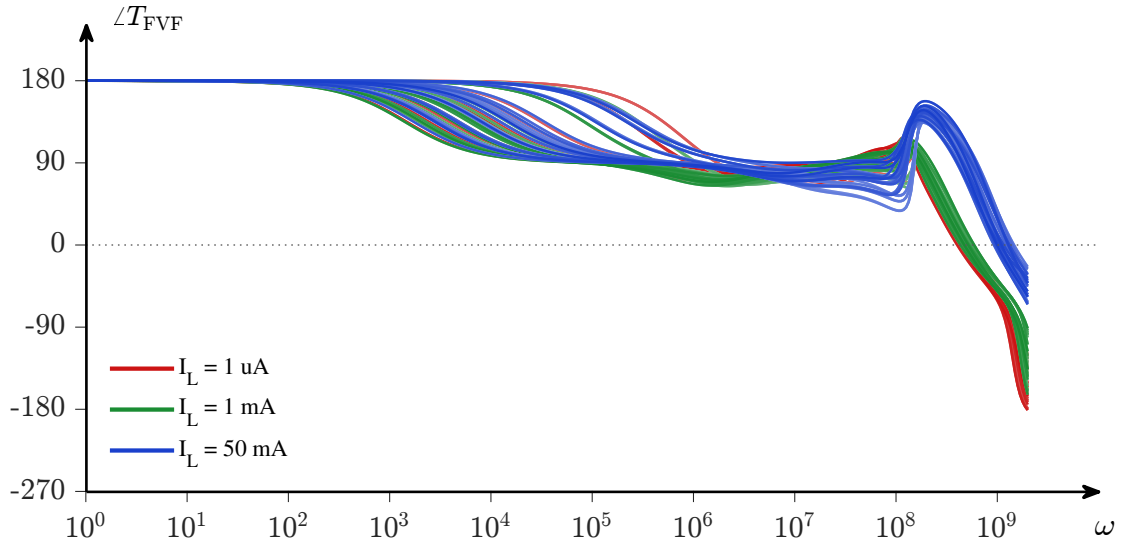


Figure 5.14: Fast-loop PVT phase responses including parasitic effects, grouped by load current.

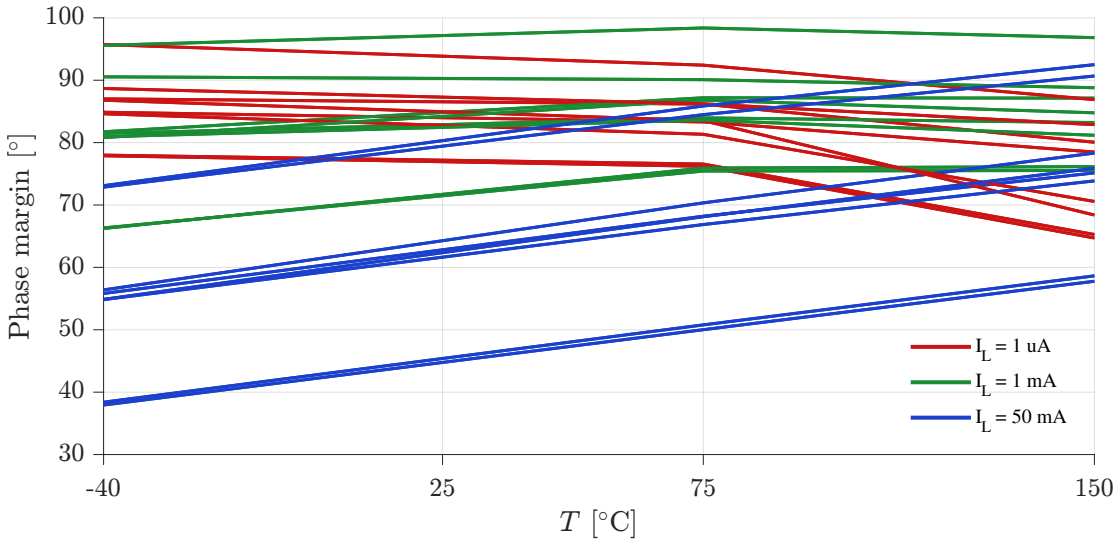


Figure 5.15: Fast-loop PVT phase margin including parasitic effects, grouped by load current.

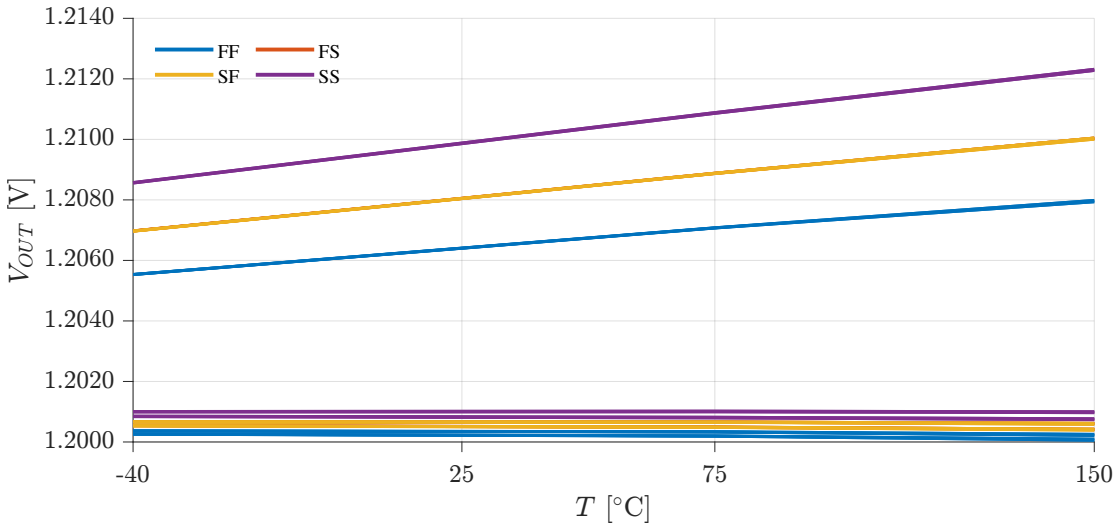


Figure 5.16: Fast-loop PVT output voltage including parasitic effects, grouped by process corner.

The nominal slow-loop response is shown in Fig. 5.17. The slow loop crosses 0 dB at about 1.1 MHz at both loads, with phase margins of 89.0° and 88.7° at 1 μA and 50 mA.

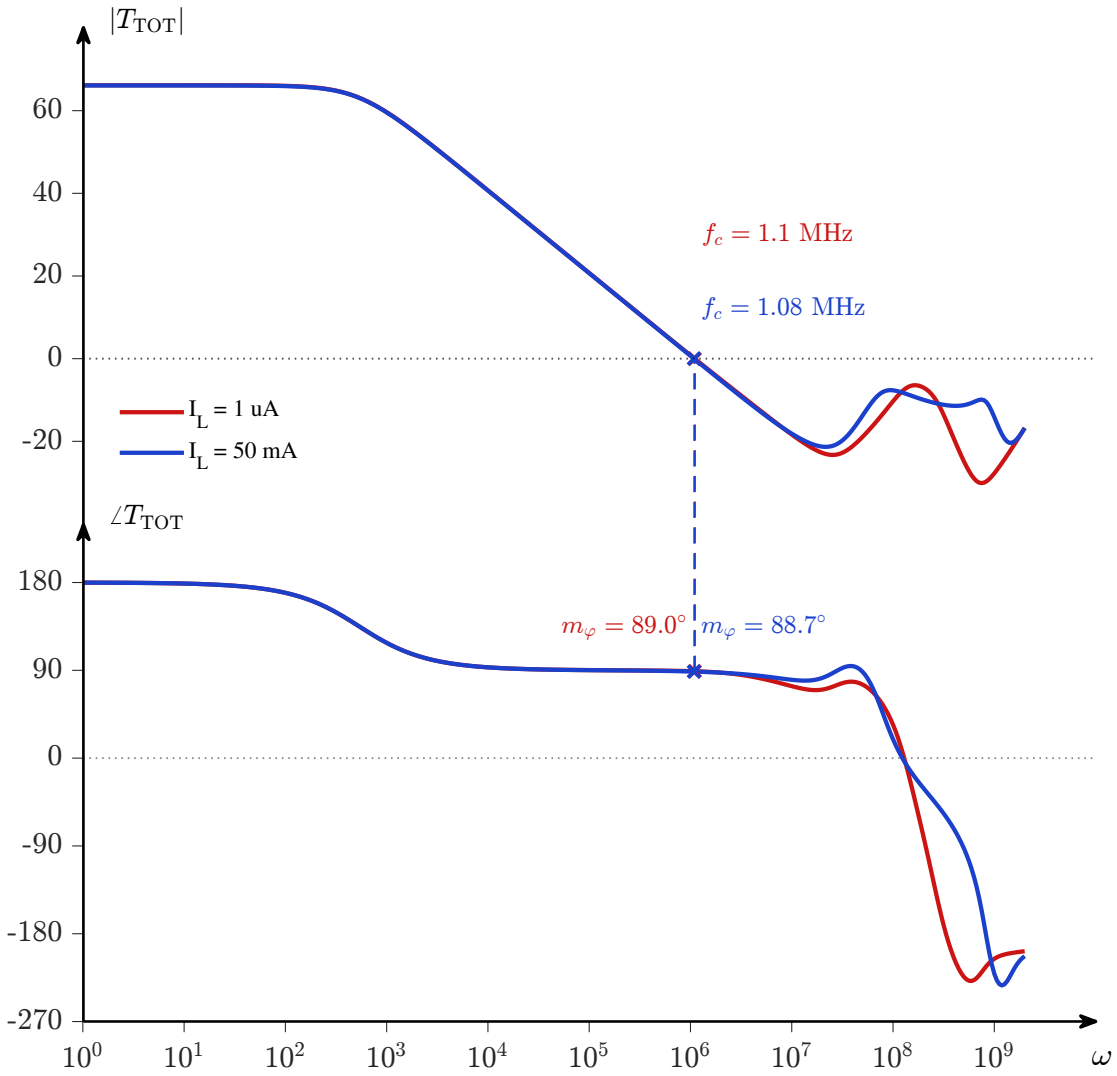


Figure 5.17: Nominal slow-loop Bode responses at minimum ($I_L = 1\ \mu$A) and maximum ($I_L = 50$ mA) load.

The PVT gain and phase responses of the slow loop, including the parasitic effects, are reported in Figs. 5.18 and 5.19. Across the simulated PVT corners and load currents, the DC gain ranges from 59.0 to 66.5 dB, the unity-gain frequency from 0.64 to 1.73 MHz, and the phase margin from 88.2° to 89.4°.

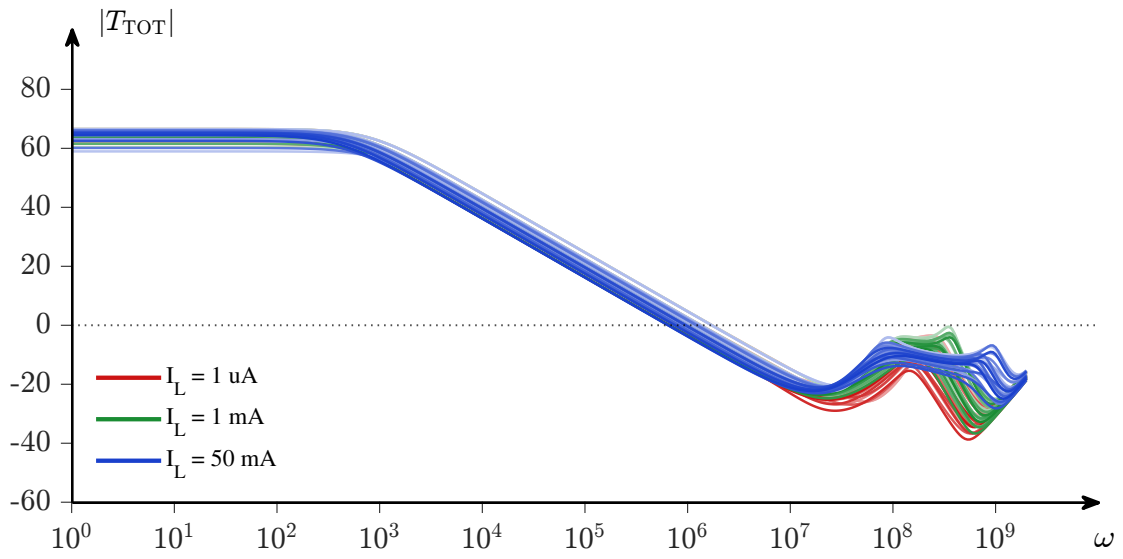


Figure 5.18: Slow-loop PVT gain responses including parasitic effects, grouped by load current.

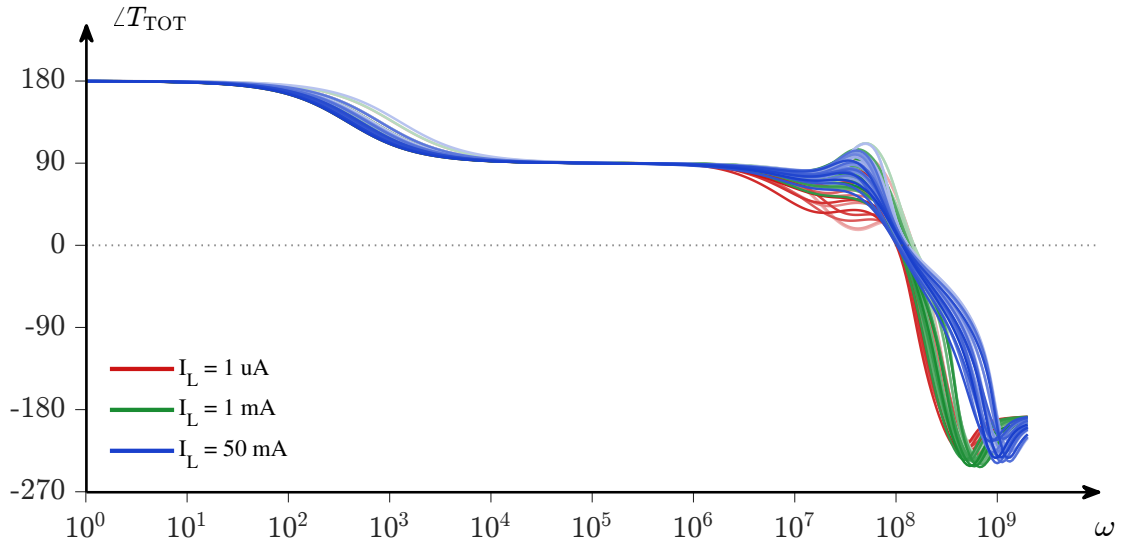


Figure 5.19: Slow-loop PVT phase responses including parasitic effects, grouped by load current.

To better understand the operation of the zero-tracking compensation and the fast-loop dynamics, Fig. 5.20 shows the extracted pole and zero frequencies as functions of the load current I_L. The dominant pole f_{pB} remains approximately between 3 and 5 kHz over the load range, while the higher-frequency pole f_{pA} is located at about 500 MHz. A further fitted pole, f_{pG}, lies above 1 GHz, more than one decade above the unity-gain bandwidth (UGB); its contribution is therefore neglected in the discussion of the loop dynamics. Figure 5.21 examines f_{pO} and f_z in more detail: the tracking zero follows the output pole, compensating for its phase lag.

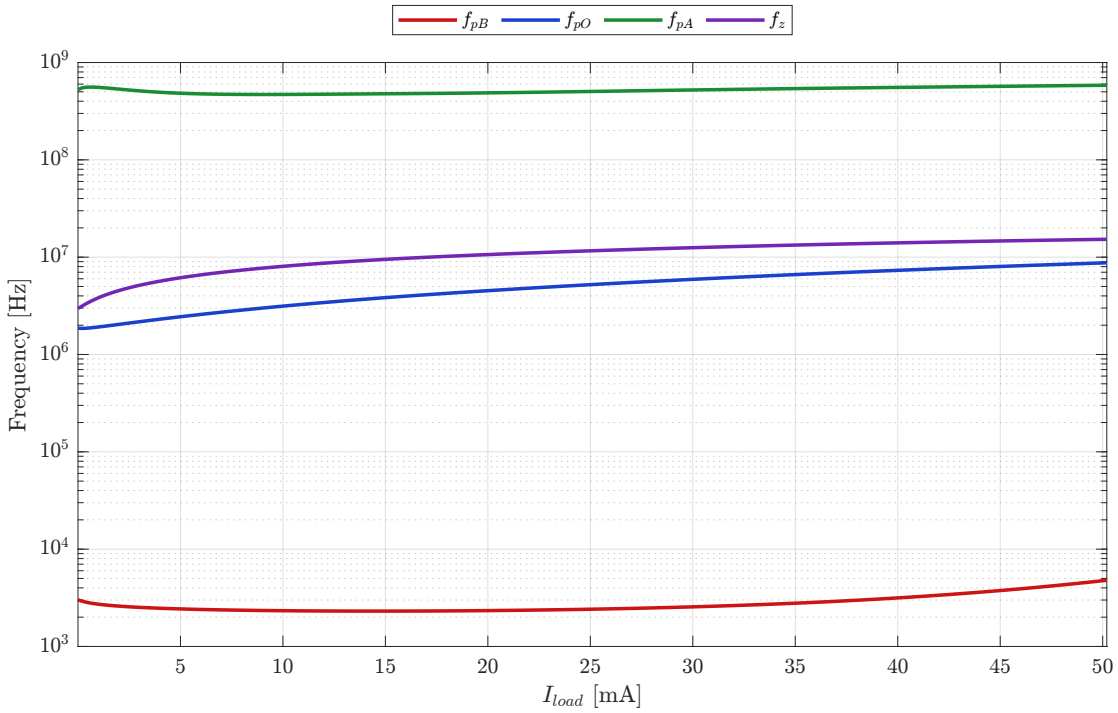


Figure 5.20: Qualitative illustration of the poles and tracking zero of the loop gain versus load current.

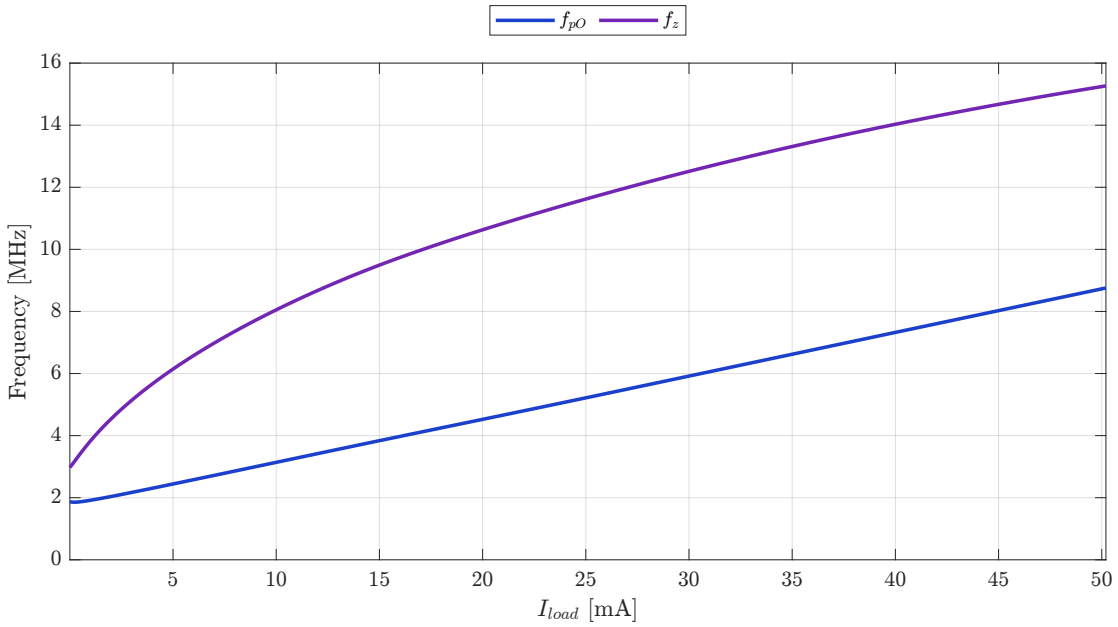


Figure 5.21: Mobile pole and tracking zero versus load current.

Figure 5.22 shows the equivalent total tracking resistance $R_{Z,\text{tot}}$ as a function of load current. As described in Section 4.4, it is set by placing the fixed resistor $R_{Z,\text{fix}}$ in parallel with the load-dependent resistance of the MOS transistor M_Z. The total resistance decreases monotonically from 5.24 kΩ at minimum load to 1.02 kΩ at maximum load,

with most of the reduction occurring below 10 mA. Its trend is consistent with the qualitative target, allowing the zero to track the output pole quite closely.

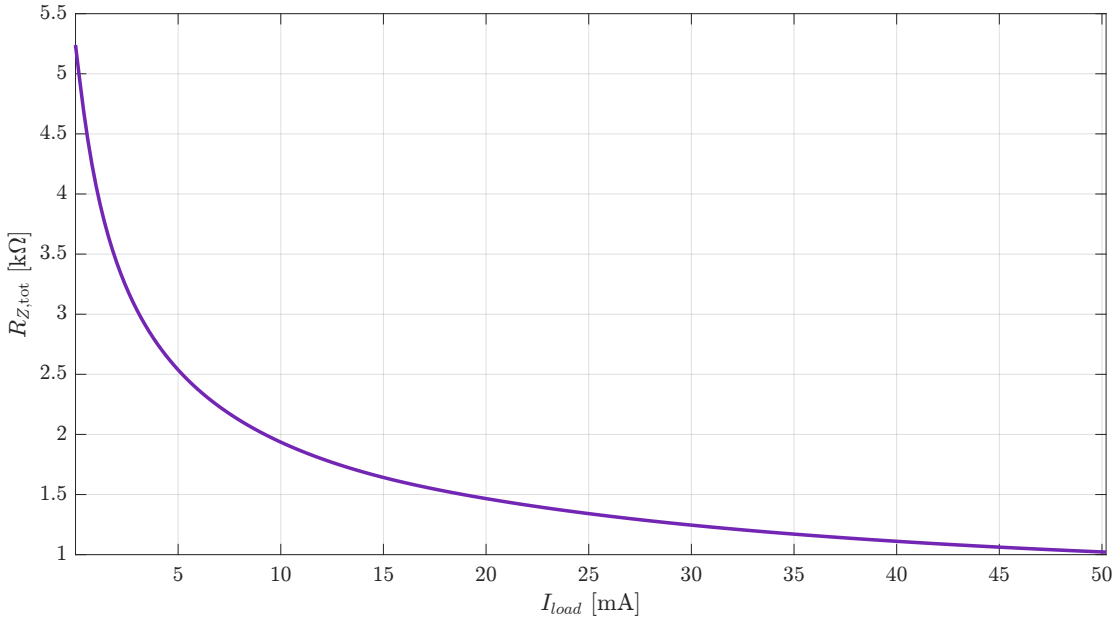


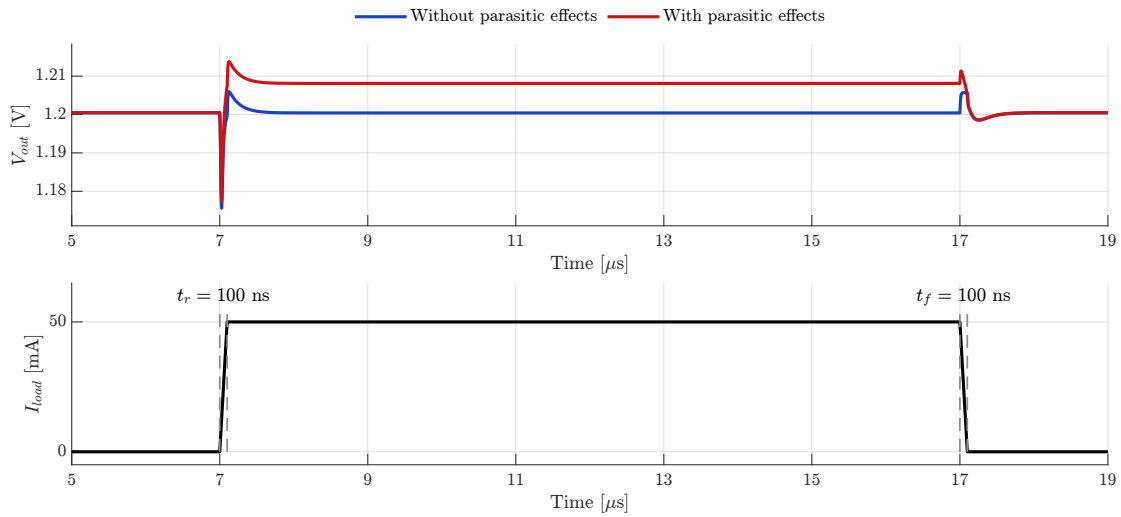
Figure 5.22: Equivalent total tracking resistance $R_{Z,\text{tot}}$ versus load current.

Due to time constraints, the variation with load current of the poles and zeros associated with the parasitic network is not presented in this thesis. A more detailed study of these effects is left to future work during my PhD.

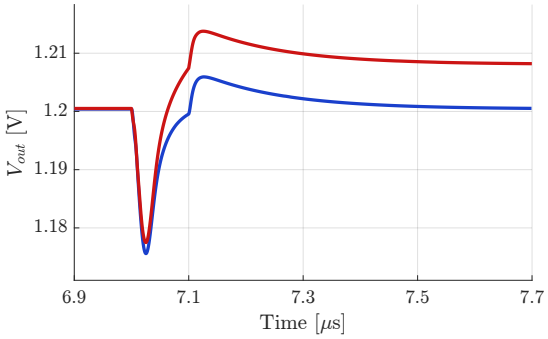
5.4 Time-Domain Performance

This section evaluates the regulator's response to rapid load-current steps and its ability to maintain output regulation. The main metrics are undershoot, the maximum drop in output voltage following an increase in load; overshoot, the maximum rise following a decrease in load; and settling time, the time required for the output voltage to return to and remain within 1% of its steady-state value. The voltage deviations are expressed as a percentage of the nominal output voltage.

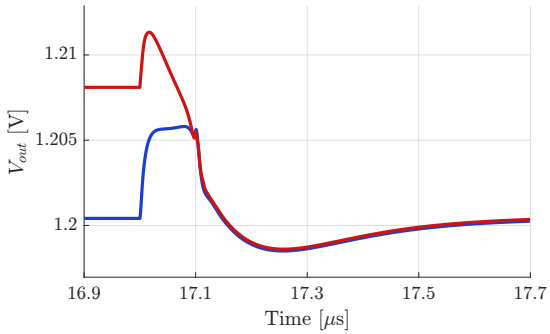
For the target application, the worst-case transient condition is a load step from 0 to 50 mA and back to 0, with rise and fall times of 100 ns. The responses with and without parasitic effects are compared in Fig. 5.23. Relative to the nominal output voltage of 1.2 V, the undershoot and overshoot are 2.03% and 0.48%, respectively, without parasitic effects, and 1.88% and 0.94% with parasitic effects. Both deviations remain well below the target application's 8% limit under nominal conditions.



(a) FVF-LDO load-current step response.



(b) Undershoot following the load increase.



(c) Overshoot following the load decrease.

Figure 5.23: Output-voltage step response with and without parasitic effects.

Figure 5.24 shows all PVT load-transient responses, grouped by temperature. Colors identify the process corners, while solid and dashed lines denote $V_{DD} = 1.71$ V and $V_{DD} = 1.89$ V, respectively. These simulations illustrate, in particular, the sensitivity of the transient response to temperature variations.

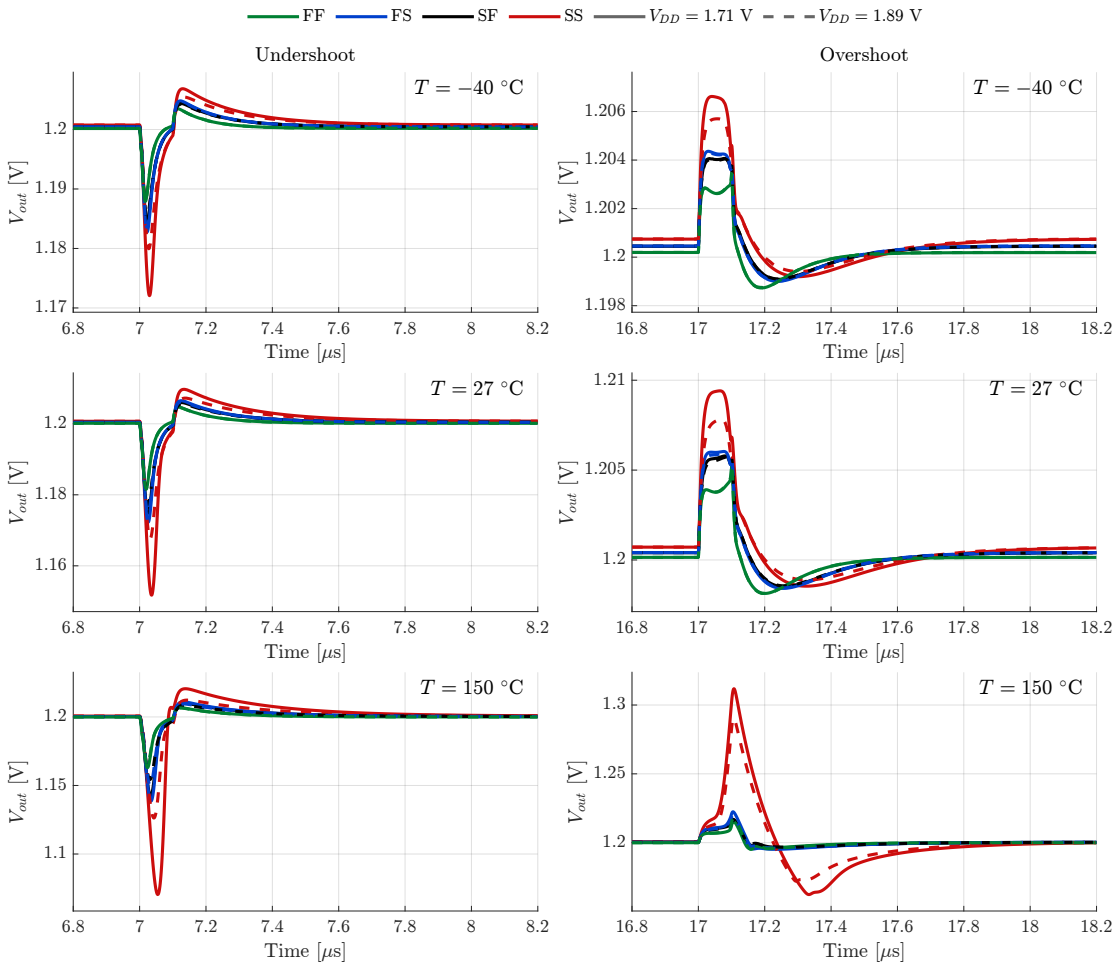
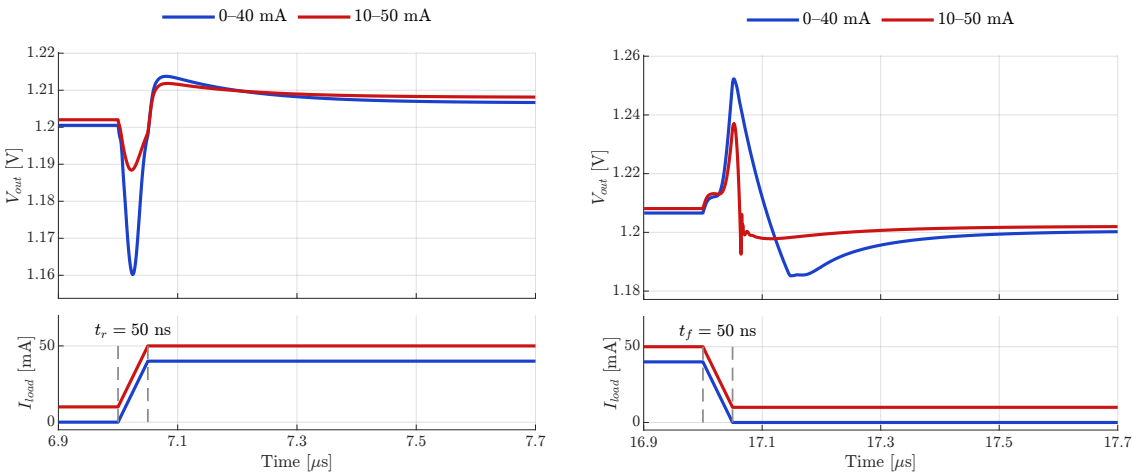


Figure 5.24: PVT load-transient responses grouped by temperature.

To further explore the regulator's transient limits, additional simulations were performed with faster load-current transitions. Figure 5.25 shows the responses for rise and fall times of 50 ns, comparing load steps between 0 and 40 mA and between 10 and 50 mA. The corresponding load-current steps are shown below each output-voltage response.

Although both steps have the same amplitude of 40 mA, the 10–50 mA case exhibits smaller undershoot and overshoot. This comparison illustrates a general consideration in LDO transient testing: transitions to and from zero load can be more demanding than steps of equal amplitude at higher load currents. The step amplitude alone therefore does not determine the transient performance.

This distinction is important when comparing the results with the state of the art. To obtain better transient results, load steps that do not start from zero load current are often analyzed. A fair comparison should therefore consider both load-current endpoints, as well as the step amplitude and rise and fall times.



(a) Undershoot following the load increase. (b) Overshoot following the load decrease.

Figure 5.25: Output-voltage responses and corresponding load-current steps for the 0–40 mA and 10–50 mA cases, with 50 ns rise and fall times.

Even in the more demanding 0–40 mA case, the LDO exhibits an undershoot of 3.32% and an overshoot of 4.36%, relative to the nominal output voltage of 1.2 V. Both deviations remain below 8%, showing that the regulator maintains good transient regulation even for this load step with 50 ns rise and fall times.

To push the transient limits further, an additional simulation was performed for the 10–50 mA load step, with rise and fall times reduced to 1 ns. Figure 5.26 shows the resulting output-voltage response to these faster load-current transitions.

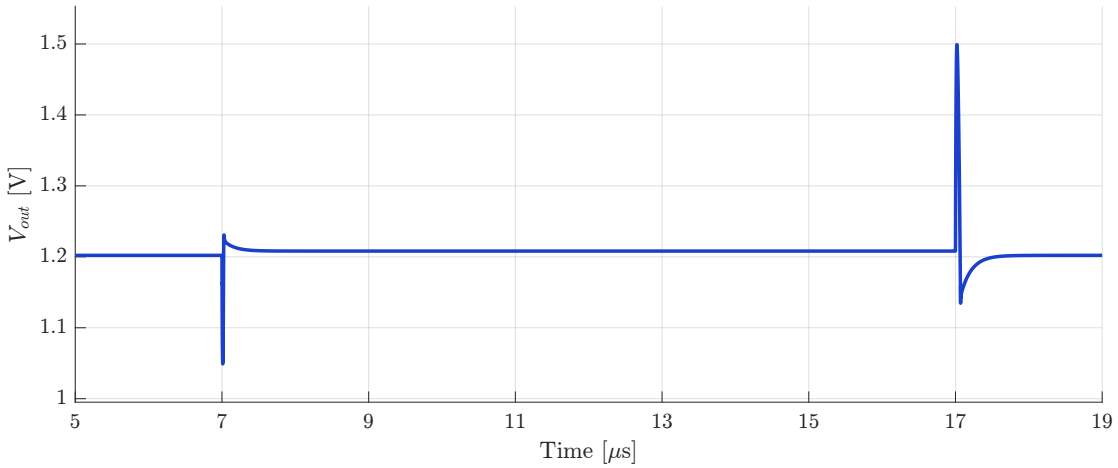


Figure 5.26: Output-voltage transient response for the 10–50 mA load step with 1 ns rise and fall times.

The faster transitions produce larger voltage deviations, particularly overshoot: the undershoot and overshoot reach 12.58% and 24.93%, respectively, relative to the nominal output voltage of 1.2 V. The larger overshoot is consistent with the finite

response time of the PMOS gate drive. Following a load decrease, the gate voltage must rise to reduce the pass-device current. Until this current falls to the new load level, the excess current charges the output capacitance. Moreover, the high-side pass device cannot actively sink this excess charge from the output. The severity of the overshoot therefore depends on the gate-drive dynamics and circuit capacitances, rather than on the PMOS device type alone.

Although not shown in the schematics presented in Chapter 4, the implemented circuit includes a replica of M_1, denoted M_{C2}, together with R_3, as shown in Fig. 5.27. This additional branch provides a current-sinking path to improve the response to load decreases and limit overshoot.

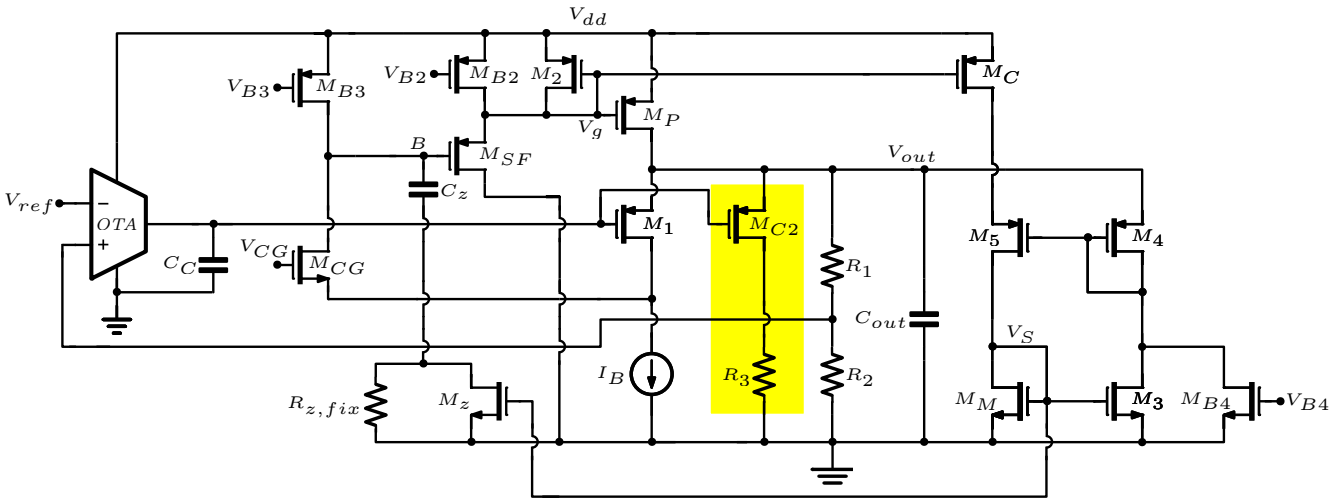
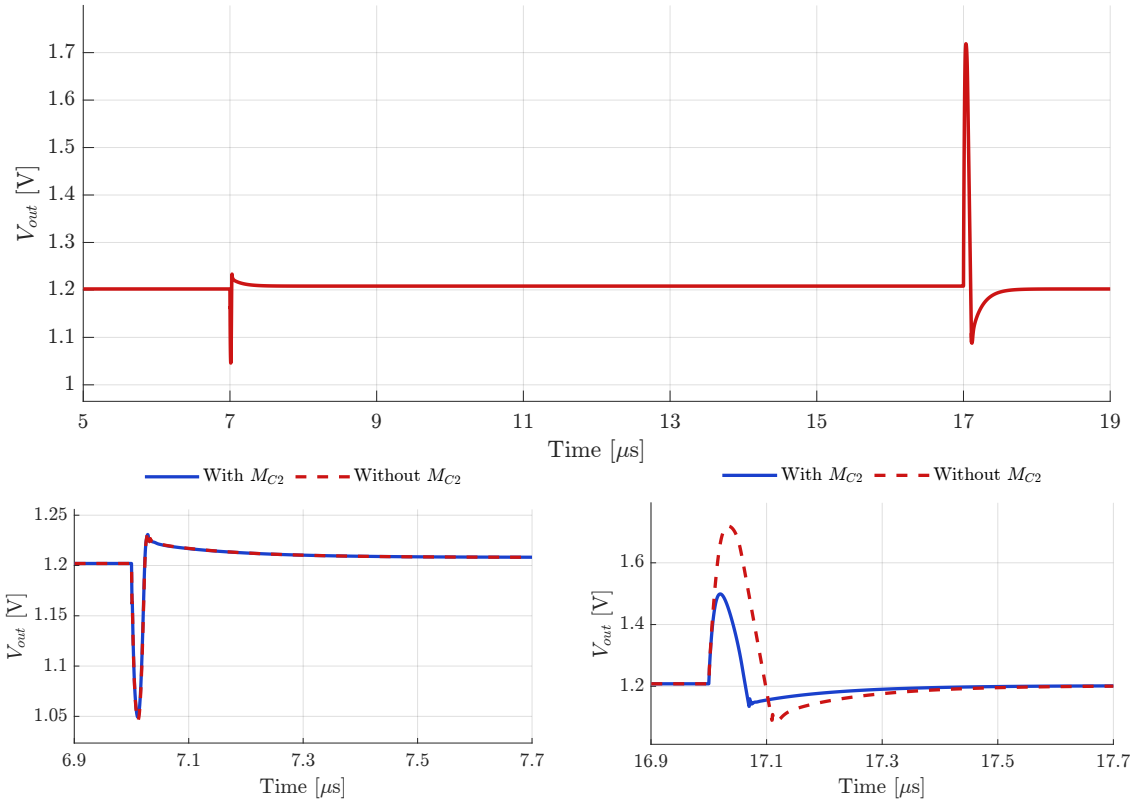


Figure 5.27: Final FVF-LDO schematic.

The role of this branch is illustrated in Fig. 5.28, which shows the transient response without M_{C2}. The load-current range and step amplitude are the same as in Fig. 5.26: a 10–50 mA step with 1 ns rise and fall times. Without M_{C2}, the regulator cannot counteract the rapid load decrease quickly enough, and the output voltage rises to nearly V_{DD}. This comparison highlights the importance of the added current-sinking branch in limiting overshoot for very short fall times.



(a) Undershoot comparison.

(b) Overshoot comparison.

Figure 5.28: Output-voltage transient response without M_{C2} and comparison with the response including M_{C2}.

5.5 Comparison with the State of the Art

The results presented in this chapter provide the basis for comparing the proposed PMOS FVF-LDO with representative regulators from the literature. Before examining individual performance metrics, it is important to recall the requirements that guided the design. The target application calls for load transitions between 0 and 50 mA with rise and fall times of 100 ns, while keeping the output-voltage deviations below 8%. The simulations also show that the LDO maintains output regulation at higher load currents, up to slightly above 300 mA, although this extended range was not a requirement of the target application. The additional tests with faster transitions explore the transient limits of the regulator beyond the specified rise and fall times.

LDOs reported in the literature address different applications and make different trade-offs between transient response, quiescent current, dropout voltage, and output capacitance. As illustrated by the preceding simulations, even steps of equal amplitude can produce different responses when their load-current endpoints differ.

Among the reviewed designs, no LDO was identified that uses the same technology, supply voltage, output capacitance, and load conditions as the proposed regulator. A direct comparison under identical conditions is therefore not possible. The selected references are mainly FVF-based LDOs designed for high bandwidth and a robust transient response, which share the main objectives of this work despite differences in their implementation and operating conditions.

The comparison is presented in Table 5.1. Under the listed test conditions, the proposed LDO stands out particularly for its small overshoot and undershoot. It also exhibits good nominal stability: the fast-loop phase margins are 86.7° and 62.8° at minimum and maximum characterized load, respectively. The results of this work include the performance degradation caused by the parasitic network and the damping measures required to preserve stability, which reduce the maximum-load bandwidth from 133 to 81.9 MHz. The other simulation-based designs in the comparison do not include this parasitic-network analysis, except for [8], where these effects are also treated.

For the designs compared in Table 5.1, particularly those with higher bandwidths and limited nominal phase margins, PVT variations and parasitic effects could compromise stability. Their nominal results alone therefore do not guarantee stable operation under these conditions.

The imposed load edge time T_{edge} is distinct from T_R, which is estimated from the output-voltage excursion and is not a settling time. When $T_R \gg T_{\text{edge}}$, the load transition is approximately instantaneous relative to the regulator response, giving

$$T_R \approx \frac{C_L \Delta V_{OUT}}{\Delta I_{OUT}}$$

This assumes that the load capacitor initially supplies the full current step. If the regulator responds during a linear load ramp, the current imbalance is still increasing, and the finite-edge estimate is used:

$$T_R \approx \sqrt{\frac{2C_L \Delta V_{OUT} T_{\text{edge}}}{\Delta I_{OUT}}}, \qquad T_R < T_{\text{edge}}$$

Here, ΔV_{OUT} is the output-voltage excursion from the pre-step level used for the charge-based response-time estimate.

	[2]	[3]	[5]	[8]	[10]	[11]	**This work**
Year	2024	2019	2022	2025	2021	2023	**2026**
Technology [nm]	65	180	22	22	65	180	**12**
Process	CMOS	CMOS	CMOS	CMOS	CMOS	CMOS	**FinFET**
Pass transistor	PMOS	PMOS	PMOS	NMOS	PMOS	PMOS	**PMOS**
Topology	FVF	Conventional	FVF	FVF	FVF	FVF	**FVF**
Results	Simulated	Simulated	Simulated	Simulated	Measured	Measured	**Simulated**
V_{IN} [V]	1.2	2.4–4	1.05	1.15	1.2	0.7–1.1	**1.8**
V_{OUT} [V]	1.0	2.2	0.9	0.9	1.0	0.6	**1.2**
C_L [nF]	0.3	0.1	NR	1	0.3	0.12	**1**
I_Q [μA]	110	70	11	400	27–82	0.22–660	**650**
UGF [MHz]	1–309	4.9–28	0.35–128.28	14–161	0.7*–436	NR–100*	**40.4–81.9**
Phase margin [°]	66	47 / 81	> 81	55 / 77	> 59	> 49*	**86.7 / 62.8**
$I_{L,\min}$ [μA]	0	0	10	100	5	10	**0**
$I_{L,\max}$ [mA]	20	50	20	200	20	30	**50**
Transient load [mA]	0–20	0–50	0.1–10	20–80	0.1–20	1–25	**0–50**
ΔI_{OUT} [mA]	20	50	9.9	60	19.9	24	**50**
US [%]	7.40	10.45	4.30	6.70	5.90	35.83	**1.88**
OS [%]	5.60	7.73	2.78	4.00	7.10	10.50	**0.94**
T_{edge} [ns]	0.01	100	300	1	0.8	100	**100**
T_R [ns]	1.11	9.59	NR	1.35	0.90	14.66	**9.60**

Table 5.1: Comparison of this work with state-of-the-art high-bandwidth LDOs

* Estimated from the figure in the cited work.

Chapter 6

Conclusions and Future Work

The aim of this work was to design a PMOS capless LDO in a 12-nm FinFET technology, providing a 1.2 V output from a nominal 1.8 V supply for load currents up to 50 mA. The design specifications required overshoot and undershoot below 8% for load transitions between 0 and 50 mA with 100 ns edges.

A dual-loop FVF architecture was chosen to combine accurate DC regulation with a fast response to load changes. The slow loop sets the output voltage, while the local FVF loop corrects rapid voltage deviations. Zero-pole tracking compensation preserves fast-loop stability as the output pole moves with load current.

Including parasitic effects, the nominal fast-loop bandwidth is 40.4 MHz at 1 μA and 81.9 MHz at 50 mA, with phase margins of 86.7° and 62.8°, respectively. This bandwidth, together with the compensated loop response, allows the regulator to limit undershoot to 1.88% and overshoot to 0.94% for the specified load step with a 1 nF load capacitance. These nominal results demonstrate excellent transient performance, with both voltage deviations well below the limit, while retaining good stability margins.

Reaching this result required multiloop analysis, DC and transient simulations, and PVT checks. The architecture, device sizing, and compensation were refined iteratively as these analyses revealed the limitations of each design choice. Particular attention was given to the parasitic network, which is often neglected but can introduce resonances and compromise stability. Accounting for these effects helped determine the required damping and compensation, bringing the simulated response closer to the regulator's actual behavior.

Future work will focus on a more detailed study of the parasitic network to identify which elements have the greatest impact on stability and transient response, and refine the compensation and damping choices. Further work could address power-supply rejection, which was not evaluated in this thesis, and investigate ways to improve the PSRR. It could also explore how far the dropout voltage can be reduced while

maintaining output regulation. The PMOS pass device offers an advantage here, since it does not require an additional, higher-voltage supply to drive the gate, as an NMOS implementation would need. Finally, adaptive biasing could reduce current consumption by adjusting the internal bias currents to the load and transient demand. This would allow the regulator to save power when less drive current is needed, while retaining sufficient current for rapid load changes. Such a strategy would need to preserve the stability and transient response achieved by the present design.

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