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Architectural Exploration and Trade-off Analysis of Power Management Solutions for Automotive Matrix Headlamps

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Abstract

This thesis presents a study on possible methods for driving an automotive headlamp from the vehicle battery, with the goal of finalizing a power management solution capable of supplying the LED matrix headlamp with its high current requirements. Beginning with a theoretical overview on voltage conversion techniques like DC-DC converters and low dropout regulators (LDO), this research continues with the choice of the blocks that will be put together in order to generate three different voltage rails, required for the analog, digital and power core of the headlamp system, concluding with the analysis of the performance of the system in terms of efficiency and size. TSMC 180 nm BCD technology will be used for the transistor level implementation. The components as well as the final structure of the entire system will be discussed on the basis of a series of trade-offs, and finally the system will be simulated.

Introduction

Modern electronic devices rely on a number of interconnected subsystems tied together to achieve certain functions. For example, in a smartphone, the screen, the speakers, the cameras and many more components need to be turned on at the same time in order for the whole package to work properly; every single piece of hardware requires its supply voltage, but that supply can differ among all the parts and, usually, the main source of power is a single battery able to output a single voltage, thus the need for voltage conversion mechanism like DC-DC converters and linear regulators has seen a heavy rise in recent years and these converters are present everywhere in the electronic world.
There exist two main macro classes for voltage conversion circuits (Fig. 1):

- Switching converters
- Linear regulators

As the name suggests, switching converters rely on switches (transistors, mainly MOSFETs and IGBTs) controlled by a series of pulses, with a certain phase delay between each other, and use reactive components like inductors and capacitors to store and release energy, in order to achieve the voltage conversion [4]. Aside from DC-DC converters which will be further investigated in this work, switching converters also include AC-DC, DC-AC and AC-AC converters.
Linear regulators rely instead on a pass element (again a transistor, be it MOSFET or BJT) between input and output, that can be controlled in order to vary its voltage drop and essentially regulate the output, by acting as a simple resistor. It should be noted that this type of linear regulator referred to as a voltage regulator (low dropout regulator if certain characteristics are met) is just one subcategory of linear regulators that also include voltage reference circuits, such as bandgap references, although their function is to generate a precise voltage rather than regulate power delivery to a load.
DC-DC converters (Fig. 3a) can achieve very high efficiencies; the main sources of power dissipation are the switches conduction and switching losses as well as the parasitic resistances of the reactive components, all of which are practically reducing the efficiency, but in the ideal theoretical case, are

reduced to zero (the same cannot be said for linear regulators which, even ideally, present high power dissipation). The problem is that due to high switching activity, electromagnetic interference (EMI) and noise are more pronounced. DC-DC converters can be of two types depending on the reactive components adopted:

- Inductor-based
- Inductorless (Switched capacitor / Charge pump)

The first type can achieve the highest efficiency using an inductor as the energy storing device; the inductor is usually the component that needs the most attention when designing this type of converter since it can be very bulky and expensive, leading first in the bill of materials (BOM). Inductor-based converters can deliver high currents and have a more continuous varying conversion ratio compared to the inductorless type. While a switched capacitor design can be fully integrated, its lower efficiency and higher output ripple may lead to the choice of the inductor-based design in certain applications, despite the latter disadvantage in cost and size. [5].

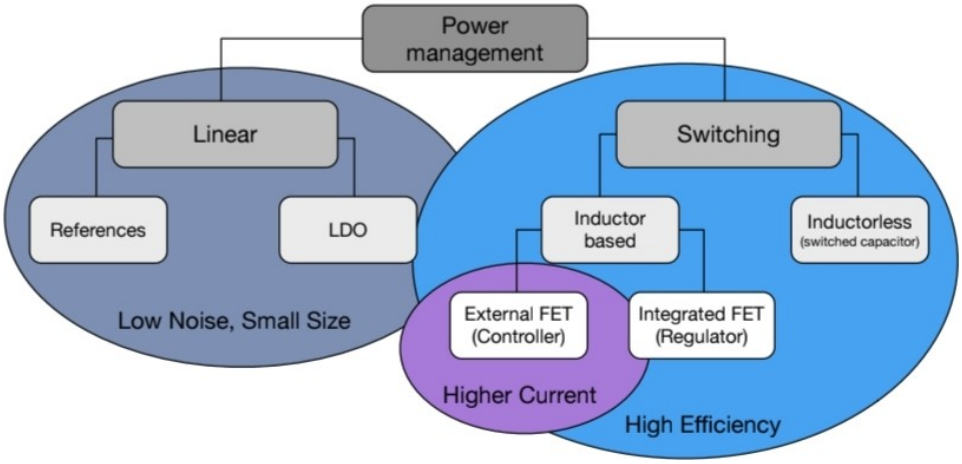


Figure 1: Classification of power converters.

The way the conversion happens in a DC-DC converter depends on the topology:

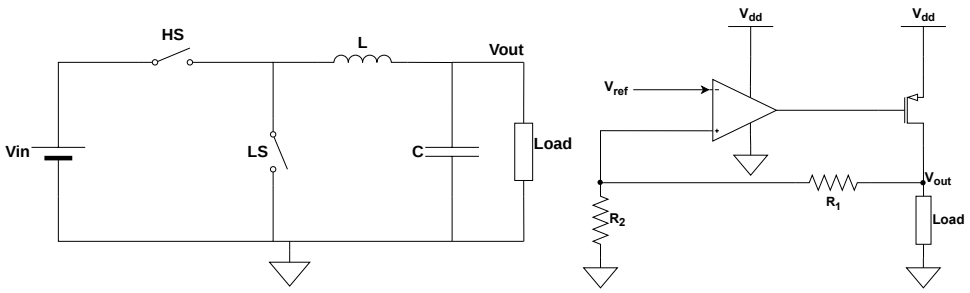
- Buck - voltage step down from input to output
- Boost - voltage step up from input to output

Other topologies exist in literature, but the aforementioned topologies are the two basic functions of a DC-DC converter, consisting of creating a voltage higher than the available supply, with a boost converter and a lower one with a buck converter.

	Linear Regulator	Switching Regulator	
		Inductive	Charge Pump
Efficiency	20-60%	90-95%	75-90%
Ripple	Very low	Low	Moderate
EMI Noise	Very low	Moderate	Low
PCB Area	Very small	Largest	Medium
Cost	Lowest	Highest	Medium

Figure 2: Summary of power converters performance.

A linear regulator (Fig. 3b), on the other hand, is less complex and expensive than its switching counterpart; it boasts very low output ripple and noise, since there is no switching activity that contributes to EMI, but there is one main issue: efficiency. In a voltage regulator, the voltage drop across the linear pass element between the source and the output translates directly into lost power; this loss is highly accentuated if the voltage drop is high. This may result in the need to use a heat sink and highlights the difficulty in using this type of regulator in high power applications. It is important to notice that, while in switching converters there is the possibility of stepping up the source voltage, in a linear regulator we talk only about a "voltage drop"; that is because this type of regulator can only step down a voltage and there are no complementary versions able to step it up.
Since conditions in the system may change due to a lot of variables (i.e. temperature), power converters use a control feedback loop in order to stabilize the output voltage against said variable conditions. The control loop will not be studied as it is outside the scope of this work.
A general performance overview of power converters is summarized in Fig. 2.



(a) (b)

Figure 3: (a) An inductor-based buck converter with ideal switches; the feedback control loop is not shown. (b) An LDO regulator using a PMOS transistor as the pass element.

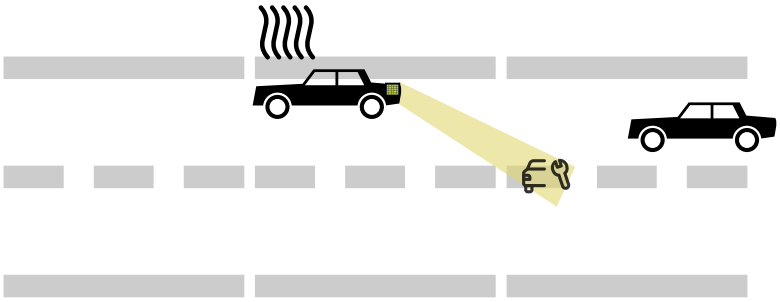
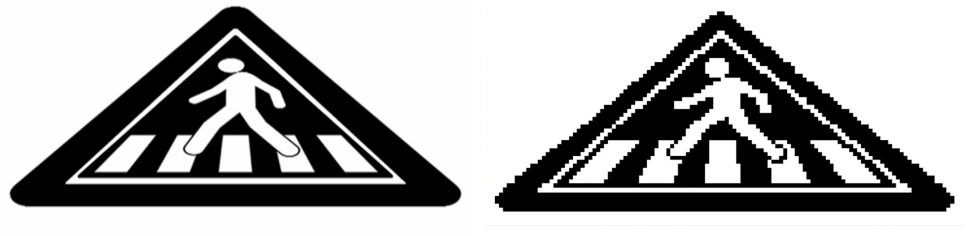


Figure 4: A possible application of matrix LED lamps: warning signs for other vehicles on the road are projected.

This thesis, conducted in collaboration with ams OSRAM, has the aim of designing a solution to drive an automotive matrix LED headlamp from a 12 V automotive battery while maximizing efficiency.
In recent years, the automotive sector has introduced many smart features in modern cars, starting with advanced driver assistance systems. Lighting is one aspect that can help the driver in numerous ways. The level of auxiliary functions that a lighting system can deliver is directly associated with how much performance the lighting system itself can achieve.
In a matrix LED headlamp, the array of LED lights can be controlled by blocks of pixels in the matrix or even up to a single pixel. The beam of light can be steered with high accuracy and depending on the matrix resolution, some pixels can be turned on or off or dimmed to reduce glare to other oncoming drivers on the road, projecting images to send messages to other drivers (Fig. 4) or warning the driver by continuously displaying information and signs on the road [6].
LED lights guarantee better efficiency and life cycles compared to other technologies as well as lower CO_2 emission [7].
Old automotive LED headlamps are arranged in strings, but that leads to a large voltage supply, since the voltage required for a string with n number of LEDs is n times the forward voltage of a single LED. A matrix layout is better, since all LEDs can be supplied even at low voltages. A matrix arrangement can also achieve high pixel resolutions, that can be useful for better quality of projection (Fig. 5) and illumination, shining light even in blind spots of the driver.
By integrating the matrix LED unit with a variety of sensors, the light emission of the headlamp can become "road adaptable", changing with road conditions, traffic and environmental aspects, being able, for example, to automatically turn on the fog lamp, when high humidity is detected [8].



(a) (b)

Figure 5: A high resolution matrix LED unit can project high quality images on the road: (a) High resolution matrix, (b) low resolution matrix.

Overall, matrix LED headlamps can improve driver safety and enhance the driving experience by providing a lot of information to the driver directly on the road and adapting automatically to weather conditions.
To maintain this performance, the matrix unit requires high power and high efficiency for driving the LEDs, but not only that: aside from the power core to drive the matrix itself, the unit needs supply to the analog and digital section that will complete the headlamp system.
The voltage required to supply the headlamp system is lower than the automotive battery, thus the analysis is conducted on buck converters and linear voltage regulators, in order to step down the source to the required voltage of the LED lamp. This required voltage is not a single one, but a set of three different voltages needed for the analog, digital and power section of the LED matrix unit and hence the scope of this thesis: to define the entire structure sitting in between the car battery and the headlamp unit.
In Chapter 1, possible structures for driving the LED are presented with their trade-offs, leading to the chosen solution. Chapter 2 presents the design and implementation of the power supply blocks developed for the analog section, describing their architectures, operating principles, and key design considerations. Chapter 3 and Chapter 4 focus on the power supply generation circuits for the power and digital sections, respectively, detailing the adopted solutions and their specific requirements. Finally, the obtained results are presented and discussed to assess the overall performance of the proposed design.

Chapter 1

Definition of the power management structure

Modern vehicles are becoming increasingly smart; after automatic parking and self driving, lighting is an aspect that is becoming more intelligent. Matrix LED headlamps mounted on a car can make use of individual pixels in order to steer a beam of light, project visuals on the road, or dim the brightness when other cars are incoming. The applications of smart lighting are vast, but how are such high power lamps supplied in automotive application? This section will detail some possible solutions to supply a matrix LED headlamp with particular attention to the system efficiency.

1.1 Supply of the matrix LED unit

The unit in question is a high power lamp in development by ams OSRAM. The requirements for its supply are listed below:

- VDD_p: 4 V - 25 A
- VDD_a: 3.3 V - 2 A
- VDD_d: 1.8 V - 10 mA

In Fig. 1.1, VDD_p is tied to the power section of the LED unit; this rail must be able to provide the power needed to turn on every pixel of the matrix at full brightness. Given the high current involved, this section will be the most problematic, requiring a keen eye on power dissipation, since even a small percentage of dissipation from the total power, directly translates into the device heating up. Consequently, the power section cannot allow suboptimal efficiency.
VDD_a supplies the analog section of the unit and has a lower demand in terms of power. In the analog section, some voltage references for the system are generated.

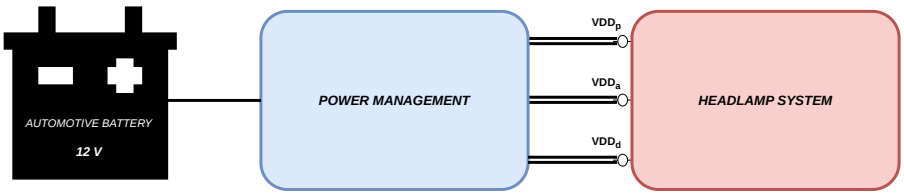


Figure 1.1: A schematic view of the power management structure driving the headlamp.

VDD_d is the digital rail; it is by far the least demanding supply, but the design must be heavily centered on robustness and stability against any variable conditions like temperature, load and line fluctuations, in order to maintain the controlling unit of the LED matrix functioning properly.
The three rails at the output of the power management are all lower than the 12 V vehicle battery; a DC-DC buck converter or a linear voltage regulator is essential, but should all three outputs come from a buck converter or should the linear type be used? or better: is there a way to use a single mechanism to build all the outputs?

1.2 SIMO DC-DC architecture

Single inductor multiple output DC-DC (SIMO) are a type of inductor-based DC-DC converters that make use of a single inductor to generate multiple output voltages from a single source [9]. As mentioned in the previous chapter, in inductor-based DC-DC, the inductor is the most important component; having to generate three outputs with three different DC-DC converters can significantly increase the size of the system, especially since, if high power is required, the inductor is even bulkier. The SIMO topology introduces a great advantage in this regard, allowing the designer to use only one inductor which will be time-shared between the multiple loads. Multiple outputs require replicating the switch on the load side; if no switches are present on the load side, like in the SIMO buck converter in Fig. 1.2, a new switch is added for every new load.
While the reduction in size due to the presence of a single inductor is a great achievement, there are many drawbacks to consider when opting for a SIMO topology:

- Time sharing of the inductor can become an issue when the switching period is small and there is the need of guaranteeing the proper disoverlap between the switches, in order to avoid an instantaneous current path to ground.

- Cross regulation between outputs must be taken into account because

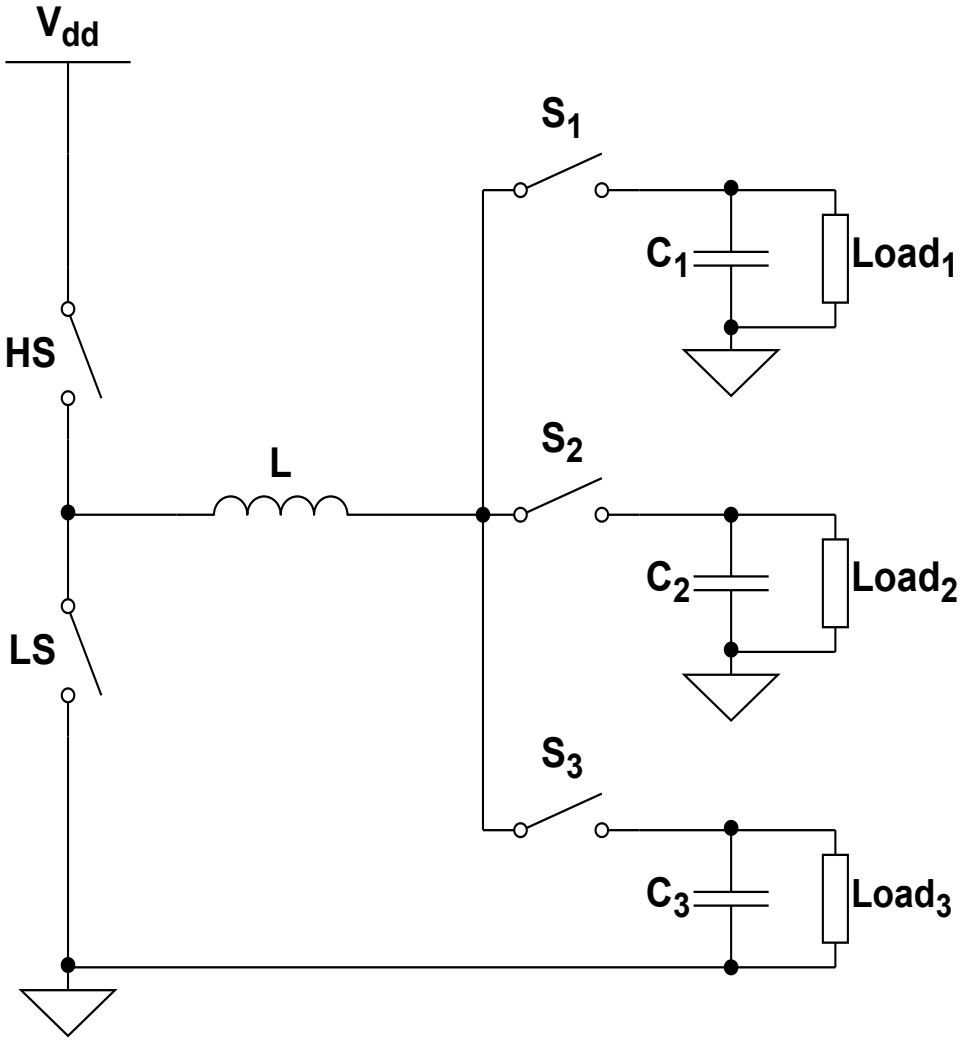


Figure 1.2: A SIMO DC-DC buck converter with 3 outputs.

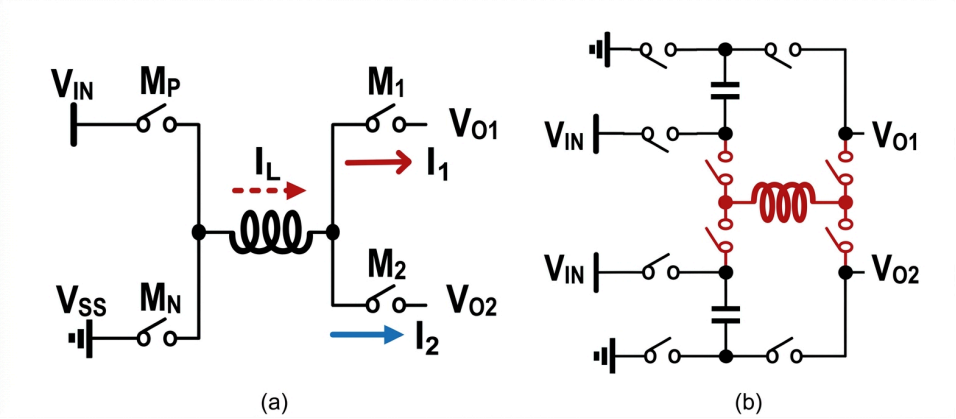


Figure 1.3: Schematic of a SIDO buck converter: (a) conventional SIDO topology; (b) dual path topology.

the power delivery to one load can affect the other loads.

- The feedback control to ensure stability, becomes a multi-loop control.

Furthermore, SIMO seems not to be suitable for driving high currents. In [10], a dual path topology is studied for a SIDO (double output) converter (Fig. 1.3): an auxiliary capacitor is switched in parallel to the inductor, in order to carry some of the load current, increasing in this way, the load current without increasing the inductor size, but still, the currents involved are far from the headlamp target.
In the LED matrix case the three outputs of the SIMO would be having very different performance in terms of load current; even assuming that a high current could be delivered to the power core, the mismatch in requirements between the loads, hints that the SIMO approach is not the right direction. Given the importance of the supply of the power section, it would be wiser to design a system that is custom made for this purpose, instead of building a multiple output system and tweaking it to satisfy all. This way the choice of the switches, the inductor and the switching frequency, is free from the other supply sections of the unit.

1.3 Possible implementations

Having established that the VDD_p rail is not to be part of a SIMO DC-DC design, a number of possible implementations are still left to be scrutinized. First of all, the VDD_a and VDD_d could still be implemented as a SIDO DC-DC structure; VDD_p will be either a buck or a linear converter. Knowing that the linear regulator behaves in a worse manner, efficiency wise, compared to a DC-DC, in high power application, the choice is trivial. Fig. 1.4 illustrates this first possible solution.

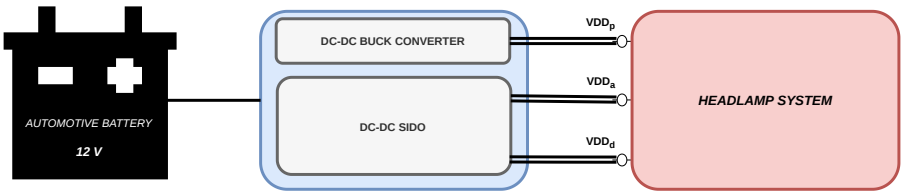


Figure 1.4: A possible power management solution: a buck converter and a SIDO generate the output voltages.

Making use of two single inductor single output (SISO) buck converters instead of the SIDO configuration, for the analog and digital section, is also feasible, since the unbalanced requirement of load current is still an issue, even for VDD_a and VDD_d. This second option, illustrated in Fig. 1.5, is valid but seems like a poor choice in terms of size of the system.
The digital core of the matrix LED unit is controlling the pixel array: it is important to have good stability for this section, thus a linear regulator, with its more accurate analog performance (output ripple and noise) would be a great choice to drive the digital part of the LED unit.
Since the power needed for the digital part is minimal, a lower efficiency is not a heavy issue. That said, it is not advisable to connect the linear regulator input to the 12 V automotive battery.
Linear voltage regulator experience a significant efficiency degradation when the voltage difference from input to output increases; given that VDD_d is 1.8 V, driving the linear regulator from the 12 V battery is a no go. The solution is to drive the regulator from VDD_p or VDD_a. If VDD_p is chosen, then an issue arises: since VDD_p is very power hungry, it may be turned off when not required. This means that to power on the digital core, the power core needs to be already on beforehand, but that is not always the case. Obviously this problem is to be avoided. Connecting input to VDD_a is a far better choice, given that the analog section should always be working and also, this rail is at a lower voltage than the power rail, giving a boost in performance, due to the lower voltage difference from input to output of

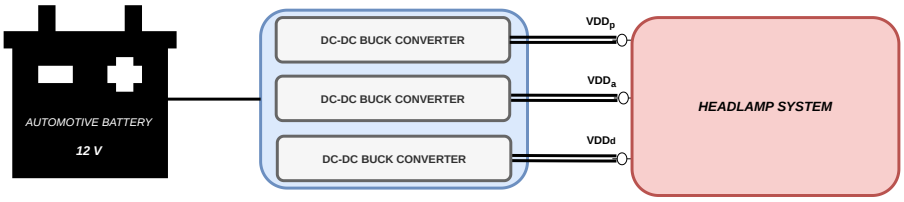


Figure 1.5: Second power management solution: three different buck converters generate the different supplies.

the regulator.
Established the need of a linear regulator for VDD_d, we are left with two options (Fig. 1.6) with regard to the analog section: a simple buck converter to generate VDD_a or an LDO (this regulator would be an LDO, because the voltage difference from its input, which is VDD_p, and the 3.3 V output, is just 700 mV).
Let us analyze mathematically the efficiency of the analog supply when the LDO architecture is used (Fig. 1.6b):

- $V_{in} = VDD_p = 4V$
- $V_{out} = VDD_a = 3.3V$
- $Iload = 2A$
- $P_{load} = V_{out} \times I_{load} = 6.6\,\mathrm{W}$

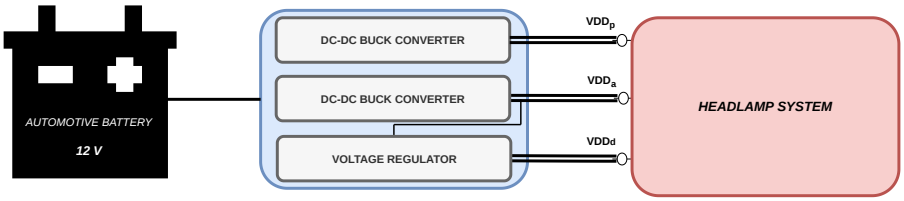
Below is the efficiency equation that can be used for the LDO, when the quiescent current is negligible:

$$\eta = \frac{P_{load}}{P_{in}} = \frac{P_{load}}{P_{load} + P_{diss}} \tag{1.1}$$

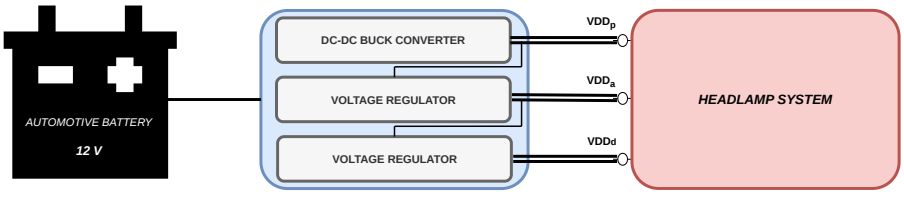
The voltage difference from input to output will be:

$$\Delta V = V_{in} - V_{out} = 700\,\mathrm{mV}$$

The dissipated power will be:



(a)



(b)

Figure 1.6: Alternative power management solutions: (a) VDD_a is generated by a buck converter; (b) VDD_a is generated by an LDO.

$$P_{diss} = \Delta V \times I_{load} = 1.4\,\mathrm{W}$$

Now the efficiency of the analog section would be:

$$\eta_a = 82.5\,\%$$

Notice that for different values of the load current that may be lower than the maximum 2 A, the efficiency will not change, in fact Eq. 1.1 may be rewritten as follows:

$$\eta = \frac{V_{out} \times I_{load}}{V_{in} \times (I_q + I_{load})}$$

Where I_q is the quiescent current for the amplifier embedded in the regulator, which is usually negligible; This way the term I_{load} cancels out and the efficiency in the LDO depends just on the input and output voltage.

$$\eta = \frac{V_{out}}{V_{in}} \tag{1.2}$$

η_a of 82.5 % is not a bad result, but there are two reasons why it is better to opt for a buck configuration for the analog section:

1. The LDO would be supplied by VDD_p which may not always be turned on; this is the same issue mentioned for the digital section regulator.
2. A DC-DC converter could still yield a better result; This will be confirmed true, later in Chapter 2.

1.4 Chosen solution

Given all the reasons presented, the finalized power management structure from Fig. 1.1 has been updated to the one in Fig. 1.7.
The chosen full structure is as follows:

- A SISO DC-DC buck converter for VDD_a.
- A linear voltage regulator for VDD_d.
- A multiphase DC-DC buck converter for VDD_p.

Each section will be discussed in a dedicated chapter and the reason for the use of a multiphase DC-DC, will be later explained.

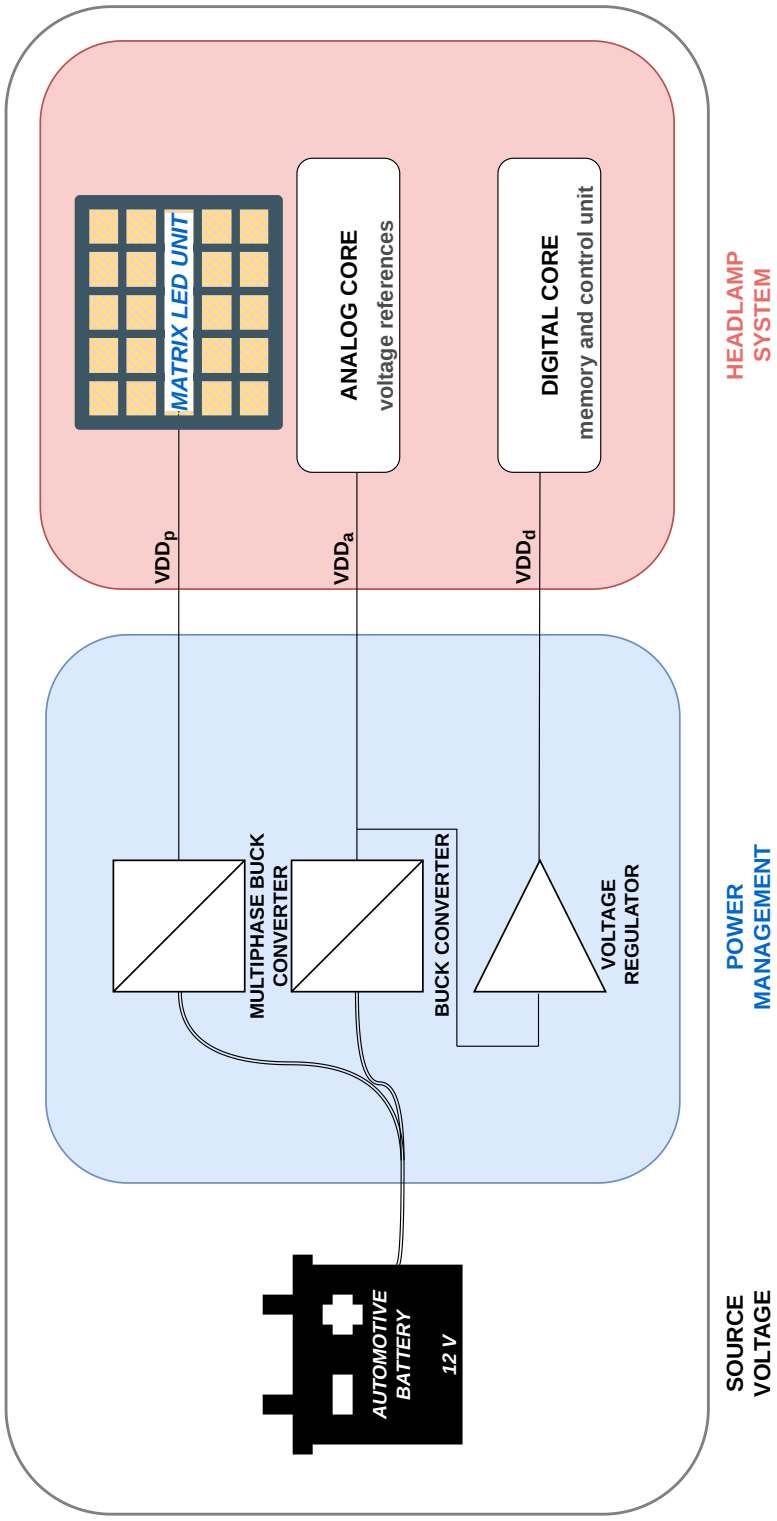


Figure 1.7: Chosen power management solution for driving the LED matrix.

Chapter 2

Analog domain power supply: architectural analysis and implementation

This chapter is dedicated to the analysis of the architecture that will supply the analog core of the headlamp system with the VDD_a rail.

2.1 DC-DC buck converter working principle

An inductor-based DC-DC buck converter is a voltage step-down switching converter, that in its simplest form is composed of:

- Two switches that form a half bridge configuration
- An inductor
- A capacitor

In Fig. 2.1a the input DC voltage source is applied to the top switch, called the high side switch (HS); this switch turns on and off at given intervals of time and so does the bottom switch, the low side (LS). This will generate a square waveform at the phase node in between the high side and low side switches, because of the constant switching between the input voltage and ground potential; this waveform will have a DC value given by the mean of the square wave, which is directly correlated to how much time the high side switch is turned on, parameter defined as the duty cycle (D). This way a node with a lower DC value than the input applied one, has been generated. The voltage at the phase node is still a square wave and not the DC value that is expected, so the next move is to extract this DC voltage thanks to a filter and that is the role of the inductor and the capacitor in Fig. 2.1b. The inductor and capacitor are a better choice than an RC filter due to the fact that these are reactive components, which, ideally, do not dissipate power.

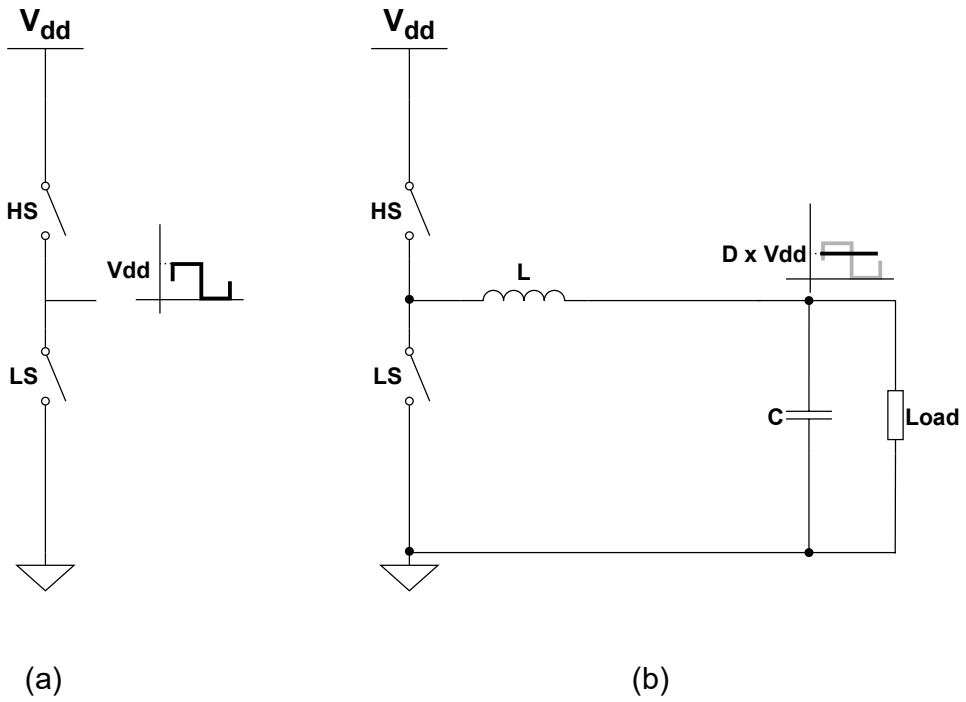


Figure 2.1: Buck converter configuration. (a) A half bridge creates a square waveform on the phase node, with a given duty cycle. (b) This waveform is filtered by the inductor and the capacitor to extract the DC voltage.

2.1.1 Buck converter half bridge

An ideal switch does not lead to any power loss: when the switch is on, the voltage across it is zero and when the switch is off, the current flowing through it is zero. In a real implementation though, the situation is quite different.
Let us analyze three different ways in which a buck converter half bridge may be implemented in reality.

- Asynchronous buck coverter

In this configuration the role of the high side switch is managed by a PMOS transistor, while a diode is used for the low side. When the PMOS is on, the current will flow through it, from the source to the inductor and when it turns off, since the inductor current is continuous, the diode will carry the inductor current; in order for this to happen, the phase node will go negative so that the diode may turn on. Only the high side will need a driver, while the low side diode will act accordingly, thus the asynchronous behavior.

- Synchronous CMOS buck converter

This time the high side still makes use of a PMOS, but the low side is replaced by an NMOS transistor; both switch will be driven by complementary phases, so that when one side is off, the other will be on.

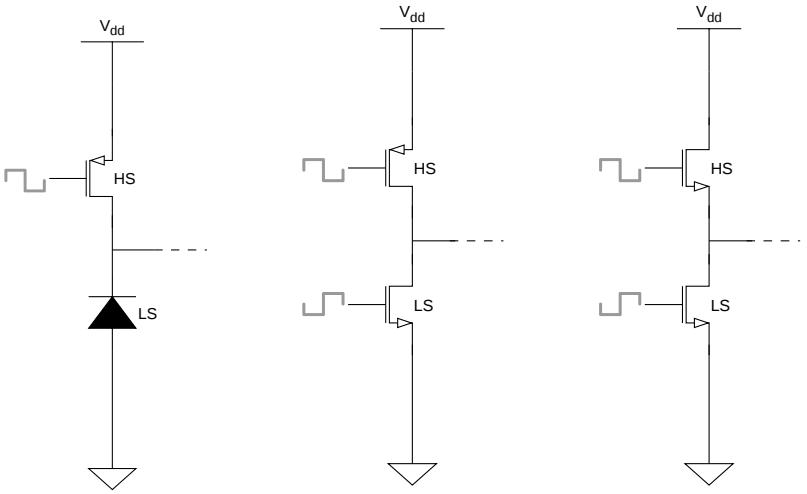
- Synchronous double NMOS buck converter

This configuration uses two NMOS transistor for both the high side and low side of the bridge. A high side NMOS is more difficult to drive than the complementary PMOS, but gives a huge advantage in terms of size and on-resistance (R_{on}).
These three configurations are illustrated in Fig. 2.2.
In order to understand which configuration to use in the design, let us introduce the buck converter conduction losses.
Conduction losses are due to power dissipation in the high and low side of the bridge, when current flows; as mentioned before, ideal switches do not dissipate power, but transistors and diodes do.
The power dissipation in a diode is:

$$P_d = V_f \times I_{load} \tag{2.1}$$

Where V_f and I_{load} are the voltage across and the current through the diode.
The power dissipation in a transistor is:

$$P_d = R_{on} \times I_{load}^2 \tag{2.2}$$



(a) (b) (c)

Figure 2.2: Half bridge configurations in a buck converter. The high side and low side are implemented as: (a) PMOS and diode, (b) PMOS and NMOS, (c) two NMOS.

Where R_{on} and I_{load} are the transistor on-resistance and current.
Given Eq. 2.1 and 2.2, a synchronous configuration becomes the better choice when:

$$R_{on} \times I_{load}^2 < V_f \times I_{load} \tag{2.3}$$

The asynchronous configuration is the simplest one to design, but the diode forward voltage can lead to considerable power loss, when high current flows through the diode. Replacing the diode with a transistor may greatly reduce this loss. In fact a transistor used in the triode region, behaves like a switch with a certain resistance; if this resistance is small, the power dissipated on the switch becomes low. This also hints to the advantage of using two NMOS instead of a PMOS and NMOS configuration. NMOS transistors have a lower R_{on} compared to PMOS of the same size. Under high current operating conditions, transistors must be very wide to achieve low R_{on} and reduce power consumption; in this case, a PMOS would be prohibitive in terms of area consumption. Using a double NMOS configuration comes with a drawback though. When an NMOS is used as the high side, the phase node is the source terminal of the transistor; the phase node should rise up to V_{dd} when the high side turns on, but in order to have the high side on, the NMOS should have a voltage equal to its source plus a transistor V_{GS}, on its gate terminal. If the maximum voltage allowed to the gate is V_{dd}, the high side will not turn on and the converter will not work as intended. To solve this issue, the double NMOS configuration requires a bootstrap/charge pump circuit to supply the high side gate with a voltage higher than V_{dd}.

2.1.2 Buck converter ripple and waveforms

The duty cycle of the high side switch is directly transferred to the square wave on the phase node. It is easy to see that the mean value of this square wave is related to the duty cycle, hence at the output, after the square wave is filtered, the retrieved DC voltage is the following:

$$V_{out} = D \times V_{dd}$$

The conversion ration of the buck converter is then:

$$\frac{V_{out}}{V_{dd}} = D \tag{2.4}$$

Which is exactly the duty cycle of the converter.
In reality the inductor and the capacitor are not able to filter the phase node waveform down to just its DC value; that is not possible with a real filter. As a consequence, the output voltage is not a perfect DC value, but it will have some ripple on top of it. This is not just an output voltage

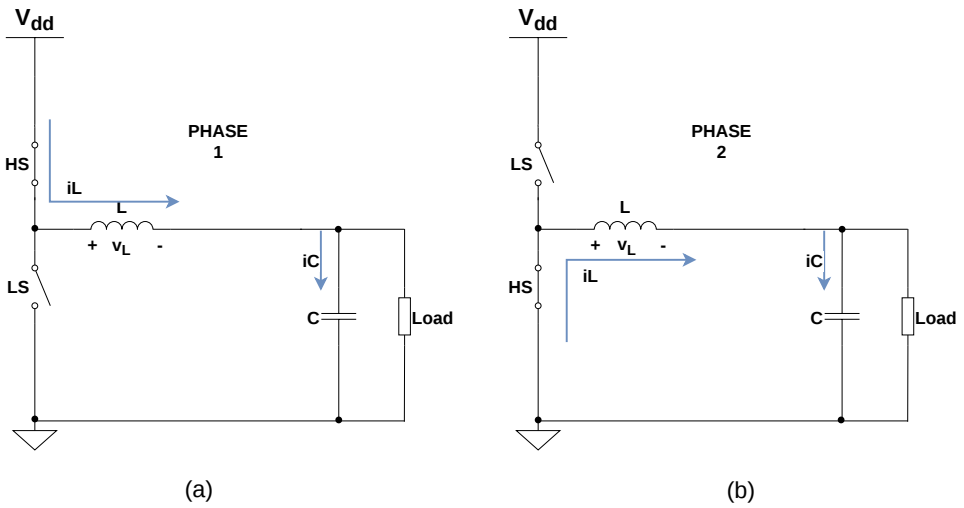


Figure 2.3: The two phases of operation of a buck converter. (a) In phase 1, the high side switch is on and the inductor is connected to V_{dd}. (b) In phase 2, the low side is on and the inductor is grounded.

phenomenon, as it also happens to the inductor current, which will have a ripple current on top of its DC value.
In order to further analyze the behavior of the buck converter, let us introduce an important assumption:

- Small ripple approximation [11]

With the small ripple approximation, it is assumed that the output ripple voltage is small compared to its DC value and thus it can be neglected (later this same ripple will be calculated).
Let us now analyze the two phases at which the converter operates. Fig. 2.3 illustrates the operation.
Neglecting the ripple, the output voltage is constant at V_{out}.
In phase 1, when the high side switch is on (low side off), the voltage across the inductor is:

$$v_L = V_{dd} - V_{out}$$

The current in the inductor is related to the voltage across it, by the following equation:

$$L\frac{di_L}{dt} = v_L \tag{2.5}$$

So in this case:

$$\frac{di_L}{dt} = \frac{V_{dd} - V_{out}}{L}$$

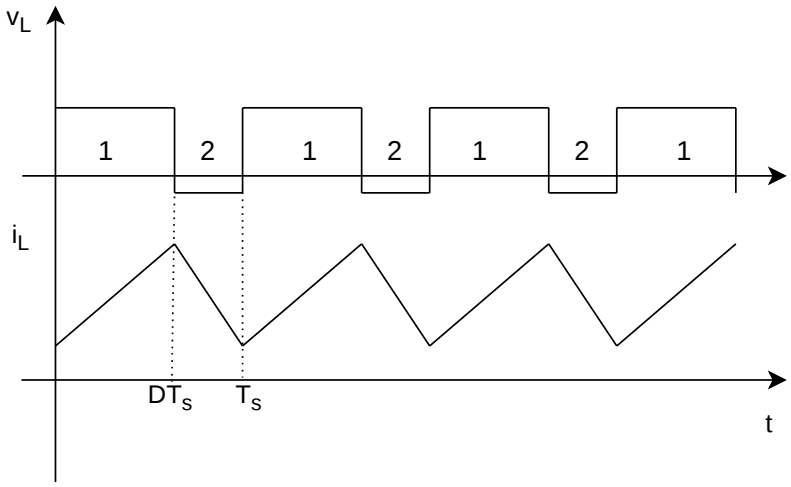


Figure 2.4: The inductor voltage and current waveforms. The voltage is a square wave with duty cycle D, switching from positive to negative values. The current is a triangular waveform with a positive DC value and a superposed ripple.

In phase 2, when the low side is on (high side off), the inductor is now grounded; The voltage across it is:

$$v_L = -V_{out}$$

And:

$$\frac{di_L}{dt} = \frac{-V_{out}}{L}$$

With these few information we can plot the inductor and voltage currents graphs in the two phases of operation.
$\frac{di_L}{dt}$ represents the slope of the inductor current and that is why in Fig. 2.4 the inductor current appears as a triangular waveform; in fact since small ripple approximation is taken in account, the slope of the inductor current is constant in both phases, but with opposite sign, leading to a rising and a falling line in each phase.
This behavior is assuming that the converter is working in steady-state conditions. In that case the inductor current shows a periodic behavior where it can be stated that:

$$i_L(nT_s) = i_L((n+1)T_s) \tag{2.6}$$

Where T_s is the switching period of the converter.

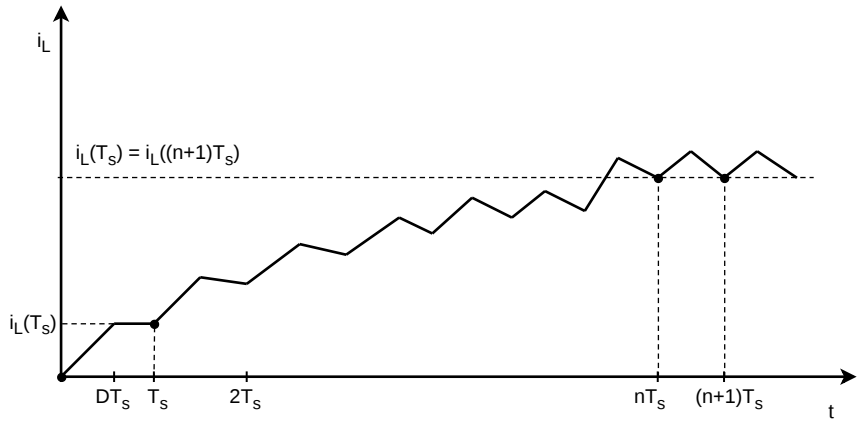


Figure 2.5: Inductor current behavior from turn-on to steady-state.

During turn-on, the converter is not in steady-state. Since the capacitor is assumed as completely discharged at the beginning of turn-on, the inductor current will rise up very fast at phase 1 of the first switching period, with a higher than steady-state slope, and in phase 2, the falling slope is close to zero. With time, the capacitor charges up and the output voltage rises; this way, the slope in phase 1 decreases, while the slope in phase 2 becomes higher in magnitude. This continues till the converter arrives at a point where the inductor current, in a period, rises as much as it falls (Eq. 2.6 now holds on). The converter now is in a periodic stage or else it is in steady-state. The behavior of the inductor current from turn-on to steady-state is illustrated in Fig. 2.5 for better visual understanding.
Steady-state condition results in two important principles in DC-DC operation:

- Inductor Volt-second balance
- Capacitor Amp-second balance

From Eq. 2.5if v_L is integrated over the switching period we get:

$$\frac{1}{L}\int_0^{T_s} v_L\,dt = i_L(T_s) - i_L(0)$$

This amounts to zero in steady state:

$$\int_0^{T_s} v_L\,dt = 0$$

The name of this principle comes from the $V \times s$ unit of this integral.
Dividing both sides by the switching period gives:

$$\frac{1}{T_s}\int_0^{T_s} v_L\,dt = 0$$

Which is the average of the inductor voltage.
The inductor Volt-second balance states that in a DC-DC converter working in steady-state, the average inductor voltage is zero. This is useful to calculate parameters like conversion ratio of a converter.

$$< v_L >= 0 \tag{2.7}$$

A similar conclusion is achieved for the capacitor current, starting from Eq. 2.8.

$$C\frac{dv_C}{dt} = i_C \tag{2.8}$$

Integrating the capacitor current over the switching period:

$$\frac{1}{C}\int_0^{T_s} i_C\,dt = v_C(T_s) - v_C(0)$$

Equivalently to the inductor current, the voltage across the capacitor has the same value at multiple of the switching period. the result is then zero.

$$\int_0^{T_s} i_C\,dt = 0$$

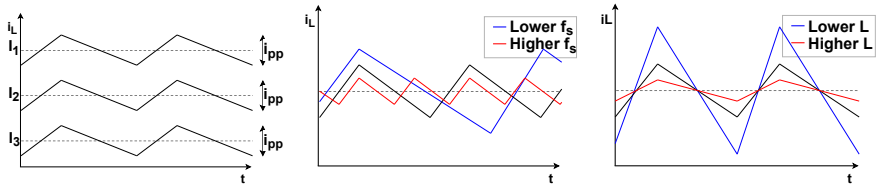
The unit of this integral is $A \times s$ and hence the principle name. Note that this unit has the dimension of an electric charge.
Dividing by the switching period:

$$\frac{1}{T_s}\int_0^{T_s} i_C\,dt =< i_C >= 0 \tag{2.9}$$

The result is the Amp-second rule, which states that in a converter working in steady-state, the average of the capacitor current is zero, meaning there is no net change in capacitor charge.
Assuming now the steady-state condition, the inductor ripple current can be calculated. Looking at the graph in Fig. 2.4 and multiplying the slopes by the duration in which they are active, the peak to peak amplitude of the ripple will be:

$$i_{pp} = \frac{V_{dd} - V_{out}}{L} \times D \times T_s \tag{2.10}$$

Eq. 2.10 is very important in the design of the buck converter as it relates all the parameters that can affect the inductor ripple: the duty cycle, the frequency (switching period) as well as the value of the inductance are all responsible for the ripple.



(a) (b) (c)

Figure 2.6: Effect of a change in the following parameters on the inductor current: (a) load current, (b) switching frequency and (c) inductance value.

The effect of each parameter on the inductor current waveform is illustrated in Fig. 2.6.
Take a look at Fig. 2.6a: even if the load current is always positive, a big ripple value, may result in negative value of the inductor current, especially when the load current goes toward the minimum. Negative values of the current mean that the current is flowing back to the source and this is obviously an unwanted scenario. When this happens the converter should enter a discontinuous conduction mode of operation (DCM), instead of the normal continuous conduction mode (CCM). In DCM, a control mechanism in the feedback loop reacts when the current is about to become negative and the conduction stops, restarting only when the current achieves a positive value. Fig. 2.7 shows CCM and DCM operation.
Eq. 2.10 can be manipulated to address the choice of the inductance value in the design, in this form:

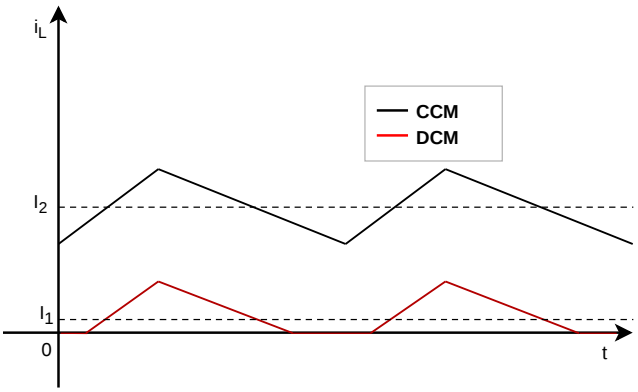


Figure 2.7: The two modes of operation of the converter: continuous conduction mode and discontinuous conduction mode. In DCM the negative side of the current is clipped by the feedback control loop.

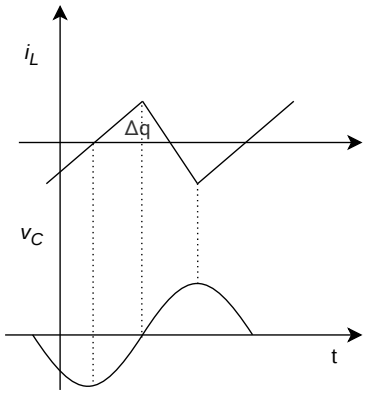


Figure 2.8: The capacitor voltage and current waveforms. A voltage ripple is present on top of the DC value due to limited filter capabilities.

$$L = \frac{V_{dd} - V_{out}}{i_{pp}} \times D \times T_s \tag{2.11}$$

What about the output voltage ripple? Remember that the small ripple approximation was used, but in this case, that leads to an absurd conclusion: the output ripple voltage is zero. Since this is not the correct conclusion, let us present the appropriate result. In Fig. 2.4 the inductor current flows to output through both the capacitor and the load: if the capacitor impedance is assumed to be much smaller than the load, at the frequency of operation, then the inductor average (DC) current will all go to the load, while the ripple will flow through the capacitor.

$$i_C = i_L - < i_L >$$

Where $< i_L >$ is the average of the inductor current. Notice that the capacitor current is exactly the inductor ripple current, as it is the inductor current without the DC value.
The capacitor current and voltage are plotted in Fig. 2.8. The relation of voltage and charge in a capacitor is:

$$q = C \times v_C \tag{2.12}$$

The charge can be extracted by integration of the capacitor current, which is trivial, as it is of triangular shape:

$$\Delta q = \frac{i_{pp}/2 \times T_s/2}{2}$$

The peak to peak ripple will then be:

$$v_{pp} = \frac{\Delta q}{C} = \frac{i_{pp} T_s}{8C} \tag{2.13}$$

Given Eq. 2.13, the parameters to control the output ripple are the value of capacitance and the switching frequency. Notice that i_{pp} is also in the equation, which means that the voltage ripple is directly dependent on the inductor current ripple.
For the value of the capacitance to achieve a certain ripple, Eq. 2.13 can be manipulated into Eq. 2.14.

$$C = \frac{\Delta q}{v_{pp}} = \frac{i_{pp} T_s}{8 v_{pp}} \tag{2.14}$$

2.2 Design of the buck converter in SIMPLIS

As the first step of the design, let us calculate the main parameters of the buck converter.

- Input voltage V_{in}: 12 V
- Output voltage V_{out}: 3.3 V

Given the input and output targets, the conversion ratio is already set as per Eq. 2.4, so the first choice of this design, the duty cycle, will then be:

$$D = \frac{V_{out}}{V_{in}} = 27.5\%$$

The flow of the design will be divided in two parts:

- Preliminary behavioral analysis with the SIMPLIS software
- A second step with Virtuoso software for an accurate simulation

2.2.1 Initial setup analysis

On the SIMPLIS software, the starting point is to use an idealized schematic of the converter, in order to verify the feasibility of the circuit and then, gradually adding a layer of non-idealities.
In this first setup the values of the components are the following:

- 10 µH inductor
- 1 µF capacitor
- 2 A load current generator

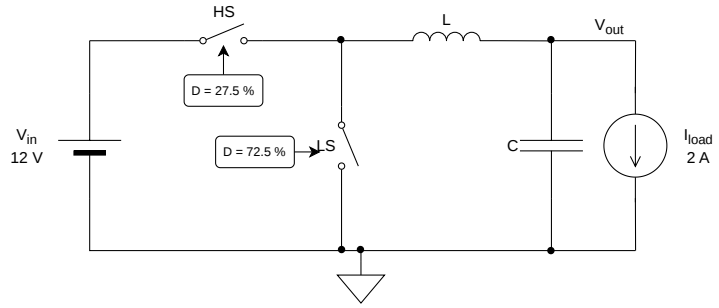


Figure 2.9: Schematic of the initial setup of the converter.

- Ideal switches for the half bridge, driven complementarily with a 27.5 % duty cycle at 1 MHz frequency.

In Fig. 2.10 the output waveforms of this setup (Fig. 2.9) are plotted: the inductor voltage and current seem to mirror perfectly the theoretical behavior. The output voltage is not a constant, but shows a ripple voltage, which is coming from the capacitor impedance, when the inductor ripple flows through. The DC value of V_{out} is 3.3 V, suggesting that the converter is working as intended, by stepping down the voltage with the correct conversion ratio.
In Fig. 2.10 the current and voltage ripple are also shown; let us calculate them by Eq. 2.10 and 2.13 and verify if the values are the expected ones:
The expected inductor current ripple is:

$$i_{pp} = \frac{12 - 3.3}{10^{-5}} \times 0.275 \times 10^{-6} \approx 240\,\text{mA}$$

And the expected output ripple voltage:

$$v_{pp} \approx \frac{0.24 \times 10^{-6}}{8 \times 10^{-6}} \approx 30\,\text{mV}$$

A good match can be seen between the theoretical values and this first simulation.
One important aspect extracted from 2.10 is that the inductor voltage has a zero average value; this confirms the inductor Volt-second balance rule in the buck converter.
The phase node voltage is plotted in Fig. 2.11: the waveform is a square wave switching between V_{in} and ground, at 1 MHz frequency, with the 27.5 % selected duty cycle. As shown in the plot, the resulting mean value of this waveform is the wanted DC output voltage.
Before continuing with the analysis of the switches to use and the timing of the phases, let us choose carefully the inductance and capacitance value for

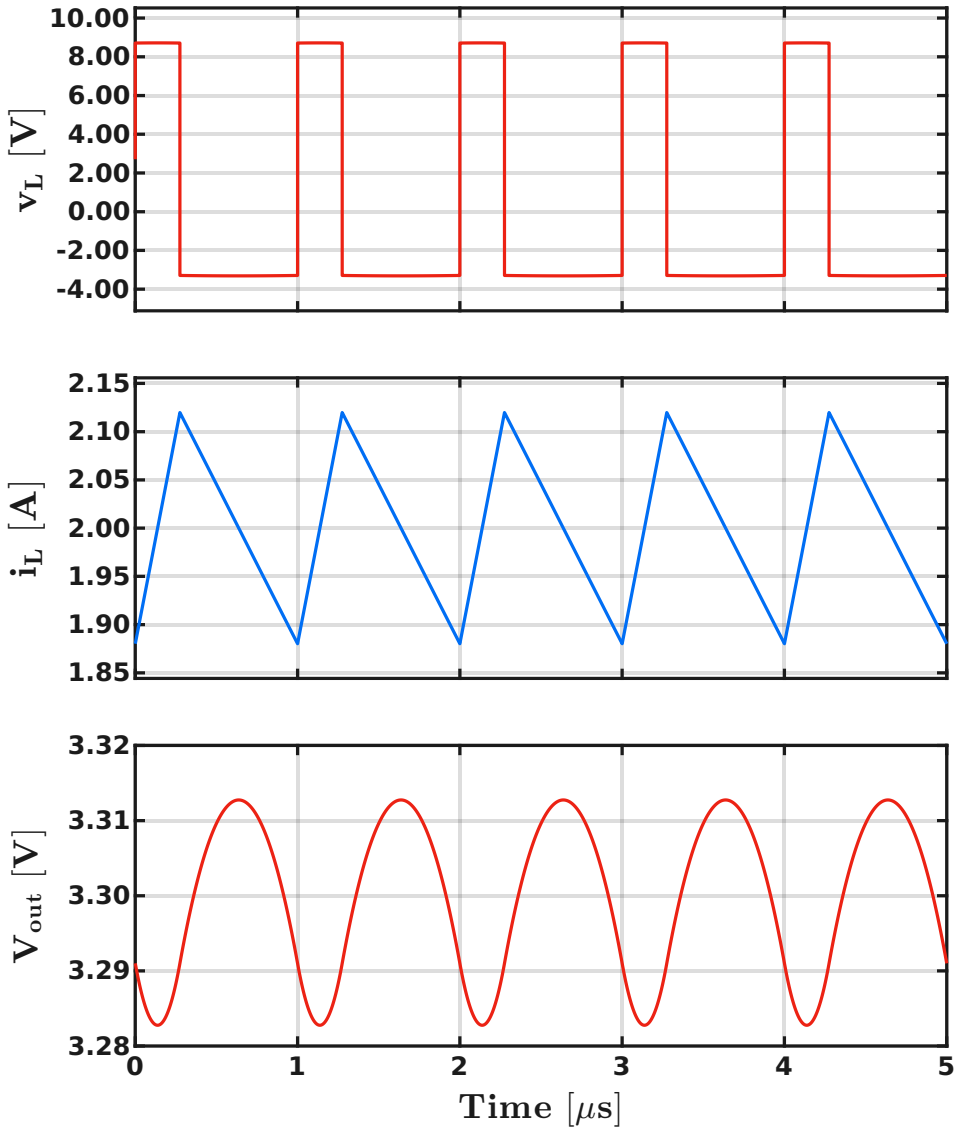


Figure 2.10: Output waveforms of the simulation with L = 10 µH, C = 1 µF.

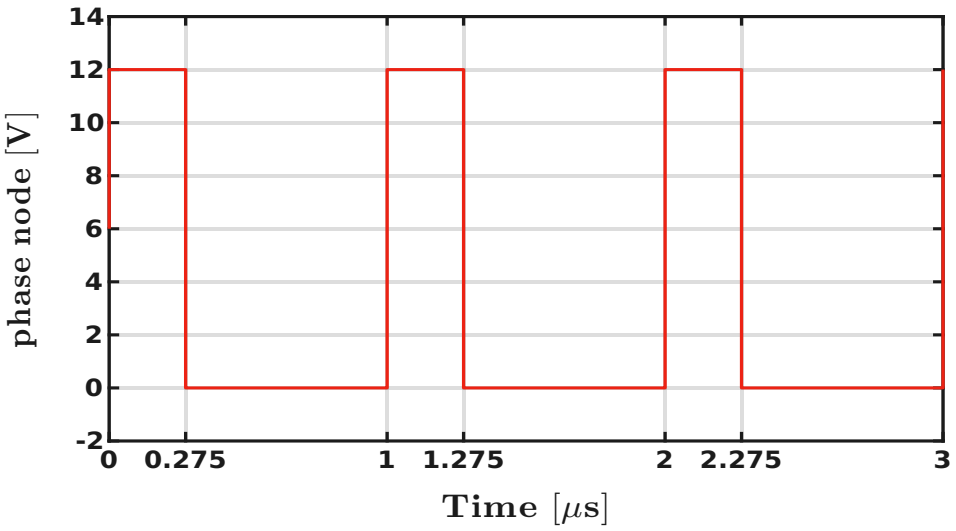


Figure 2.11: Phase node voltage.

the converter. In order to select these values, a target on the ripples must be set.
For the inductor current, normally, a ripple of 30 % or 40 % of the DC load current is accepted; furthermore, due to the high 2 A DC current, the converter stays far away from the zero current value, and it does not need to enter discontinuous conduction mode, even with high ripple amplitude. The load does not require always the maximum amount of current though. At lower load currents, continuous conduction mode is not ensured. In order not to complicate the design, it is recommended to target a CCM operation. The minimum DC load current is of 100 mA; this means that in order not to have any negative current flow, the ripple amplitude must be lower than 100 mA ($i_{pp} < 200$ mA, corresponding to 10 % of the maximum load). This ensures CCM operation in the whole range of currents required by the converter ($I_{load} \in [100\,\text{mA},\ 2\,\text{A}]$).
From Eq. 2.11 the value of inductance to satisfy this requirement is:

$$L = \frac{12 - 3.3}{0.2} \times 0.275 \times 10^{-6} \approx 12\,\mu\text{H}$$

For the 3.3 V DC value of the output voltage, a superimposed voltage ripple of 5 % would be of 165 mV and for this, from Eq. 2.13, given i_{pp} of 200 mA, a capacitance of just 150 nF is needed at 1 MHz switching frequency. By increasing the capacitance to 500 nF a ripple of just 50 mV could be achieved. Now the simulation is repeated with these components:

- Inductance of 12 µH
- Capacitance of 500 nF

The output waveforms of the simulation are plotted in Fig. 2.12 at the minimum 100 mA load and Fig. 2.13 at the maximum 2 A load.
Notice how the change in the load condition does not affect the ripple amplitude. Also the effect on the inductor current waveform i_L is just a Y-axis shift (as expected, by looking at Fig. 2.6a).
Given these results, these values of the reactive components will be, from now on, the default for the design of the converter.

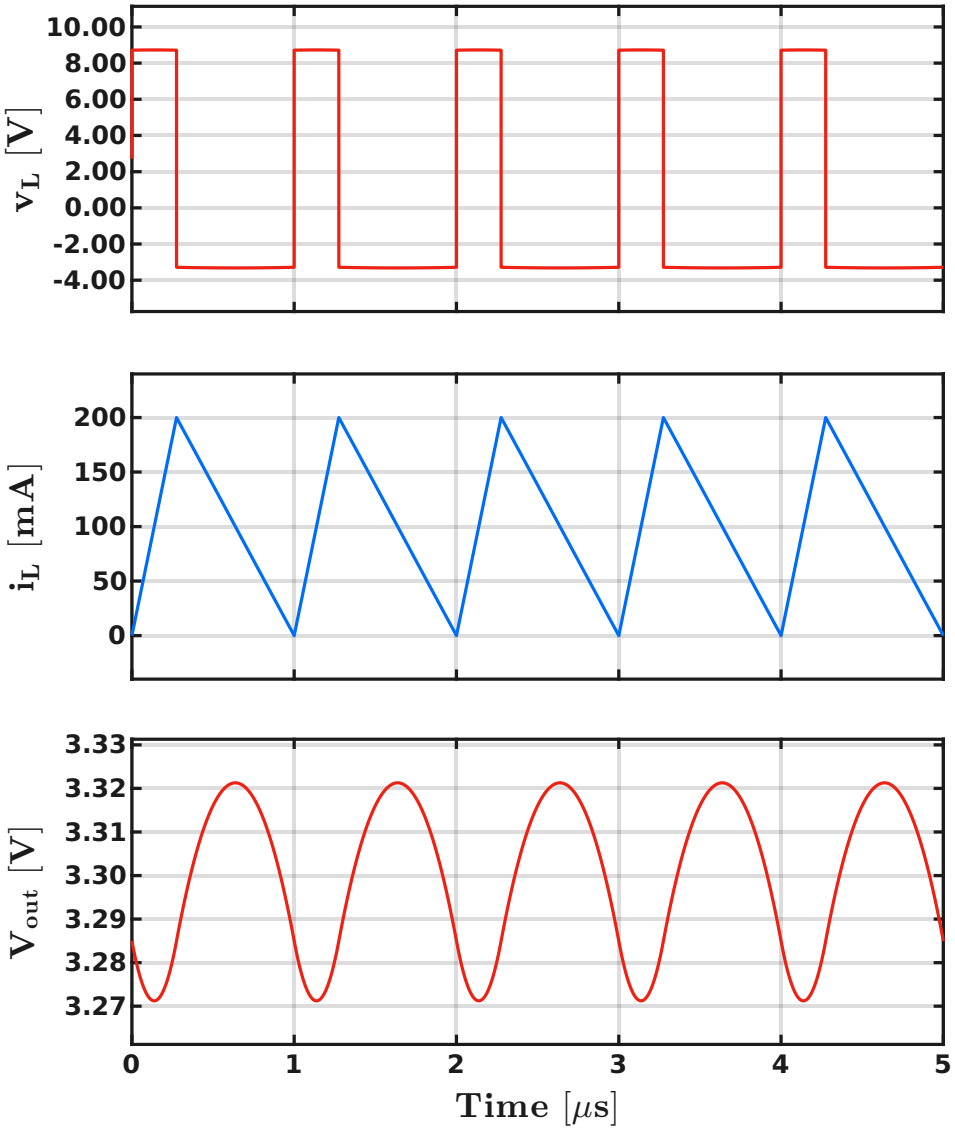


Figure 2.12: output waveforms of the second simulation with L = 12 µH, $C = 500$ nF at 100 mA load current.

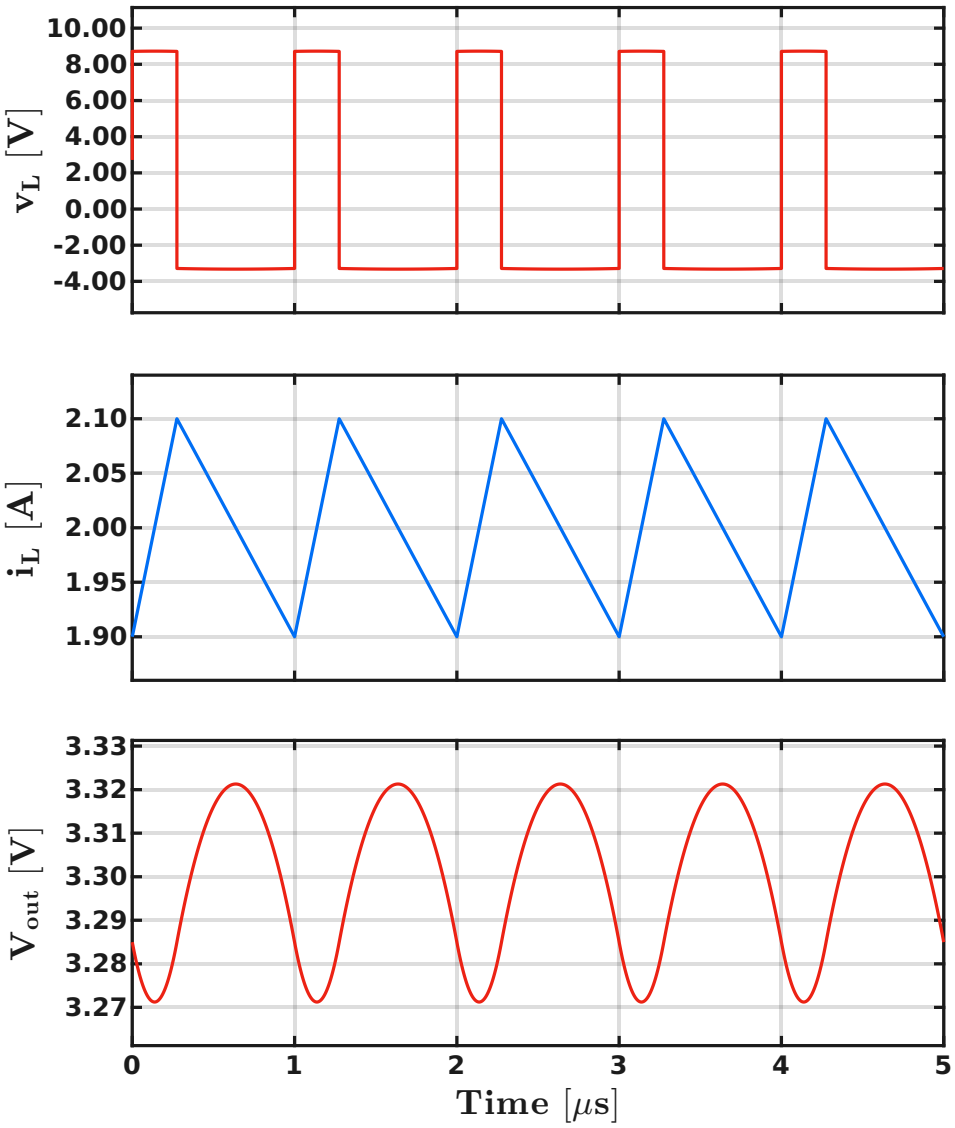


Figure 2.13: Same simulation as in Fig. 2.12 but with 2 A load.

2.2.2 Switches R_{on} analysis

Real switches will have an on-resistance that is very important for the conduction losses in the converter. That said, the resistance effect on efficiency is not the only issue to account for in the design. The switch R_{on} will also affect the ideal shape of the analyzed waveforms.
Let us introduce a $1\,\Omega$ R_{on} to the ideal switches and examine the effect on the converter.

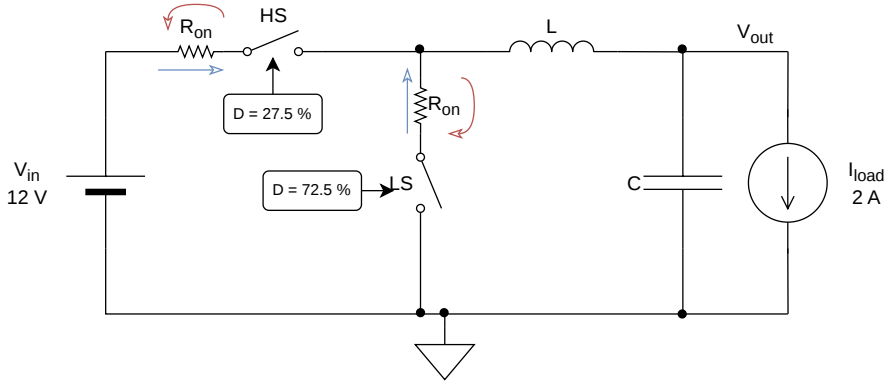


Figure 2.14: Schematic of the converter: the switch now presents its own R_{on}.

When current flows through the half bridge, a voltage difference is now generated between the input and the output of the switches. The phase node will be switching between two potentials that are not V_{in} and ground anymore. These two new potentials are in fact lower than V_{in} ($V_{in} - Iload \times R_{onHS}$) and ground ($-Iload \times R_{onLS}$). This basically, translates to a downward shift in the phase node waveform, which now alternates between less than 12 V and a negative voltage. The output DC voltage becomes different than the one set by the conversion ratio or the duty cycle. Zooming in on the phase node waveform another detail becomes apparent: the flat lines of the previously square wave, now present a slope. These slopes mimic the ripple in the inductor current, and the reason is obvious: the ripple current, enters a resistor and due to Ohm's law, the current ripple is transformed into a voltage ripple with an exact 1:1 match, since the resistance is of $1\,\Omega$. This translates also to the inductor voltage waveform, which now presents a slope itself. The DC value of v_L is not changing from the ideal case though. The reason is that while the positive node (+ node in Fig. 2.3) of the inductor has changed due to the new behavior of the phase node, the negative (-) node has also changed due to the shift in output voltage, hence v_L, which is the difference between the two nodes, remains unaffected. Note that this is to be expected since the Volt second balance rule is always valid and so

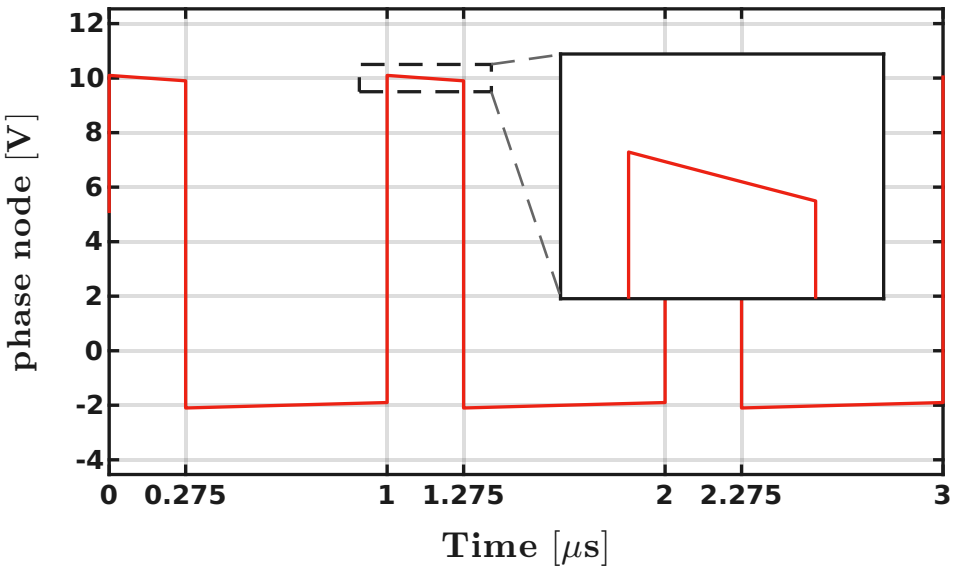


Figure 2.15: Phase node waveform when switch R_{on} is taken into account. The flat square wave now has a slope, both when HS is on and when LS is on. Here only HS slope is highlighted.

$< v_L >$ always remains zero.
In Fig. 2.16 and 2.17 the output DC voltage is reduced to 3.2 V when $Iload = 100\,\text{mA}$ and to 1.3 V when $Iload = 2\,\text{A}$. The switch R_{on} seems to reduce the conversion ratio of the converter depending on the load current. The value of the voltage drop, with regard to the correct conversion ratio, is of 100 mV in the minimum load case and of 2 V in the maximum load case. This is because, since R_{on} is $1\,\Omega$ the voltage drop matches the current flow exactly, differing only in unit (V instead of A).
In order to solve this issue, the duty cycle of the converter must be revised if the chosen switch has a big resistance, or else, some error on the output voltage has to be tolerated.
On the efficiency side, the average power loss equation is:

$$P_d = \frac{1}{T_s}\int_0^{T_s} i \times v\, dt \tag{2.15}$$

in the case of a resistor:

$$P_d = \frac{1}{T_s}\int_0^{T_s} \frac{v^2}{R}\, dt = \frac{1}{T_s}\int_0^{T_s} i^2 \times R\, dt \tag{2.16}$$

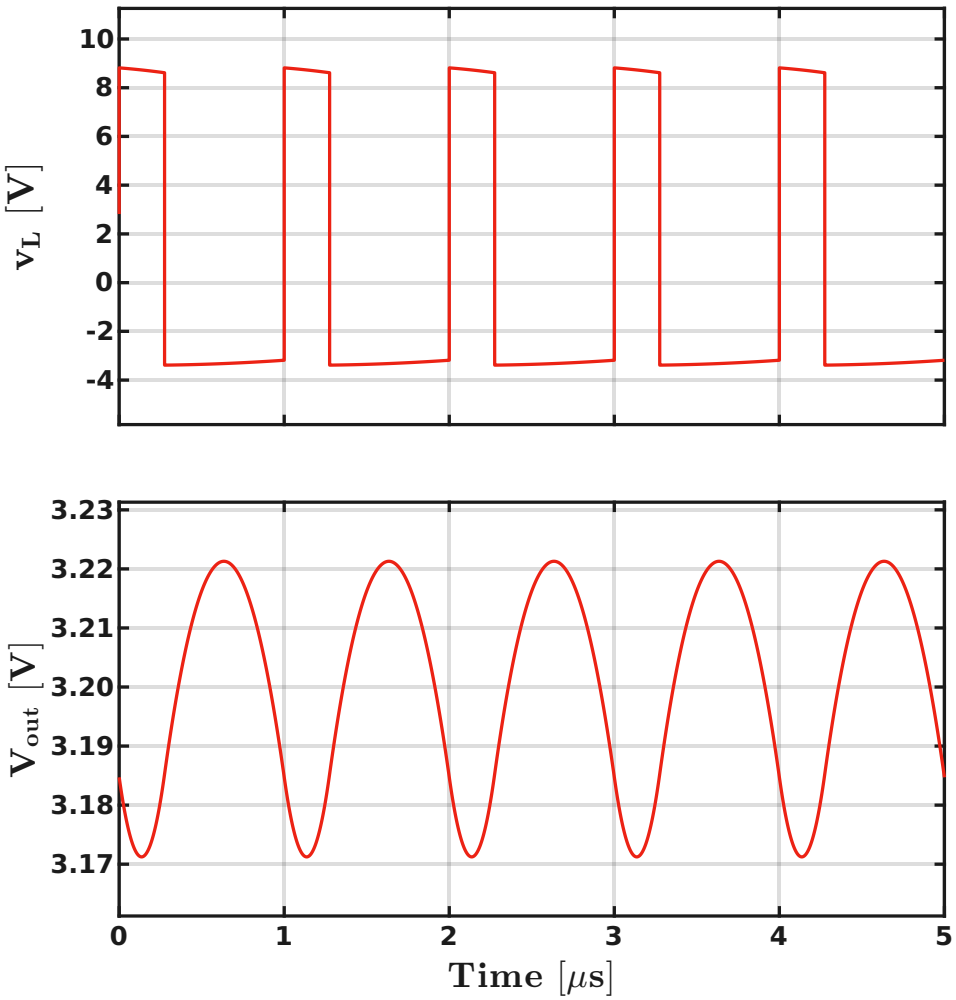


Figure 2.16: v_L and V_{out} waveforms at 100 mA load. The slope is now present also on the inductor voltage. The output voltage DC value is reduced due to the switch R_{on}.

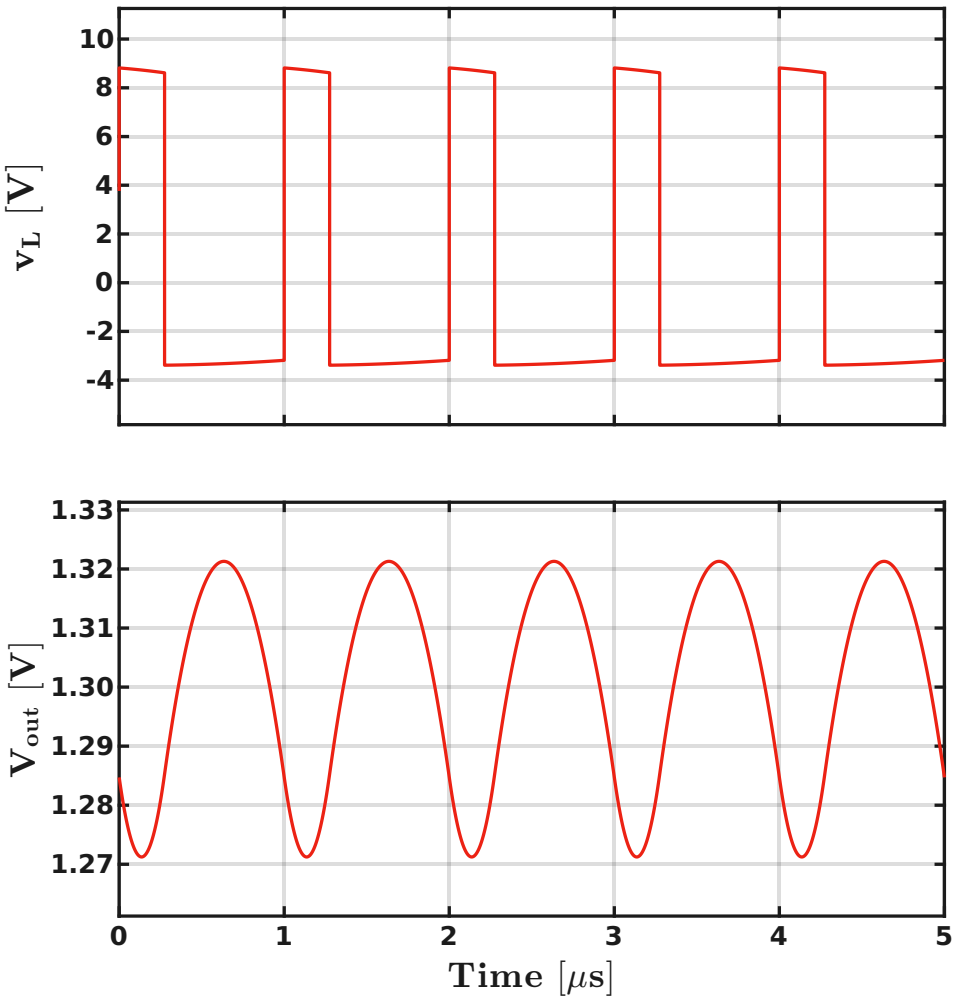
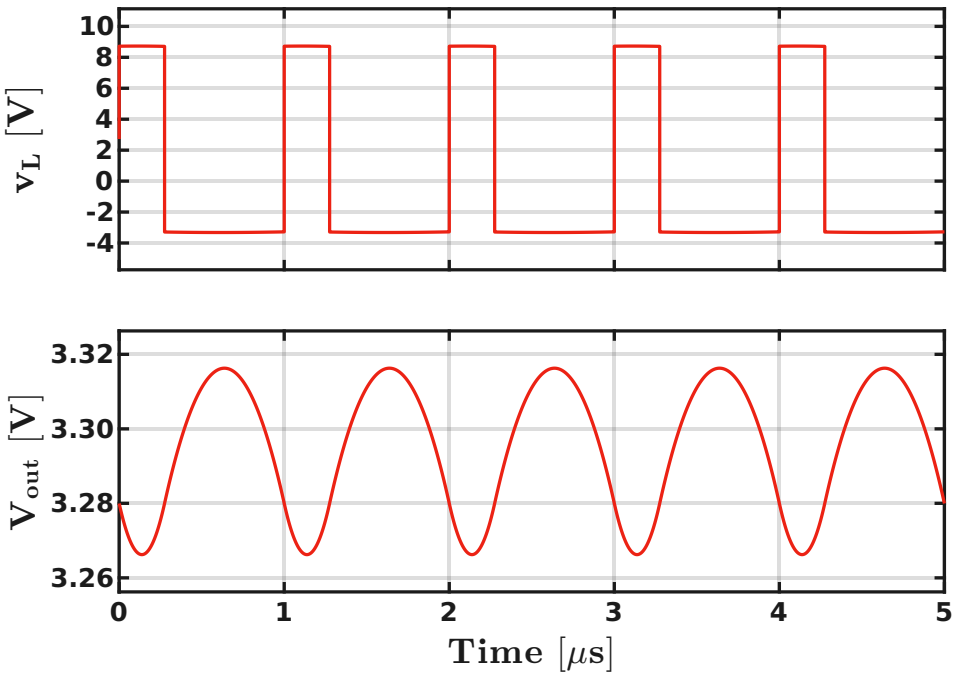


Figure 2.17: Same simulation as Fig. 2.16, but at 2 A load, the output voltage DC value is greatly reduced.

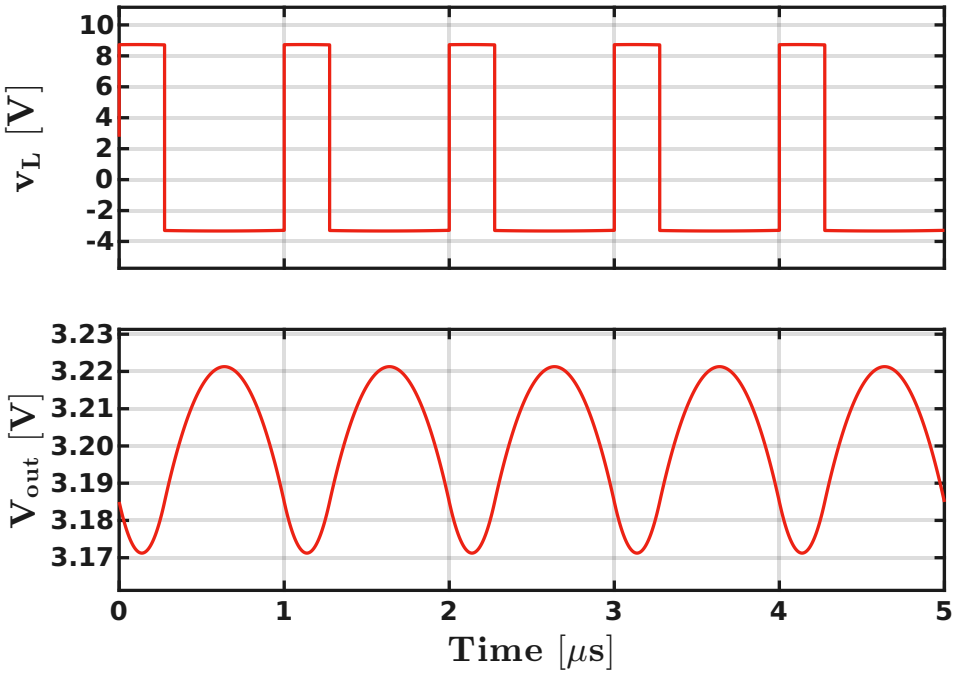
In the case of this converter, the rigorous equation for power dissipation as conduction losses would be:

$$P_d = \frac{1}{T_s}\int_0^{DT_s} i_L^2 \times R_{onHS}\,dt + \frac{1}{T_s}\int_{DT_s}^{T_s} i_L^2 \times R_{onLS}\,dt \tag{2.17}$$

Where R_{onLS} and R_{onHS} are the low side and high side on-resistances of the switches, which are equal here, but can be different by design.
A simpler (less accurate) way to calculate the average power dissipation would be to just multiply the resistance value by the square of the average load current as in Eq. 2.2
A 1 Ω resistance would amount to an average power dissipated of 4 W when the load current is 2 A. Considering that the total output power is just 6.6 W, this is not acceptable. Since the switches conduction loss is just one part of the total power dissipated in the converter, a lower R_{on} is a must.
An on-resistance of 50 mΩ is chosen for now, in order to achieve a conduction loss of less than 200 mW at maximum load.
Note that, when the load diminishes, the conduction loss greatly reduces (half a mW is the loss expected at the minimum current load), as it has a quadratic relation to current. At low load condition, in most converters, conduction losses become negligible with regard to other contributions like switching losses, that will be later discussed.
With 50 mΩ, the simulation are redone and the output waveforms are illustrated in Fig. 2.18. The slope of the waveform is scaled down because of the lower resistance and is now invisible on the graph. The DC output voltage offset is also lower than in the 1 Ω case. At 2 A, the average output voltage is just 100 mV under the target (2 A × 50 mΩ = 100 mV) and at 100 mA the deviation from the 3.3 V target is negligible (5 mV).



(a)



(b)

Figure 2.18: Output waveforms with $R_{on} = 50\,\text{m}\Omega$: (a) at 100 mA; (b) at 2 A load current.

2.2.3 Parasitics on reactive components

Aside from the switches, the inductor and capacitor in the setup also present unwanted sources of power loss; in particular the inductor DC resistance (DCR) can really degrade the efficiency, if not carefully selected. The capacitor equivalent series resistance (ESR) plays a role in the stability of the converter [1] and also affects the efficiency, but does not carry the full load current and so its effect is less pronounced.
Inductors DCR derives from the windings made with copper wires when building the inductor itself. The length of these wires become bigger for higher inductance values, as the number of turns increases and the resistance value becomes higher. The inductor DCR is the primary source of loss, but there are other mechanisms that contribute to power dissipation in an inductor, like core losses, losses due to hysteresis cycle and eddy currents when magnetic materials are used.
A DCR resistance has a similar effect of the switch R_{on}: power dissipation rises and the output voltage becomes lower than the conversion ratio set by the duty cycle. The difference is that, since the inductor is at the output, the phase node waveform will not present a slope. Note that to be precise, when the inductor DCR is taken in account, the average inductor voltage cannot be zero (as predicted by the inductor Volt second balance), but is the average inductor current multiplied by the DCR. This can be interpreted as an ideal inductor where the Volt second balance applies, to which a series resistance with value of DCR is added.
A series resistance on the capacitor will modify the output voltage waveform. The inductor current ripple will flow through the capacitor, generating the familiar waveform of V_{out} shown in previous figures. On top of this, the same current ripple will now flow also in the ESR of the capacitor, generating a voltage ripple which is a replica of the current ripple, scaled by the value of ESR. The effect is that V_{out} waveform now is less sinusoidal (Fig. 2.22).
In addition to the capacitor ESR, a parasitic inductance (ESL) is also present in series to the capacitor and this have an additional effect on the output waveform: when the ripple current flows through the ESL, the voltage across it is a square wave (from Eq. 2.5, the voltage across the inductor is the derivative of the current and because the current is triangular, the voltage will be a square wave). The output voltage, being the sum of the voltage across the capacitor and ESL, will present a form of discontinuity, instead of the sinusoidal shape (Fig. 2.22).

[1] The stability and control loop of the converter will not be discussed.

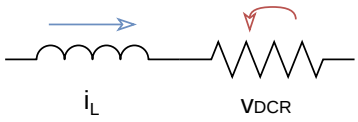


Figure 2.19: Inductor DCR modeled as a series resistance.

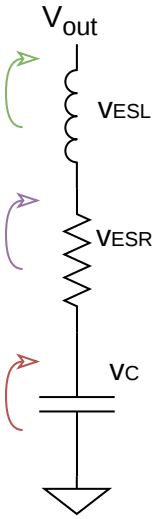


Figure 2.20: Output capacitor with its ESR and ESL. The output voltage is the sum of the voltage across the capacitor, the series resistor and the series inductance.

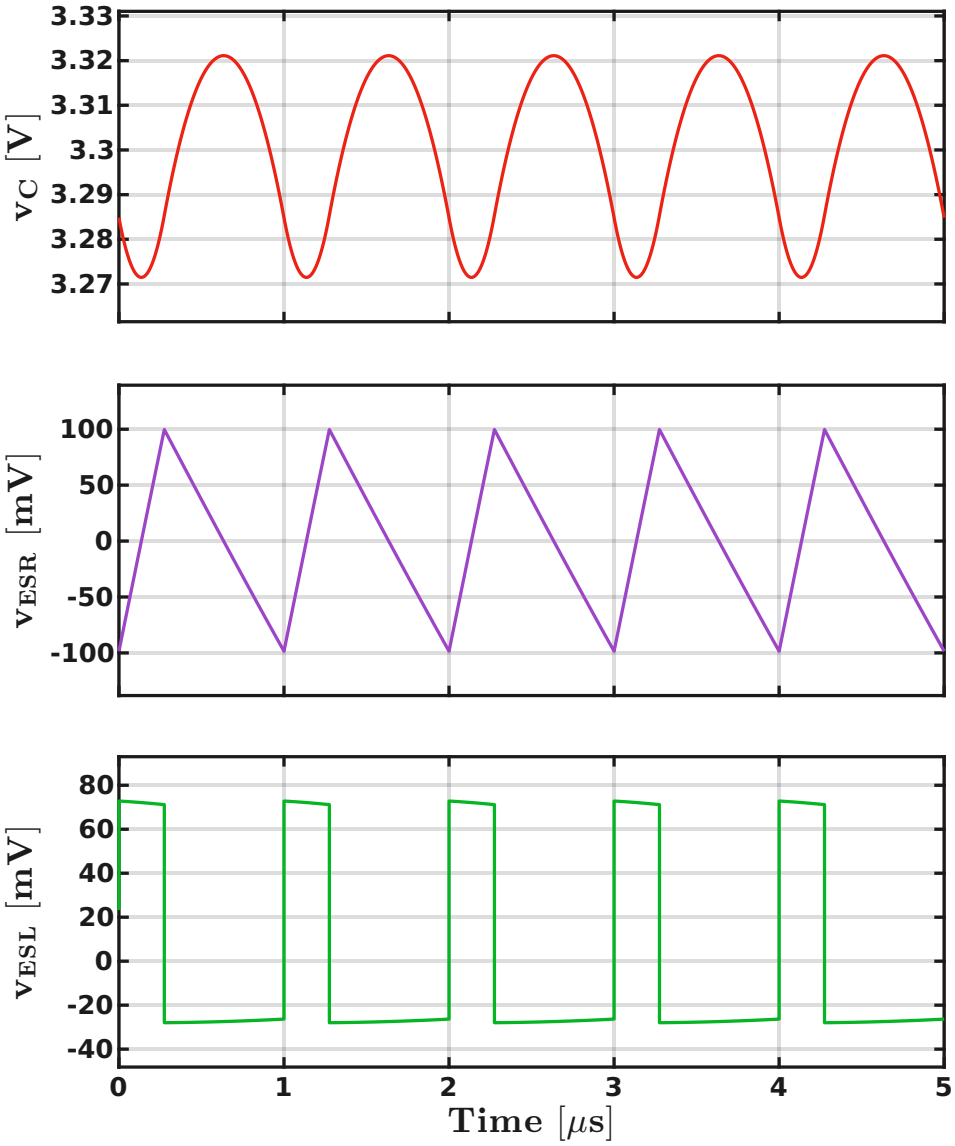


Figure 2.21: Waveforms of capacitor, ESR and ESL voltage. ESR is set to 1 Ω and ESL to 100 nH. Test is done at 100 mA load current.

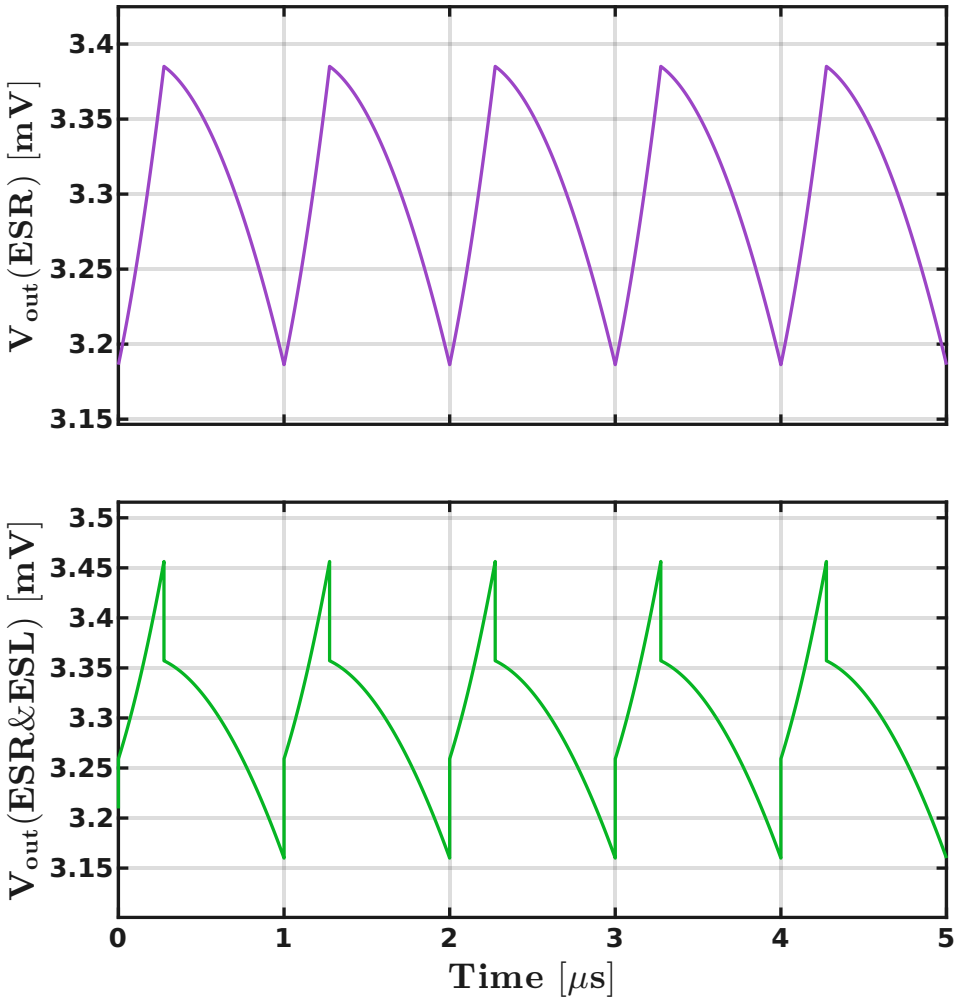


Figure 2.22: Output voltage considering ESR (top) and output voltage considering both ESR and ESL (bottom). ESR is set to 1 Ω and ESL to 100 nH. Test is done at 100 mA load current.

2.2.4 Phase timing

The half bridge switches are driven with ideal waveform generators with a set duty cycle. Let us analyze the behavior of the converter at the instants of switching.
Referring to Fig. 2.23, from time t = 0, the high side waveform generator output, v_{HS}, is high till t = 275 ns. During this time the HS switch is on and will conduct current from the input to the output through the inductor. At time t = 275 ns v_{HS} turns low and the switch turns off and stops conducting. The inductor has to have a continuous flow of current; the current that was flowing through the high side must now flow from another path to feed the inductor. t = 275 ns is also the instant when the low side switch turns on and so, the new path to the inductor is from ground trough LS. LS will continue to conduct current till t = 1 µs, instant at which LS turns off and HS turns on again. This continues on and on given that the analysis is conducted in steady-state condition. t = 275 ns is an instant in which both switches are considered on at the same time and so, a path from the input DC source to ground is established. With real transistors in place of these switches, the time in witch both the high side and low side are on can be considerable, since turn-on and turn-off time of the transistors are not instantaneous. This means that for a small interval of time a very high current will flow from input to ground, dissipating an enormous amount of power. This is accentuated since the path to ground is very conductive by design, given the choice of low resistance switches. To avoid this issue, a proper dead time or disoverlap between the high side and low side phase has to be accounted for. Notice that this also happens at t = 1 µs, meaning that 2 periods of dead time must be placed inside a switching period: one when HS turns off and LS turns on and one when LS turns off and HS turns on.
When a dead time of 1 ns is introduce from t = 274 ns to t = 275 ns (in this 1 ns interval both sides are off) and from t = 999 ns to t = 1 µs big spikes in the phase node voltage can now be seen (Fig. 2.24). The reason is that in these intervals the phase node is not driven by anything and is left to behave on its own. at t = 274 ns the phase node is high and the inductor is calling for current, but right in the next instant, the current path is cut off both from the input and the ground; in order to keep the flow of current through the inductor, the phase node relies on its parasitic capacitance to deliver the current and so the voltage goes lower and lower to negative values. The magnitude of this negative spike depends on the duration of the dead time, on the amplitude of the current drawn by the inductor and on the parasitic capacitance on the phase node.
To avoid those spikes a clamping device, like a diode, is needed to stop the phase node voltage to go towards very low values. Fortunately, a real MOSFET switch has its own parasitic diode that can work when the low side is off. An NMOS, with body connected to source, has a P-type body

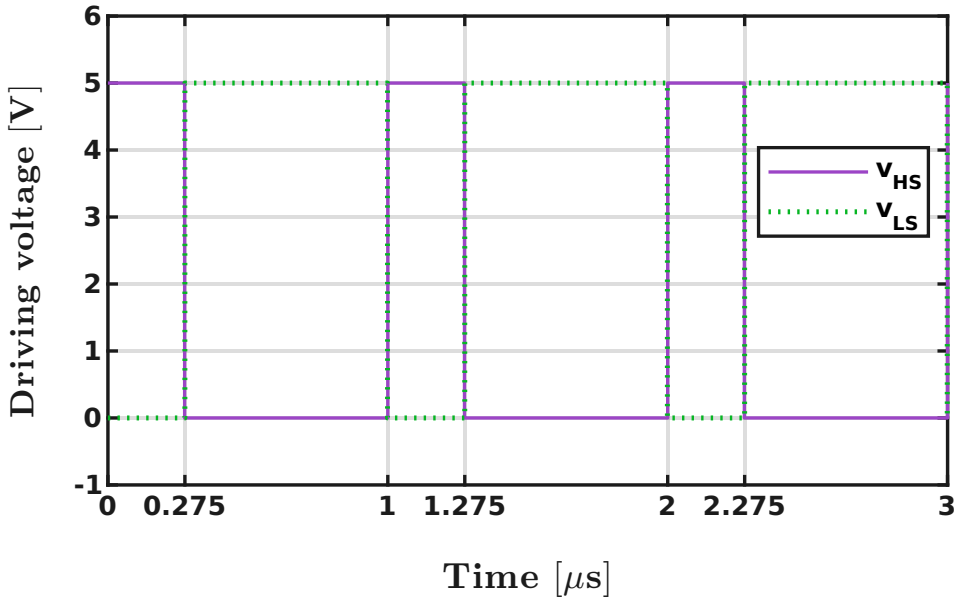


Figure 2.23: High side and low side phase waveforms.

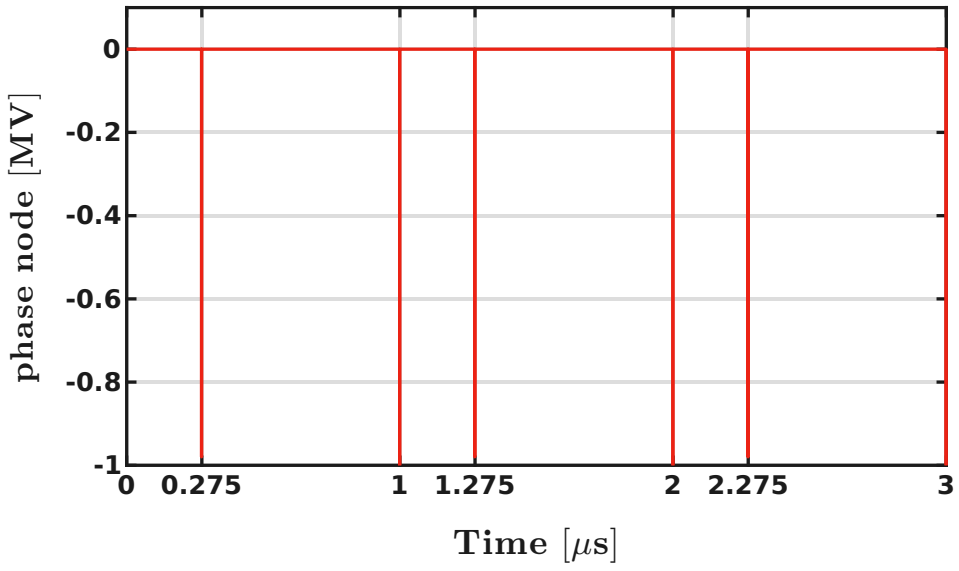
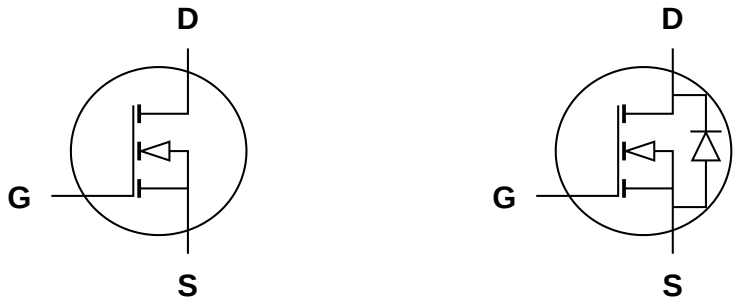


Figure 2.24: Phase node when a dead time of 1 ns is introduced. Given the lack of a clamping mechanism, the node goes down during the dead time in the simulation.

and an N-type drain, effectively creating a parasitic PN junction that works in parallel as the clamping device during the dead time in the switching period (2.25b).
The choice of the duration of the dead time, when a real transistor is used, is dictated by an important trade-off: a long duration ensures that there will be no crowbar current, but the diode will be on for a long time. The diode with its forward voltage can lead to much higher conduction losses with respect to the R_{on} of the transistor (as per Eq. 2.3). The idea is that the dead time should be long enough to avoid crowbar but not too long because there is no benefit in it.



(a) (b)

Figure 2.25: (a) NMOS symbol. (b) The body diode of the NMOS is highlighted.

The phase node behavior when a diode is introduced in parallel to the low side is depicted in Fig. 2.26 where it can be seen that, during the dead time, the node is set to the diode forward voltage just before the low side turns on and right after it turns off.

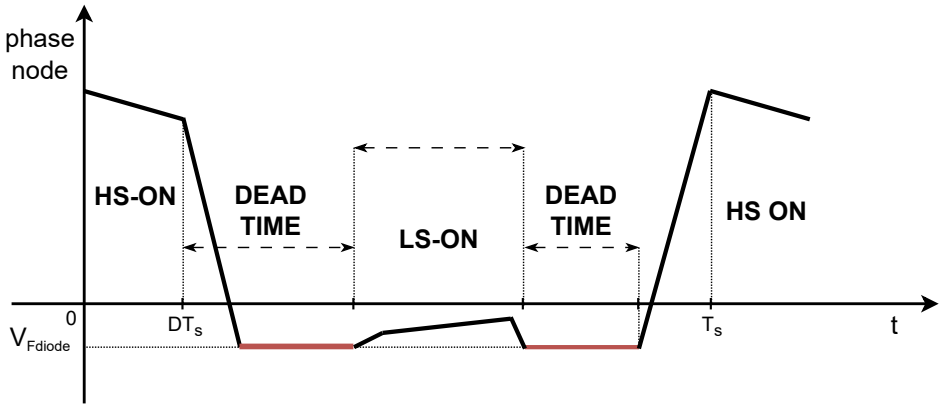


Figure 2.26: Phase node behavior: during the dead time, the diode controls the node.

2.2.5 Component selection

For the final simulation in SIMPLIS, a real inductor and real switches are introduced.

- Inductor selection

the inductor must satisfy the following requirements:

- 12 µH inductance
- Resonance frequency > 1 MHz
- Saturation current limit > maximum current load (2 A)
- Low DCR

Inductor TDK B8244T1123K000 satisfies all these requirements. It is a wire wound inductor from TDK with ferrite core, 12 μH, rated for 2.7 A, 19 MHz resonant frequency and a 141 mΩ DC resistance in a footprint of 5.6 mm × 5 mm × 5 mm.

- Switch selection

For the switch, transistor BSC110N06NS3 from Infineon high power MOSFETs is selected. It is a 60 V NMOS supporting high continuous drain current (> 50 A) and with a very low R_{on} of 9 mΩ. Although these parameters seem very adequate, it should be noted that they are valid when the transistor is driven with 10 V V_{GS}. In this setup, the switches are driven

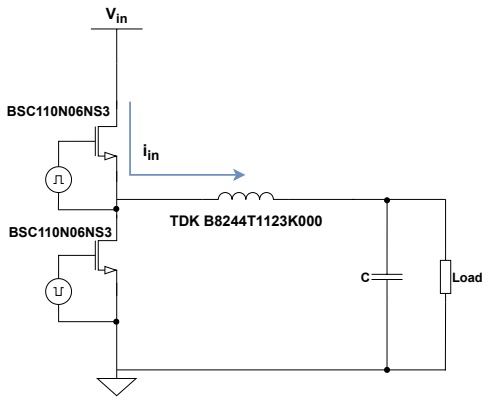


Figure 2.27: Setup of the converter with the selected components.

ideally, with pulsed waveforms, but to keep the setup fitting for future revisions in which a MOSFET gate driving circuit could be implemented, these pulses are set to 5 V as this future circuit would be expected to deliver.
At $V_{GS} = 5$ V, the resistance increases approximately threefold (Fig. 2.28, $R_{on} \approx 30\,\text{m}\Omega$), which still remains below the original $50\,\text{m}\Omega$ target.
The simulation results with these components are plotted in Fig.2.29a and Fig.2.29b. Note that there is no way to simulate the inductor model as its core losses are very complicated to model; consequently, an ideal inductor of $12\,\mu\text{H}$ with a series resistance of $141\,\text{m}\Omega$ is introduced in the setup to take the role of TDK B8244T1123K000.
At the maximum load, the DCR and the R_{on} cause the output node to deviate from the 3.3 V target; a higher duty cycle will be required to counter this effect.
For the transistor BSC110N06NS3, SIMPLIS default simulator uses a very simplified model for the simulation and the results are not very accurate, especially since turn-on and turn-off time of the transistor are not exact and as a result, switching losses are unaccounted for.
In order to better understand the behavior of the converter at the instants where the transistor actually switch, SIMPLIS offer a slightly more accurate level of modeling of the transistor (level 1 instead of level 0).
When simulating with this more accurate model, the waveforms appear to be very similar, but one significant difference can be observed regarding the input current (or the high side current) to the converter.
In Fig. 2.30 the input current to the converter is plotted: the waveform has a semi-triangular shape. This current forms the rising part of the inductor current (when HS is on), the other part comes from ground through the low side and, combined together, they form the entire triangular waveform i_L.
In Fig. 2.31 the same input current is plotted, but with the higher accuracy model.

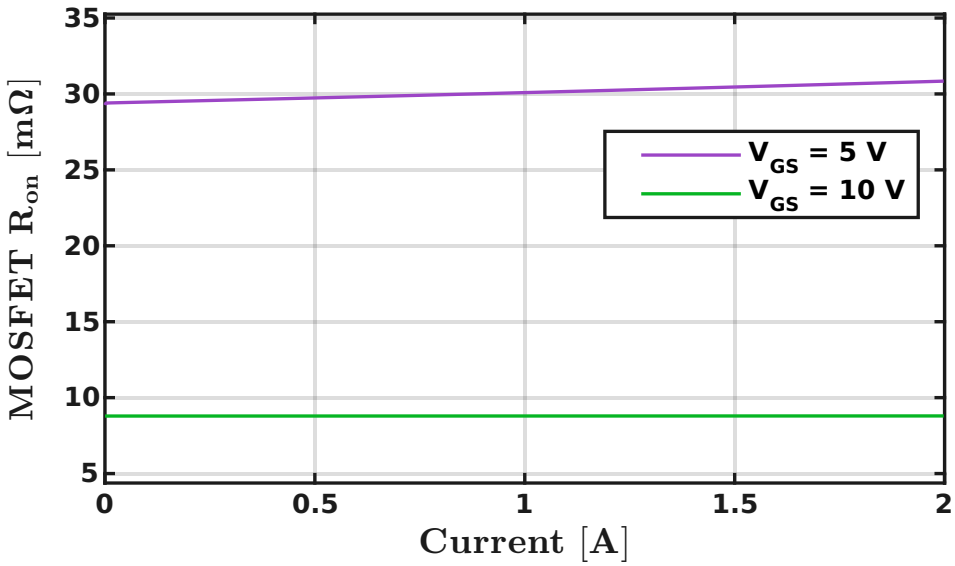
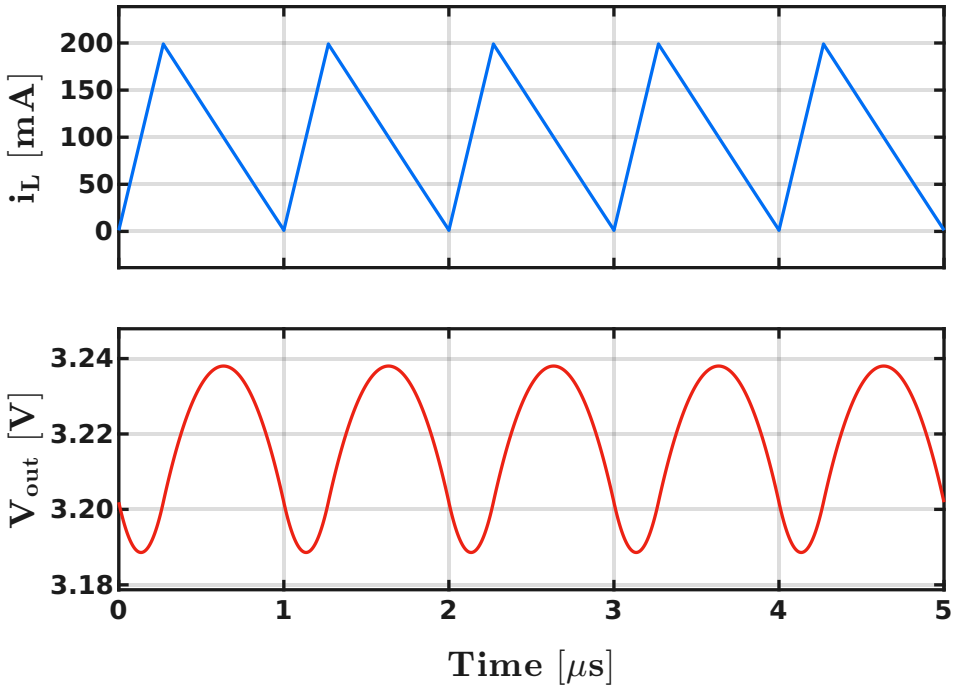
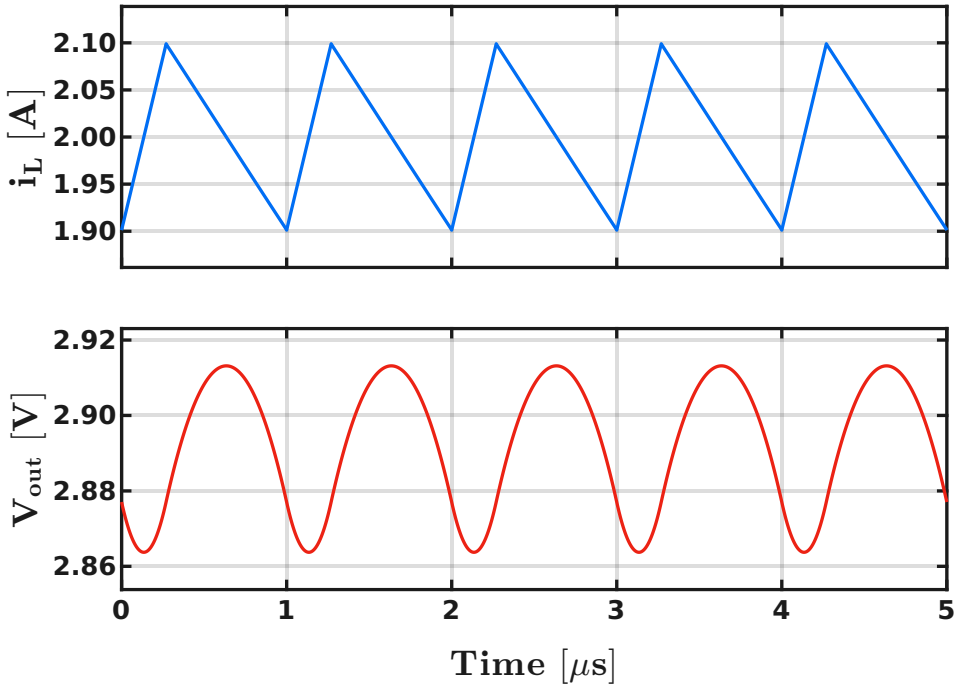


Figure 2.28: Transistor BSC110N06NS3 R_{on} value vs. drain current for 5 V and 10 V V_{GS}.

There are overshoots at the two switching instants (i.e. $t = 1\mu s$ and $t = 1.275\mu s$). The high overshoot in current at $t = 1.275\mu s$ happens when the high side turns off and the low side starts to turn on. The dead time of 1 ns is too small and for a small period of time the input source sees a path to ground through both switches that are now conducting. Consequently, the converter experiences a large shoot-trough current during this transition and that is the cause of the overshoot. This may be eliminated with a higher dead time.
For the overshoot at $t = 1\mu s$, even with a large dead time the peak remains. This happens because when the HS switch turns on, in order to bring the phase node to 12 V, it has to charge the parasitic capacitance of the node. Given the use of two external MOSFETs as the HS and LS switches, the capacitances are: the node parasitic capacitance, the transistors capacitance and possibly the inductor parasitic capacitance as well. This occurs at every switching period and leads to higher switching losses. The switching losses are not part of the analysis in SIMPLIS since the turn-on and turn-off time of the transistors are not well modeled and will be briefly discussed when analyzing the converter in Cadence Virtuoso.



(a)



(b)

Figure 2.29: inductor current and output voltage of the converter simulated with selected components:(a) at 100 mA load and (b) at 2 A load.

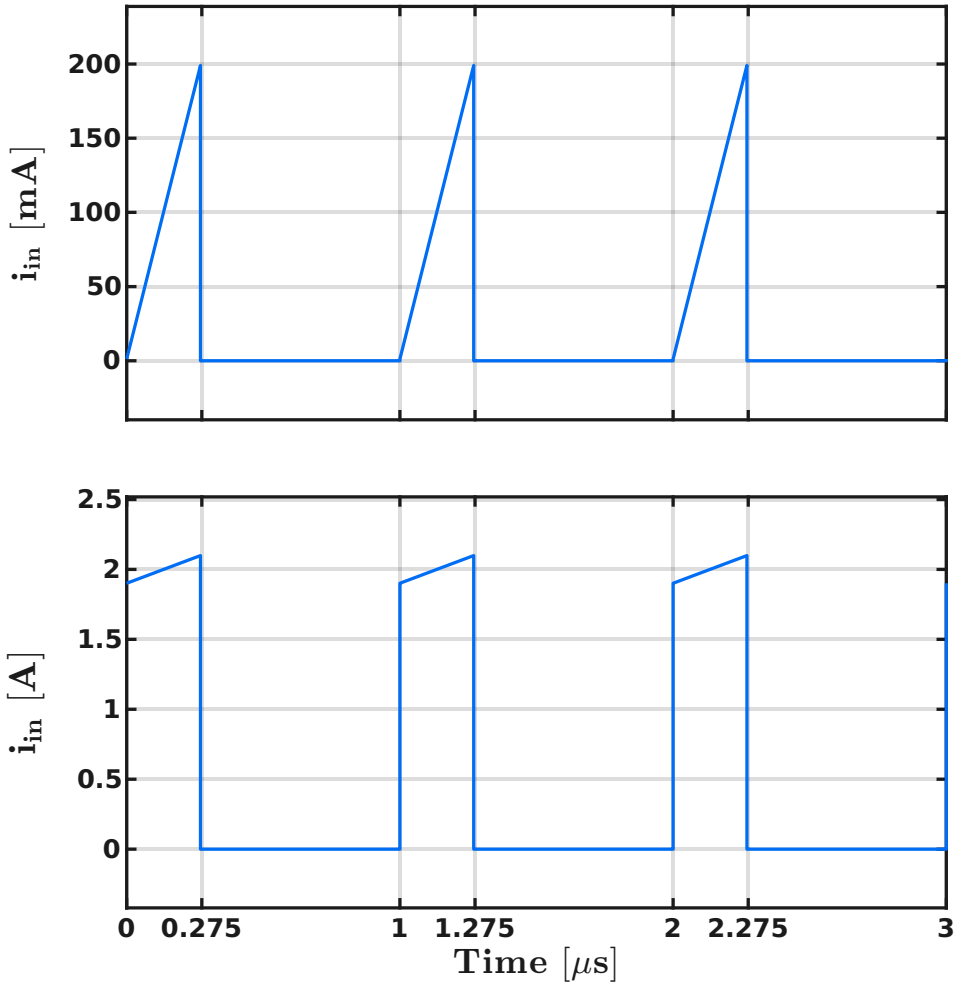


Figure 2.30: Converter input current at minimum (top) and maximum load (bottom).

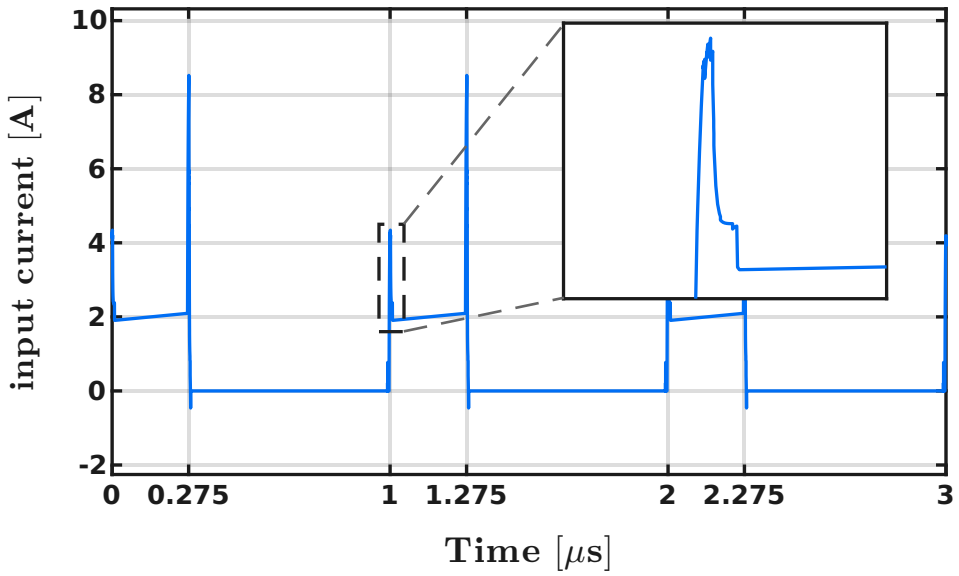


Figure 2.31: Input current to the converter: overshoots can be seen at switching instants.

2.2.6 Efficiency of the converter

The SIMPLIS software allows probes to be placed on the schematic in order to extract the power delivery and power loss of the circuit and calculating the total efficiency.
Examining Fig. 2.32, the efficiency at maximum load is higher than 85 % but greatly decreases at lower load conditions.
The normal efficiency behavior of a buck converter is similar to the one shown in Fig. 2.32, where at low load condition, the efficiency is low due to switching losses dominance and when the load current increases, the conduction losses start to dominate instead, leaving a peak efficiency in the middle. In this case the switching losses are not accurately accounted for in the plot; the low efficiency at minimum load is due to the dynamic power dissipated to charge and discharge the gate of the transistors. This power is proportional to the gate capacitance, switching frequency and the square of the voltage value applied to the gate and that is why the difference in efficiency between the 5 V and 10 V driving is very noticeable at minimum load conditions.

$$P_{dg} = C \times V^2 \times f_s \tag{2.18}$$

MOSFET BSC110N06NS3 has 2 nF gate capacitance and dissipates 50 mW of power at 5 V V_{GS} and 200 mW at 10 V. Considering that at 100 mA of current, the converter output power is just 330 mW, this explains why

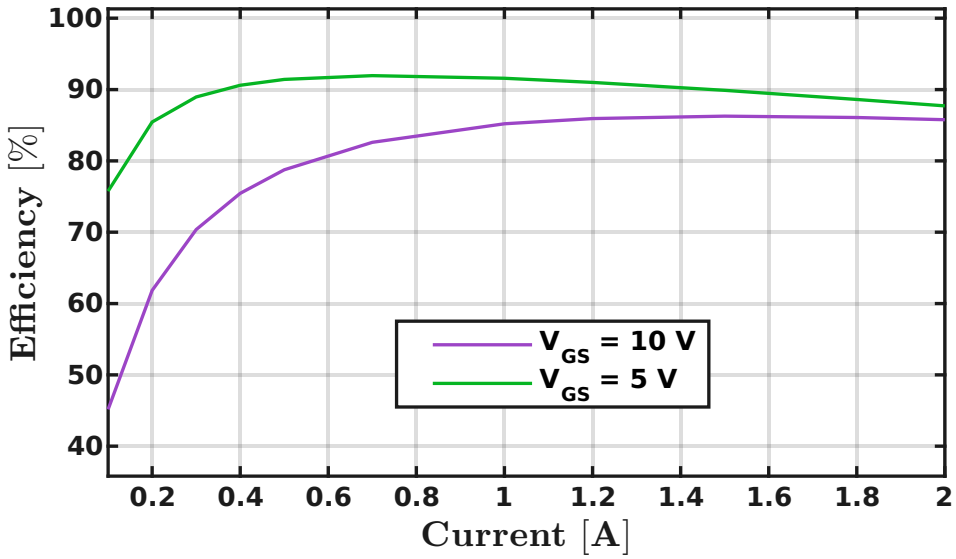


Figure 2.32: Efficiency of the converter vs. Load current evaluated when driving the MOSFETs at 5 V and 10 V V_{GS}.

the efficiency is so low. At higher load condition, the gate dissipation is less pronounced since the total output power amounts to 6.6 W.
Given these results, MOSFET BSC110N06NS3 does not appear suitable for the converter at lower output currents due to its high input capacitance.
Since the maximum current requirement for the converter is 2 A, a solution with integrated transistors is a possible approach and should lead to a more compact implementation and better performance at lower currents as well as lower parasitic capacitance and switching losses.
In the next step of the design, a solution with integrated transistors instead of external ones is explored.

2.3 Design in Cadence Virtuoso

In the Virtuoso software, the simulation models for MOSFET BSC110N06NS3 and inductor TDK B8244T1123K000 are imported and used to simulate the converter; however, as expected, the results in terms of efficiency are worse than previous simulations in SIMPLIS since now the involved switching losses are taken in account in addition to the other losses in the circuit.
Moving from discrete switches, integrated transistors will now be used.
The technology adopted is the BCD 180 nm from TSMC and the transistors are the 29 V NA29_G5A_MAC high voltage NMOS.
For the setup, apart from the integrated high and low side, the rest of the components are the same as before.

2.3.1 Switch R_{on}

Unlike the resistance of an external switch, with an integrated transistor there is the freedom of selecting the value of R_{on}; the only limit is set by the area consumption on the silicon die. If area constraint is not an issue, a very low R_{on} could be achieved, but even with no limits in terms of size, designing an excessively large device will introduce significant parasitic capacitance that are especially problematic when designing a switching converter, since this capacitance will load the nodes that have to be switched high and low at every period. In Fig. 2.33 the value of R_{on} depending on the transistor dimensions is displayed.

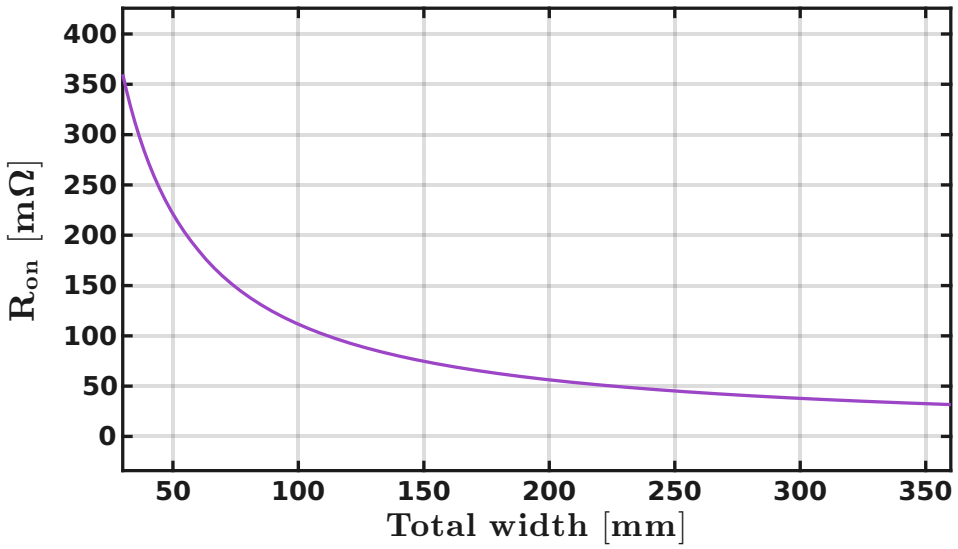


Figure 2.33: NA29_G5A_MAC On-resistance vs. Width of the device.

The transistor length (L) is set to the minimum $L = 1.3\,\mu m$ since the resistance is proportional to the length and inversely proportional to the width (W).

$$R_{on} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} V_{ov}} \sim \frac{L}{W} \tag{2.19}$$

The transistor is subdivided in 300 fingers with a minimum width of 100 μm each, so that the total width is at least 30 mm. For a good layout implementation the transistor will not be that wide in reality, but it would be implemented in order to occupy the least area while still having a large effective width without enlarging in a straight line. In order to achieve $R_{on} < 50\,m\Omega$ the total transistor width must be higher than 225 mm meaning that each finger should be at least 750 μm wide.
A total width of 300 mm is selected both for the high side and the low side switches and the output waveforms of the simulation are the characteristic

triangular wave for the inductor current and the sinusoidal wave for the output voltage with a small superposed ripple on top.

2.3.2 Timing and phase node behavior

Let us focus now on the behavior of the phase node (Fig. 2.34) when a dead time of 10 ns is set: at the switching instants, a brief negative peak at around -700 mV can be observed and that indicates that the body diode of the low side is working by clamping the node during the dead time. What is apparent is that this behavior is not the same at high load and low load conditions.
Before switching from low to high, the dead time leaves the phase node relying on the diode; the node rapidly settles from ground to around -700 mV, then the high side turns on and pulls the node towards 12 V. This behavior can be observed both for the low load and for the high load condition (i.e. at t = 1 μs).
When switching from high to low instead, the behavior is very different. A negative peak can be observed in fig. 2.34 for the high load but not for the low load condition. The current drawn by the inductor during the dead time is high during the first case; the parasitic capacitance on the phase node discharges very fast in order to provide this current and so the node voltage immediately decreases and reaches the value of the forward body diode voltage: the diode turns on and clamps the voltage. In the latter case, when the load current is low, the inductor draws less current while the parasitic capacitance is the same, hence it discharges slower than before and cannot reach the forward voltage of the diode before the dead time is over; the low side now turns on when the phase node is still high and it pulls the node towards ground with a different (faster) slope.
Notice that in the lower load condition, the LS switch turns on while its drain to source voltage (V_{DS}) is high, hence it will dissipate some power on top of the power that is normally dissipated, after its turn-on time, when the transistor is fully conducting. This power loss is part of the switching losses of the converter. Overall the dead time introduces two benefits:

- Avoiding shoot-through current
- Avoiding switching losses for the low side

The trade-off is always that the diode conduction may introduce unwanted power loss if the dead time is too high.
In the HS case, the MOSFET will always turn on when the phase node is low and so its V_{DS} will always be high, contributing to additional switching loss, unless some kind of soft switching technique is implemented [12].
The input current is depicted in Fig. 2.35: at every HS turn-on, spikes in the current waveform are observed. These are capacitive spikes that occur

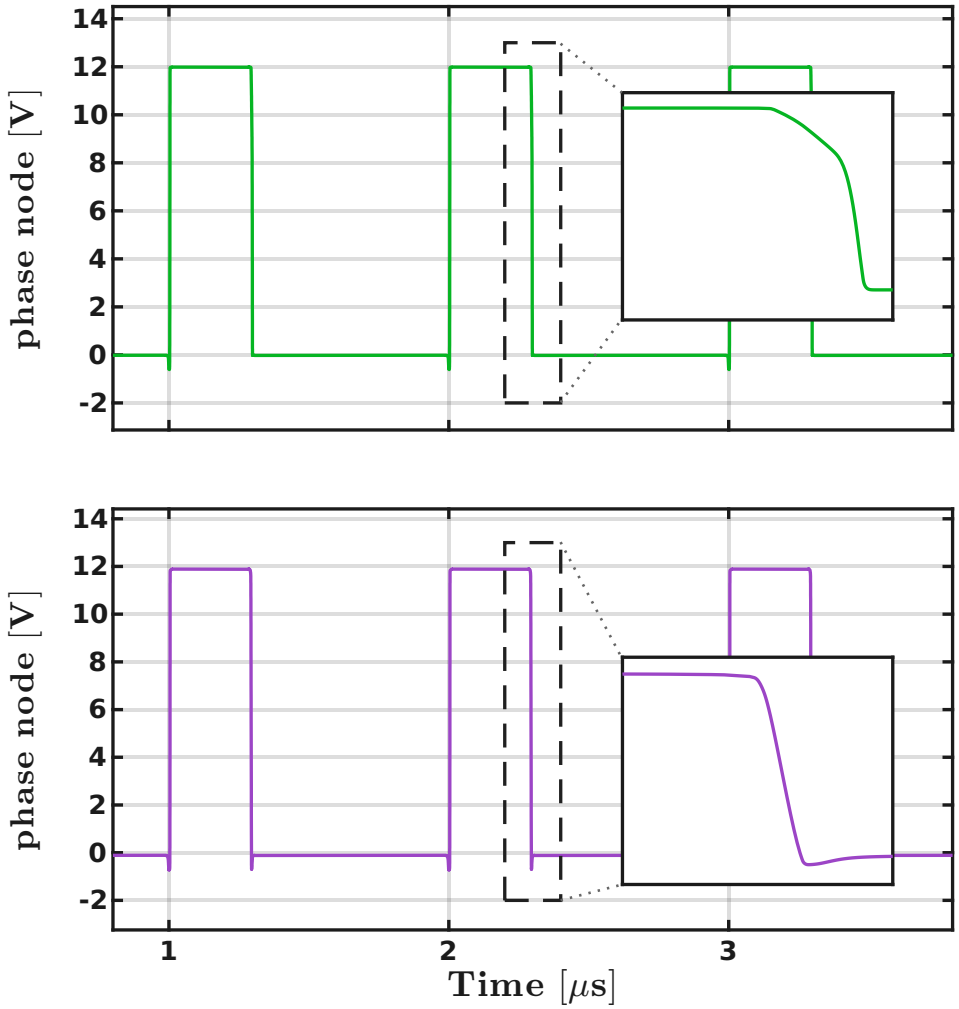


Figure 2.34: Phase node behavior at low load condition (top) and high load condition (bottom).

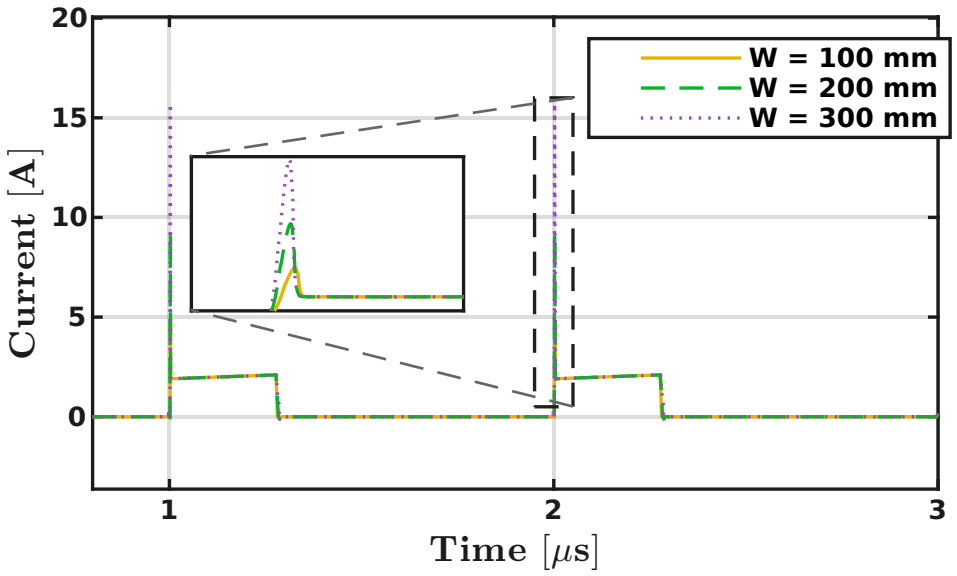


Figure 2.35: Converter Input Current: capacitive spike are observed at HS turn-on.

because in order to drive the phase node, the high side switch output capacitance need to be discharged and the low side output capacitance needs to be charged. By changing the dimension of the transistor, the output capacitance also changes and the amount of current overshoot become different. Looking at Fig. 2.35 at 100 mm of transistor width the spikes are much lower than at 300 mm. There is a clear trade-off: the wider the transistor, the higher the switching losses; conversely, the narrower the transistor, the higher the conduction losses.
The dimensions of the switch must be set with this trade-off in mind and the optimal solution is to balance both contributions.

2.3.3 Converter efficiency

The total power dissipation of the converter is analyzed at different dimensions of the transistors at the full load. In Tab. 2.1 the values of the transistor R_{on} are matched to the width of the device.
The High side and low side transistors are simulated at different combinations of widths. Up until now, the dimensions of the transistor were set equal for HS and LS, but this is not a rule; in fact, based on the application, it might be better to make the transistors mismatched. For example: when the duty cycle is very high, the HS switch conducts for the majority of the period and so it is a better design choice to minimize its R_{on} in order to counter the higher conduction loss that would derive from it; vice versa if the duty cycle is very low. In Fig. 2.36, the total power dissipation is plotted

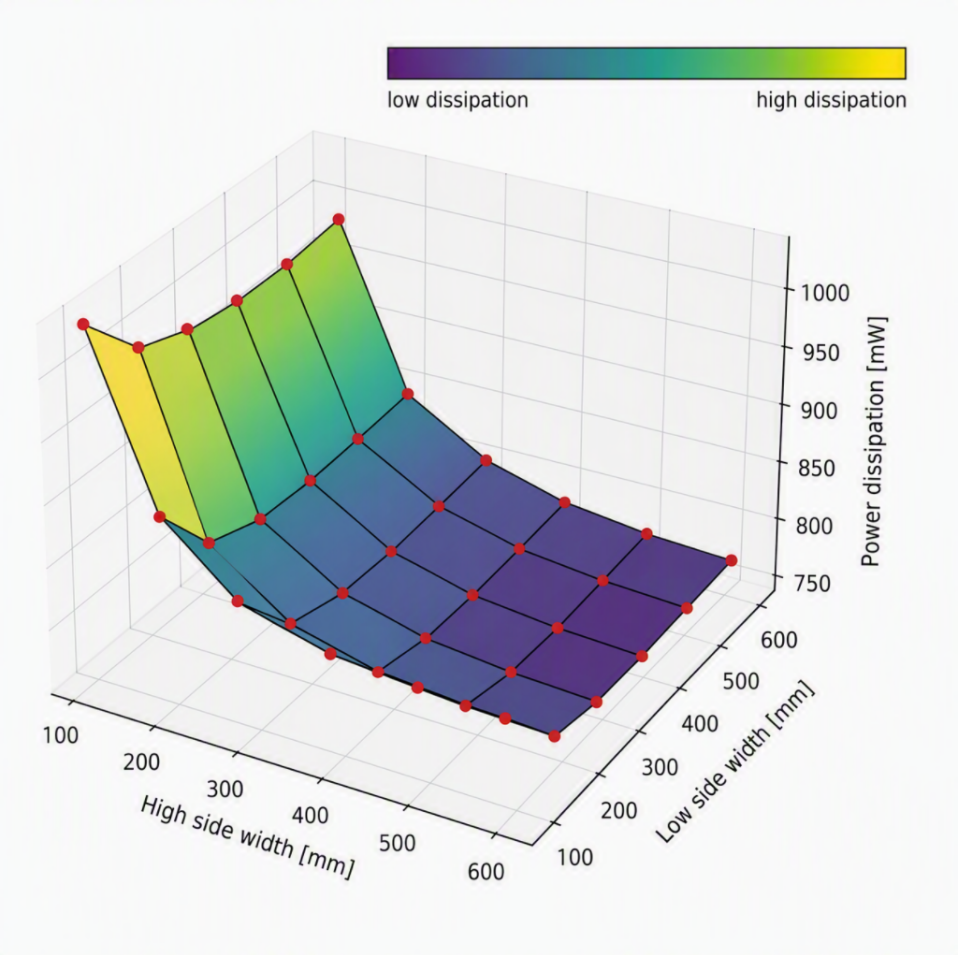


Figure 2.36: Total power dissipation vs. Width of the transistors.

in a 3-axis graph to show the loss based on the HS and LS dimensions. The power loss enters a plateau when the HS total width is around 300 mm; having larger transistors does not seem to benefit the efficiency much, while

W	**R**$_{on}$
100 mm	112 mΩ
200 mm	56 mΩ
300 mm	38 mΩ
400 mm	29 mΩ
500 mm	23 mΩ
600 mm	20 mΩ

Table 2.1: Transistor R_{on} at the analyzed widths.

greatly increasing the silicon area consumption.
Given this reason, a total width of 300 mm for both the HS and LS is chosen. The minimum of power dissipation is around 750 mW which would amount to an efficiency of:

$$\frac{P_{out}}{P_{out} + P_{diss}} = \frac{6.6}{6.6 + 0.750} \approx 89\,\%$$

The power lost on the inductor DCR alone is 520 mW, hence even with ideal transistor the ceiling of efficiency would be around 92 %. This suggest that the inductor is actually the bottleneck in the setup that bars the converter to achieve an optimal efficiency (> 90 %).
The HS and LS combined dissipate less than half of the inductor alone. An inductor with comparable or lower losses than the switches has to be incorporated in the design.
Coilcraft inductor XAL1080-123MED is a good choice: it is a 12 μH high current inductor with 12 $m\Omega$ DCR and 10.6 MHz resonance frequency.
Simulating now with this inductor in the setup, the power dissipation is much lower.
While the core losses of the inductor are not taken in account in the simulation, the producer site displays a tool to calculate the additional losses: The total power loss of the inductor is 66 mW (48 mW from the DCR and 18 mW for the core losses).
The final design is now complete and the efficiency of the buck converter that will supply the analog section is depicted in Fig. 2.37.

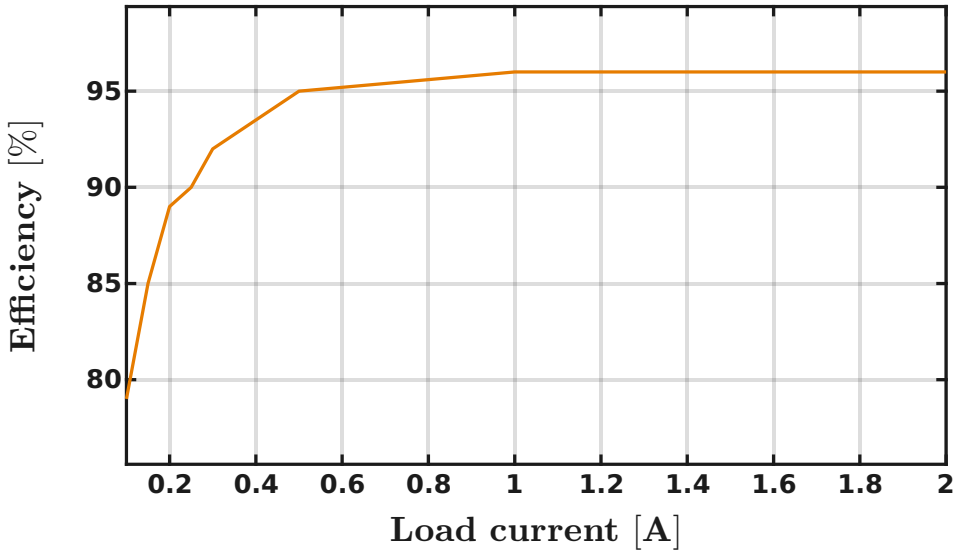


Figure 2.37: Efficiency of the converter vs. Load current

Chapter 3

Supply for the power core: architectural analysis and implementation

This chapter is dedicated to the design of the architecture that will supply the matrix LEDs with the required power.
Unlike the analog domain of the system, the VDD_p rail must supply a very high load current (up to 25 A) and deliver high power to the LED matrix. In this case, conduction losses and heat dissipation become critical.
By implementing the converter with the integrated transistors used in chapter 2, the losses would be too high and a bulky thermal management solution (like a heat sink) would be required.
Using discrete transistors with lower R_{on} would lower the conduction losses: for example, a 10 $m\Omega$ resistance with a 25 A load current would dissipate around 6 W.
Instead of trying to lower the on resistance of the switch, a possible solution is to change the topology of the converter in order to reduce the current flow through the resistance itself.
By using multiple half bridge configurations in parallel, each half bridge would carry only a fraction of the entire current, while the load would still receive the full current. The multiphase topology (Fig. 3.1) is widely used in high current applications and offers less conduction losses and other advantages over the standard buck converter [13].

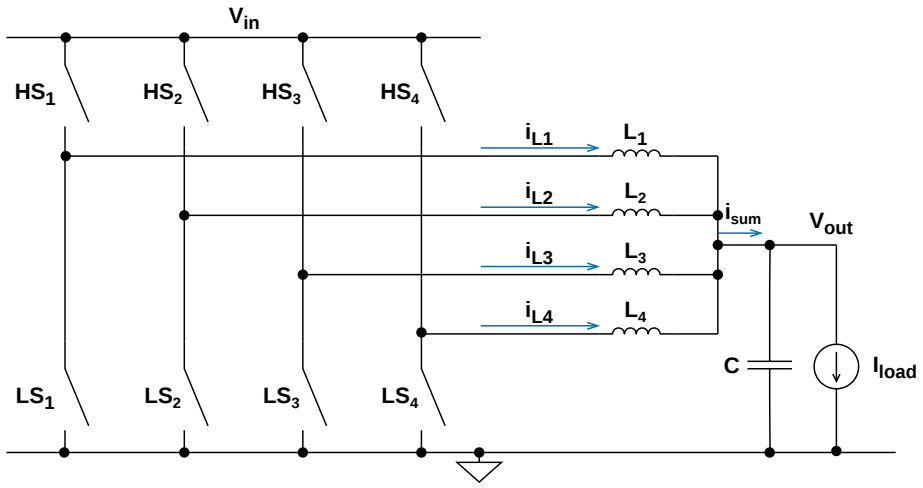


Figure 3.1: Schematic of a multiphase buck converter with 4 phases.

3.1 Multiphase buck converter

Suppose a buck converter is required to deliver 100 A to a load and the half bridge is composed of switches with 10 $m\Omega$ R_{on}; let us focus on the switching losses: the power dissipation on the switches would be roughly $R_{on} \times I_{load}^2 = 100\,\mathrm{W}$. If now two half bridges with the same switches are connected in parallel, the current in each bridge is half of the total current (50 A) and the power dissipation will be roughly $R_{on} \times \frac{I_{load}^2}{2} \times 2 = 50\,\mathrm{W}$, which is half of the original power. This effect of reducing the power dissipation can be generalized for any number of half bridges (phases), in this way:

$$P_{multiphase} = \frac{P_{standard}}{N}$$

Where N is the number of phases utilized.
Lower current through the transistors means less thermal management constraints, but also means that the heat is no longer concentrated in a small area as it is shared over all the transistors. Obviously this comes at the cost of a higher BOM since more phases require more transistors and inductors. Another advantage is that due to the lower current on each switch, the voltage drop on them is reduced, hence at the output, the DC voltage will be closer to the target set by the duty cycle, compared to a standard buck converter (the same will happen on the voltage across the DCR of the inductors).
At the output, all the inductor currents from each phase sum up and the full load current is delivered; if the inductance values are the same for each phase, then the ripple amplitudes for each phase are also the same. As already mentioned, the current ripple is independent from the average current in

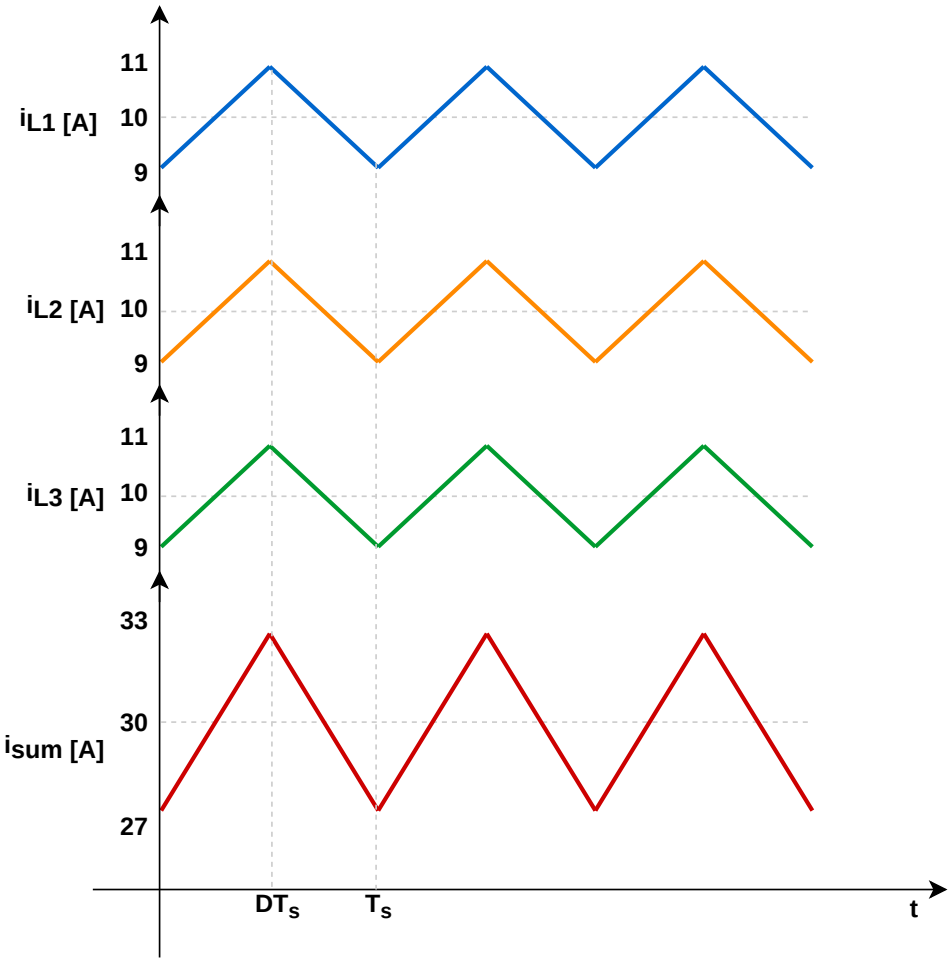


Figure 3.2: Inductor currents and their sum for a 3-phase buck converter. Each phase carries 10 A DC with a superposed ripple of 2 A.

the inductor and so, if the standard buck converter would develop a ripple of i_{pp}, the multiphase one with the same inductance value for each phase would instead develop $N \times i_{pp}$ (Fig.3.2). This will then cascade to the output voltage ripple which will also be multiplied by N.
It appears that in order to use a multiphase topology, an increase in ripple has to be accepted and this only amplifies the BOM issue: increasing the number of phases increases the size of the converter since more transistors and inductors have to be added, but not only that; in order to counter the increase in the ripple, bigger inductors are required, increasing once again the overall size.
Notice though, that for the same inductance value needed for the standard buck converter, in the multiphase topology the inductors require a lower limit on the saturation current since only a fraction of the entire load would

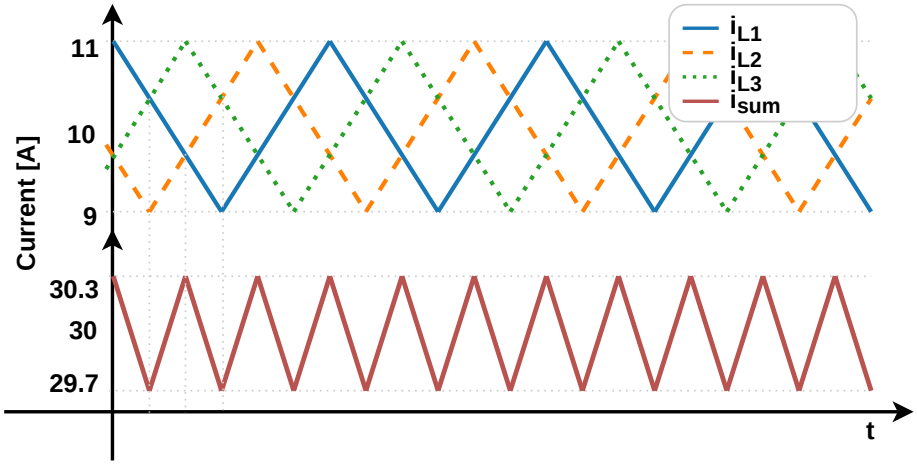


Figure 3.3: Current waveforms in a 3-phase interleaved buck converter. The phase driving signal is delayed by 120° between the phases.

flow through, leading to potentially smaller inductors and with lower DCR. The issue of ripple amplification arises from the way the transistors in each phase are driven: when each phase is driven by the same signal, the current waveforms at the output node are in phase and sum constructively. By delaying the driving signal between the phases (interleaving), this problem can be suppressed.

3.1.1 Interleaving

In interleaving operation, the converter half bridges switch at the same frequency but with a phase delay relative to each other: if the switches of phase N_0 are driven with a PWM signal with a certain duty cycle, the other phases will be driven by the same signal, but delayed by a multiple of $\frac{360°}{N}$ (i.e. in a 2-phase converter, phase N_1 is driven by the same signal of N_0, but with a 180° delay).

$$\varphi_{Ni} = i \times \frac{360°}{N} \tag{3.1}$$

Where i is the index of the phase under consideration ($i = 0, 1, 2, ..., N-1$). In Fig. 3.3, the inductor currents in a 3-phase buck converter are plotted, where the phases are driven by delayed signals as per Eq. 3.1.
Compared to Fig. 3.2, the ripple at the output has been attenuated because the peaks of current are not developing at the same instant for every phase, but are spaced in time.
This appears as a significant improvement, but an even greater result could be achieved with multiphase converters: the ripple could be totally elimi-

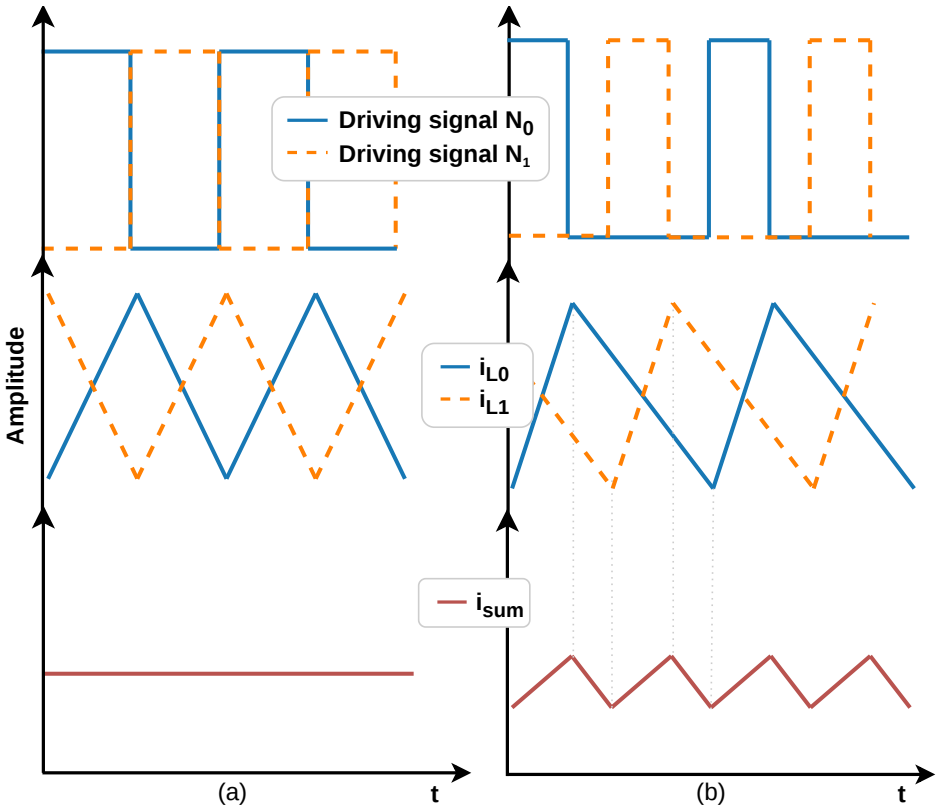


Figure 3.4: Driving signals, Inductor currents and output current of a 2-phase buck converter in interleaving mode: (a) when the duty cycle is 50 % and (b) when the duty cycle is 30 %.

nated if the timing of the phases is matched with a proper duty cycle.
Let us focus on a 2-phase buck converter for simplicity: when the driving signals are in opposition of phase, the resulting inductor currents will be one the opposite of the other and will cancel each other by destructive interference at the output node, except for the DC value which will instead double. This behavior is not always true though; it will only happen if the driving signals are perfect square waves with 50 % duty cycle (Fig. 3.4a).
Notice that the frequency of the output current ripple is now double the switching frequency and in the case of an N-phase converter it would be $N \times f_s$.
Dealing with a higher ripple frequency results in a significant advantage in the design: the required constraint on the reactive components for filtering are relaxed. At higher frequency the output inductor and the capacitor can be shrunk and the ripple amplitude becomes easier to minimize.
It can be demonstrated that in order to completely eliminate the ripple for a 3-phase converter the duty cycle must be 33.3 % or 66.6 % (HS on for $\frac{2}{3}$

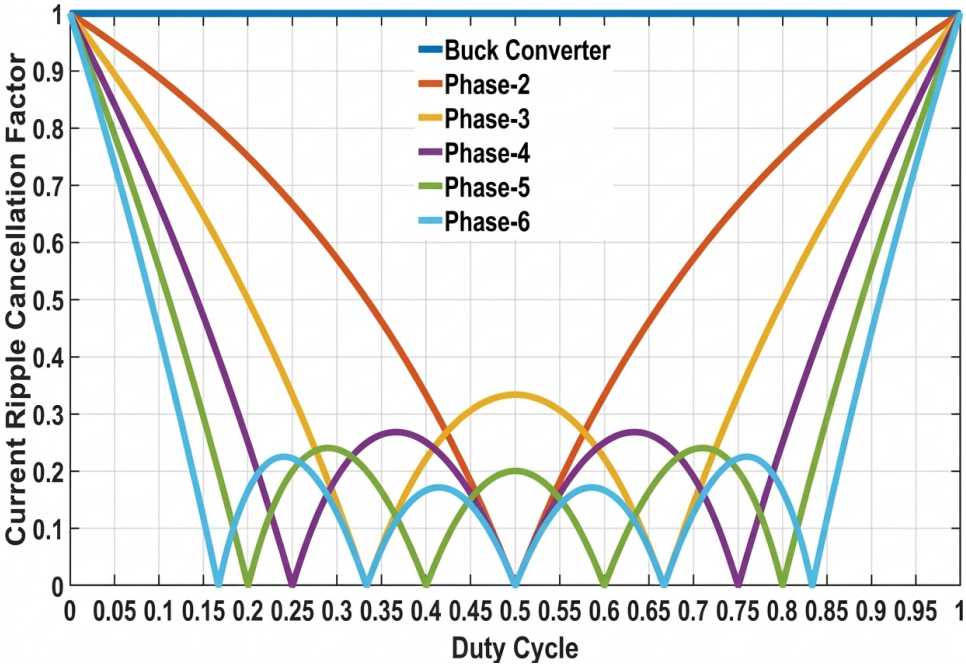


Figure 3.5: Ripple cancellation in multiphase interleaved buck converters [1].

of the switching period or LS on for $\frac{2}{3}$ of the period).
In general, for total ripple cancellation, the phases must be driven as per Eq. 3.1 and the duty cycle set as per Eq. 3.2.

$$D = \frac{i}{N} \qquad (i = 1, 2, ..., N-1) \tag{3.2}$$

Fig. 3.5 shows the reduction in ripple in multiphase interleaved buck converters when the duty cycle is varied for different numbers of phases. It can be observed that at certain discrete duty cycles, complete ripple cancellation is achieved.
Note that even if the ripple is not totally eliminated, its amplitude is still reduced when the duty cycle is close to the correct ones.
In [1] an interleaved stacked buck converter is presented. The combination of using a stacked topology with an interleaved buck converter results in a total cancellation of the ripple at the whole range of duty cycles and not just for a certain discrete number anymore.
This topology makes use of an additional auxiliary phase that blocks the dc current and replicates the ripple current with opposite sign (Fig. 3.6) so that at the output the ripple drops to zero.

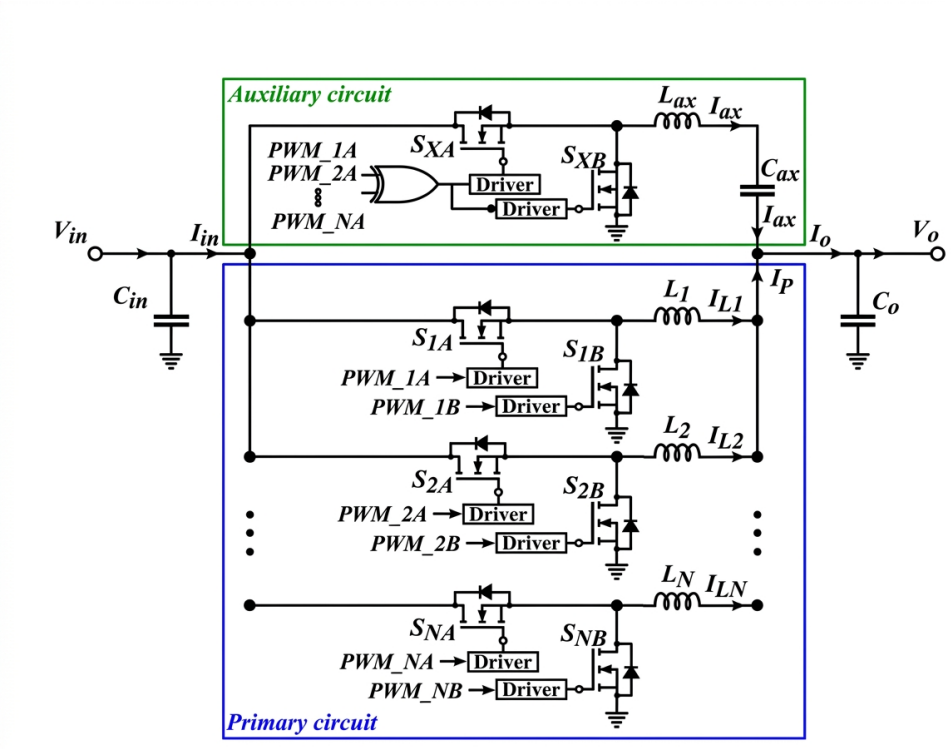


Figure 3.6: Multiphase interleaved stacked buck converter topology [1].

3.1.2 Phase shedding

All the advantages of using multiphase converters disappear if the current is not well balanced between the phases. Multiphase converters need an accurate current-balancing scheme to ensure the correct operation.
While using more phases cause a better management of conduction losses and heat dissipation, having many components switching at the same time could increase EMI and switching losses.
At high load currents, a big number of phases helps in this regard, but at low load condition, the positive effect of these many phases will disappear; rather there will be a disadvantage because the switching losses will certainly overcome the conduction ones, heavily degrading the efficiency. Fig.3.7 depicts the efficiency behavior of the converter at increasing numbers of phases: it can be observed that efficiency benefits from higher number of phases only at high load current.

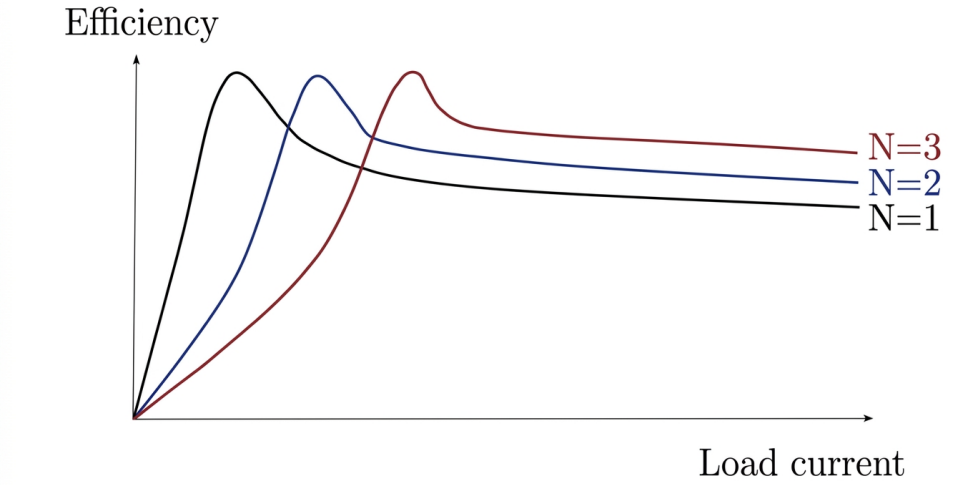


Figure 3.7: Efficiency behavior in a multiphase buck converter at different number of phases [2].

Phase shedding is a mechanism that optimizes the efficiency of the converter by activating or disabling some phases in the converter based on the load current: when the load current is very high, all phases will conduct to minimize the losses; conversely, when at low current condition, most phases will be turned off to remove additional useless switching losses, given the very low effect of conduction.

3.2 Design in SIMPLIS

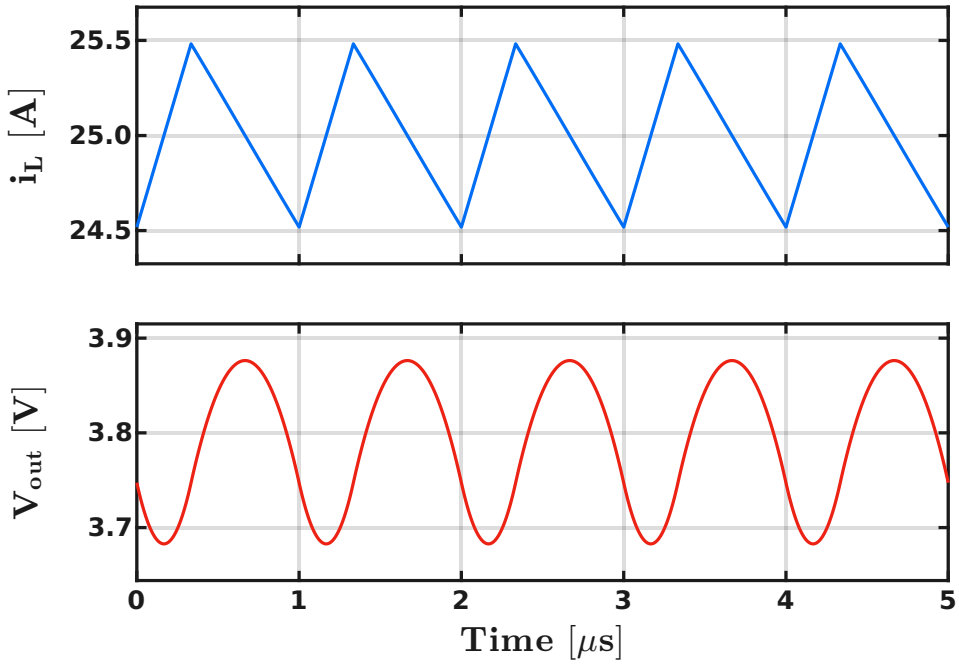
The design of the multiphase DC-DC for the VDD_p rail will follow a similar flow to the converter showed in chapter 2, starting with a behavioral analysis in SIMPLIS and concluding with a more accurate implementation in Cadence Virtuoso.

3.2.1 Initial setup

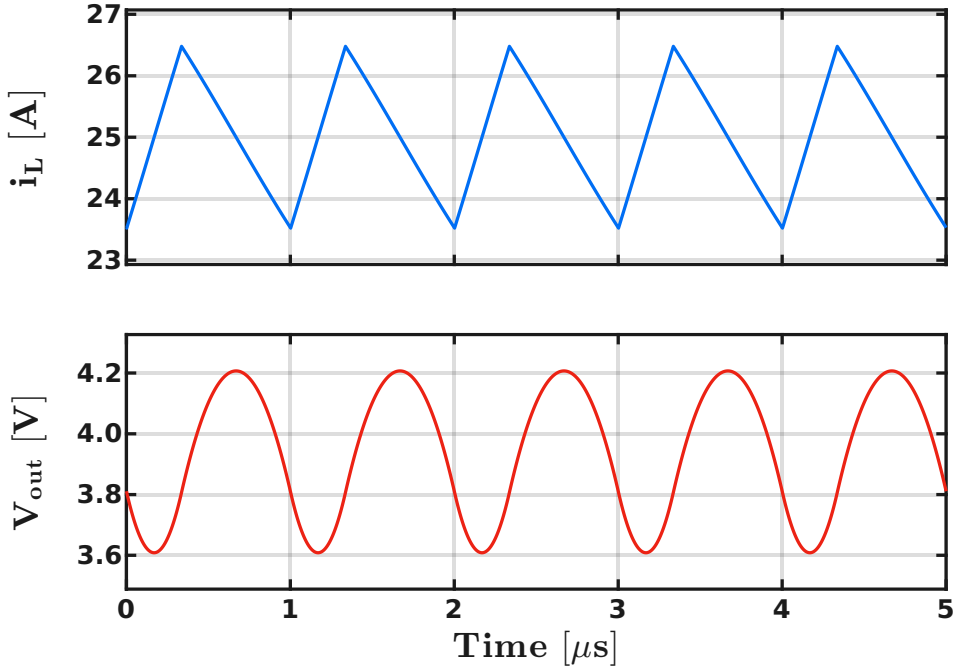
The initial setup includes a standard buck converter; this will be compared to a multiphase topology to understand the practical performance limit of the topology.
The setup targets and components are the following:

- $V_{in} = 12\,\text{volt}$
- $V_{out} = 4\,\text{V}$
- I_{load} = 1 - 25 A
- D = 33.3 %
- Inductor L = 2.8 μH
- Capacitor C = 625 nF
- Infineon BSC110N06NS3 switches

The transistors are the same ones used for the analog domain and are driven at $V_{GS} = 10\,\text{V}$ for a $9\,\text{m}\Omega$ R_{on}.
The output waveforms of the simulation are plotted in Fig. 3.8a and for 1 MHz frequency, the ripple values are: $i_{pp} = 960\,\text{mA}$ and $v_{pp} = 190\,\text{mV}$ which are close to the expected values from Eq. 2.10, 2.13.
In Fig. 3.9 the efficiency is depicted for different switching frequencies. Even in this first setup in which switching losses are not considered (apart from the charging/discharging of the gate capacitors of the switches) and the inductor is ideal, the maximum efficiency that can be achieved is around 90 %, which means that the real efficiency would be lower than 90 %.
Let us now introduce two additional phases to the setup without changing the parameters. These phases are driven without interleaving and the results are plotted in Fig. 3.8b. The ripple has increased threefold, while the output voltage mean value is closer to the target. The efficiency (which is not showed) has increased because the conduction losses are now lower. The simulator can list the power losses in the transistor and they are presented in Tab. 3.1.



(a)



(b)

Figure 3.8: Inductor current and Output voltage of the single phase converter (a) and the 3-phase converter (b) at 25 A load.

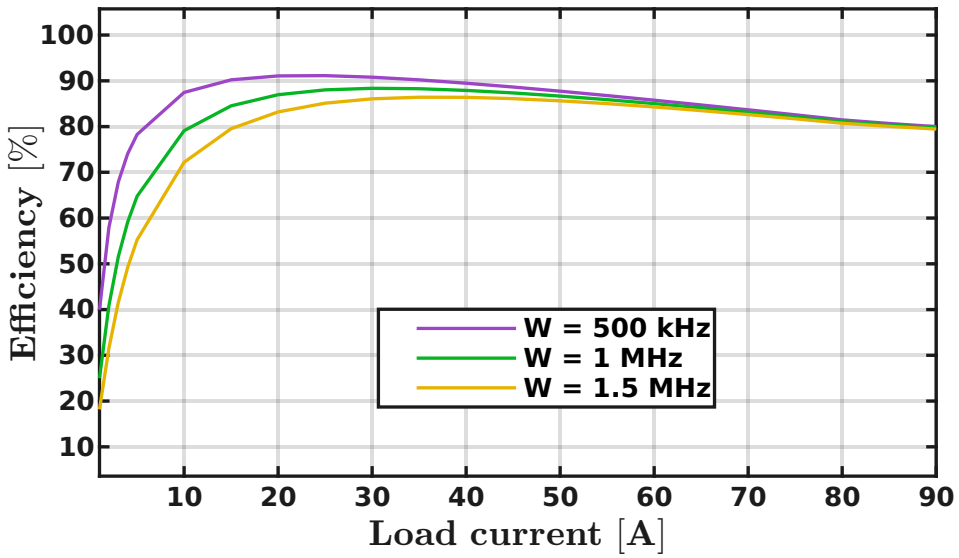


Figure 3.9: Efficiency of the converter vs. Load current at different frequencies.

The conduction losses in the second case are approximately one ninth of the standard buck converter, but there are tree times the transistors, so in reality, the total conduction loss is one third.
Notice how the power dissipation in the gate is the same in any case and that is exactly why there is an improve in efficiency: the conduction losses reduce while the power dissipation on the gate is fixed. The power on the gate has to be multiplied by the number of transistors and if the number of phases is high or the load current is low, this power dissipation starts to become higher than the conduction contribution and leads to lower efficiency.
The low side power dissipation is approximately twice the high side contribution due to the fact that the duty cycle is 33 % meaning that the low side conducts current for two thirds of the period; this is the reason that in very high conversion ratio applications the low side switch should have a very low R_{on}.

Single-phase	**Gate charge/disharge**	**Conduction loss**
P_{HS}	200 mW	1.8 W
P_{LS}	200 mW	3.7 W
3-phase	**Gate charge/disharge**	**Conduction loss**
P_{HS}	200 mW	205 mW
P_{LS}	200 mW	425 mW

Table 3.1: Transistor dissipation in the standard and in the 3-phase converter.

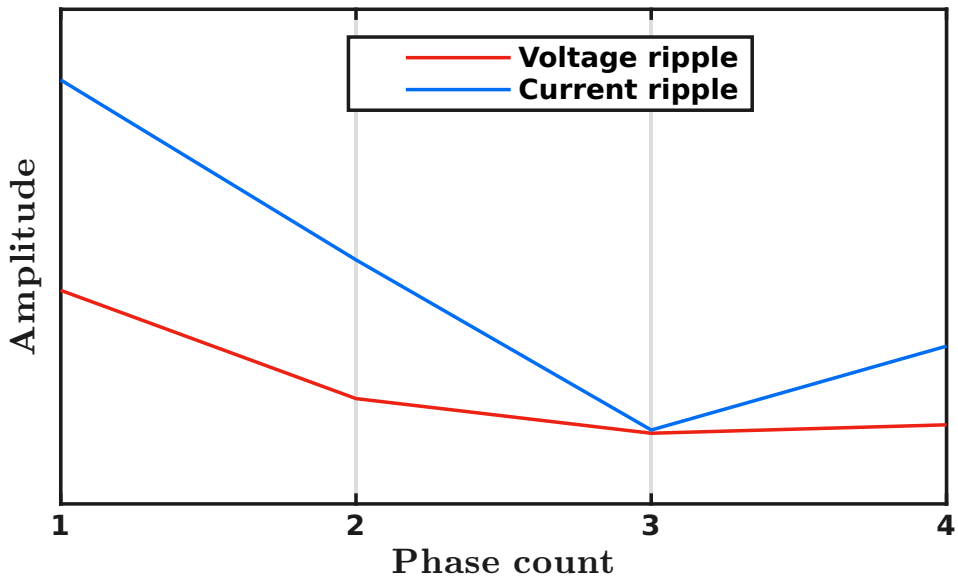


Figure 3.10: Simulated ripple amplitude for different phase count.

3.2.2 Optimal phase count

Before realizing the final interleaved multiphase setup, the optimal number of phases must be defined.
An analysis was conducted with a phase count from 1 to 4, keeping the same components and parameters. The behavior in terms of ripple and efficiency is depicted in Fig. 3.10, 3.11. These results are meant to represent just the behavior of the converter under analysis and not the actual accurate values: it can be observed that the lowest ripple is achieved for 3 phases; this is because the duty cycle is 33 % and it matches the condition of ripple cancellation when 3 phases are utilized. The efficiency behavior has been calculated with few points but still resembles the expected behavior of Fig. 3.7 where the peak efficiency moves toward higher load currents when more phases are used.
Given these results a 3-phase implementation is chosen, since using more components without any tangible advantage would not make any sense; on the other hand, using less components (i.e. a 2-phase implementation) shows instead a tangible disadvantage in ripple amplitude.

3.2.3 3-phase buck converter

For the 3-phase interleaved converter setup, the driving signals are delayed by 120° between each other (Fig. 3.12).
The chosen inductor for each phase is the 3 μH TDK B82464D6302M000 with a 21 mΩ DCR.

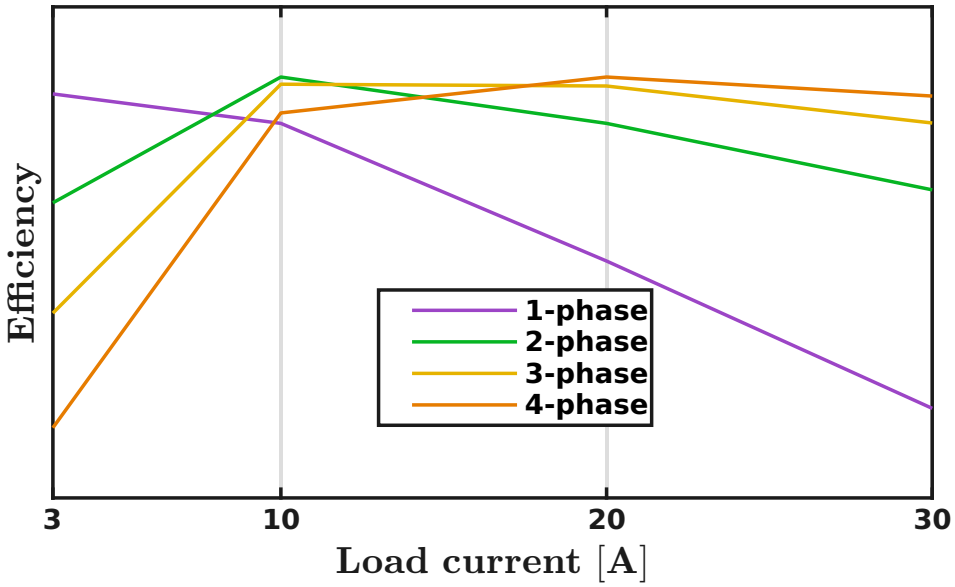


Figure 3.11: Simulated efficiency behavior for different phase count.

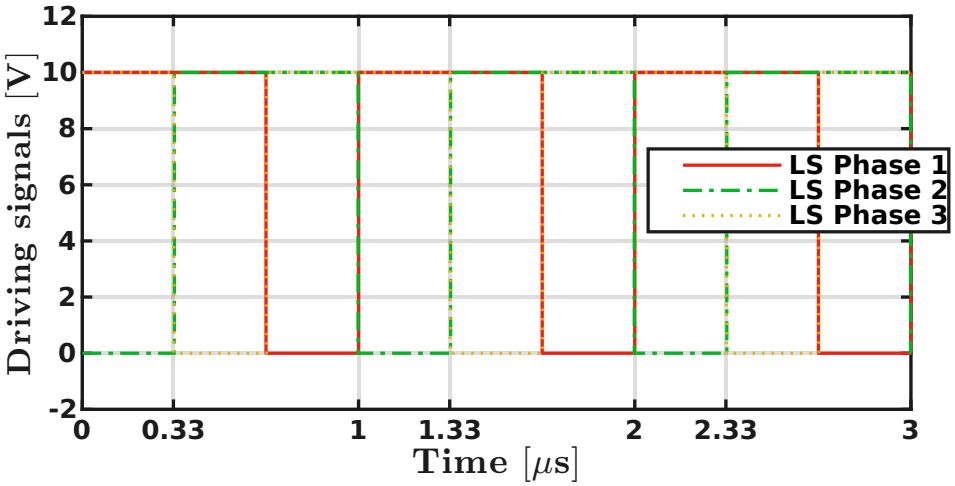


Figure 3.12: LS Gate driving signals.

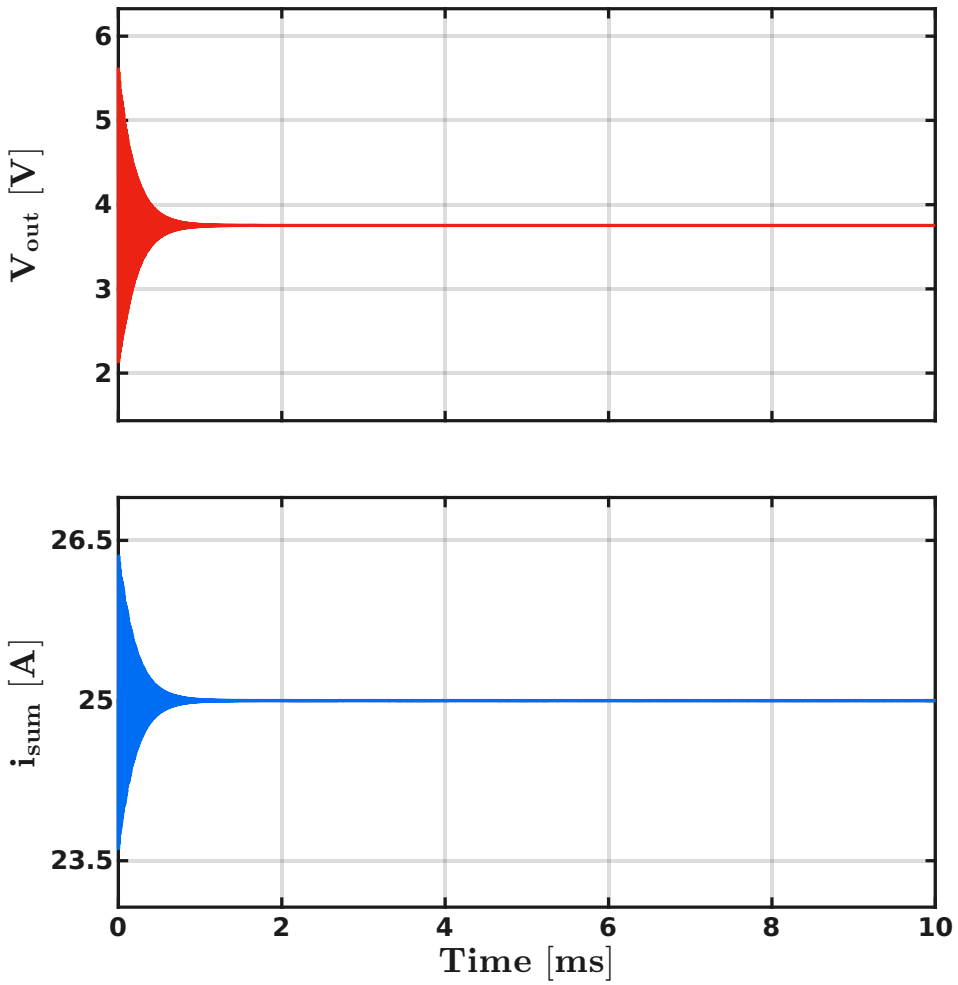


Figure 3.13: Output voltage and total output current of the 3-phase converter in a 10 ms transient simulation.

Till now, only steady-state operation has been analyzed, but this time the converter was simulated also in transient operation to better visualize the extent of ripple minimization due to interleaving (Fig. 3.13). From this simulation it can be observed that the current ripple as well as the voltage ripple are very low (less than 1 mA and 1 mV).
In Fig. 3.14, 3 peaks of the waveforms are in a 1 μs period, an indication of the increase in the ripple frequency in interleaved operation.
The output voltage DC value, again has an offset from the 4 V target due to the on-resistance of the MOSFETs and the DCR of the inductor.
The efficiency was also calculated and is plotted in Fig. 3.15: a good improvement can be seen in comparison with Fig. 3.9 due to multiphase interleaving operation (note that now DCR losses are also taken into account).

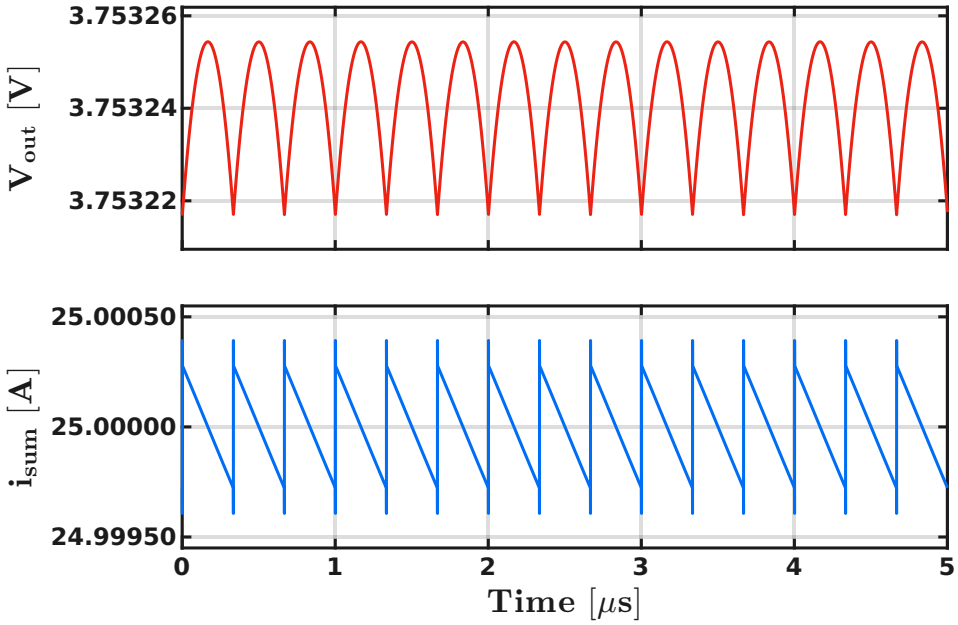


Figure 3.14: Output voltage and total output current of the 3-phase converter in steady-state.

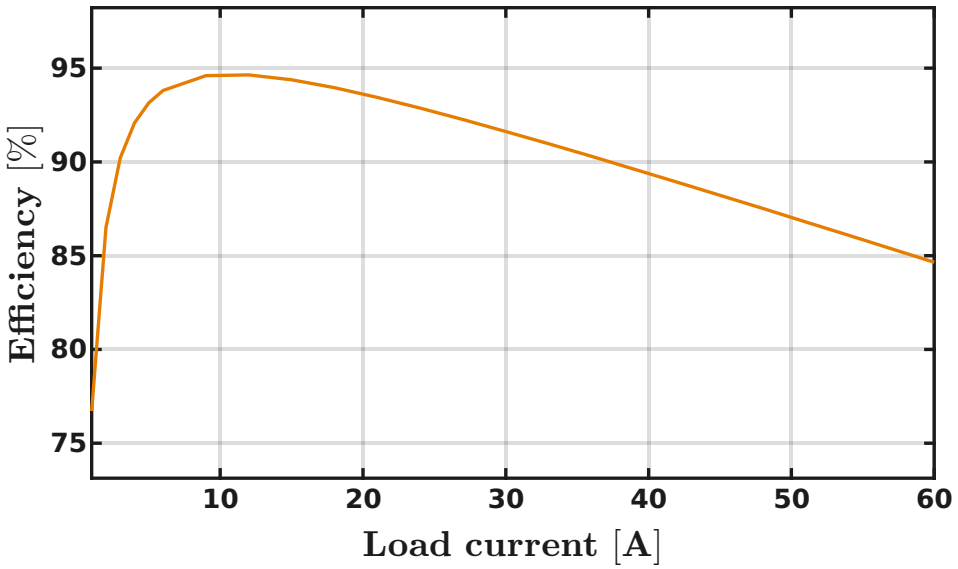


Figure 3.15: Efficiency of the 3-phase converter with load current up to 60 A.

3.3 Design in Cadence Virtuoso

3.3.1 Components evaluation

The models of transistor BSC110N06NS3 and inductor TDK B82464D6302M000 were imported in the Virtuoso software for simulation.
The transistors are driven ideally in interleaving mode with 10 V V_{GS}; when simulating at the maximum current load, a problem arises: the three phase nodes of the converter exhibit large overshoots and ringing.
Ringing on the phase node is caused by parasitic inductances and capacitances in the transistor. These parasitic components could be amplified by the additional parasitics introduced by the package and also by the printed circuit board (PCB) layout.
A simple test was conducted in order to verify the cause of ringing: when the PSpice model of transistor BSC110N06NS3 is modified to have 0 H drain and source parasitic inductance, the ringing completely disappear, leaving a perfect square wave as the phase node voltage.
Note that some parasitic inductance will always be present in any case when dealing with external discrete components: when connecting pins to the board, the bonding wires will not act as perfect connections, rather they will show some parasitic inductive component.
Another simulation was conducted with Infineon IAUZN04S7L012 40 V transistor.
This switch presents much less pronounced ringing on the phase nodes due to lower parasitic inductances in the package.
This transistor has a typical R_{on} of 1.25 $m\Omega$ when driven at 10 V V_{GS}, but even when a 5 V signal is applied, the transistor still exhibits a far lower resistance (under 2 $m\Omega$ from Fig. 3.16) than switch BSC110N06NS3 at 10 V, which is a very good improvement given the high current load operation.
Although this very low R_{on} is ideal for the high current application under test, this high voltage transistor (as well as the previous one) introduces very high capacitance loading on the phase node that will severely affect efficiency due to switching losses.
This effect is further accentuated by the fact that three phase nodes will be loaded instead of only one as in the standard buck converter.
Nevertheless, the peak efficiency stands at around 89 %, which is a good result, but to keep things in perspective, an 89 % efficiency in the buck converter from chapter 2 means an average power loss of just above 800 mW at full load (2 A), while the same efficiency at full load (25 A) in the current setup translates instead in roughly 12.5 W, an actual 15 times increase while the perceived efficiency is the same.
In Fig. 3.17 the input current to the converter is plotted.
Big capacitive spikes can be observed every time the HS switch turns on. In the 3-phase configuration this happens 3 times in a single switching period

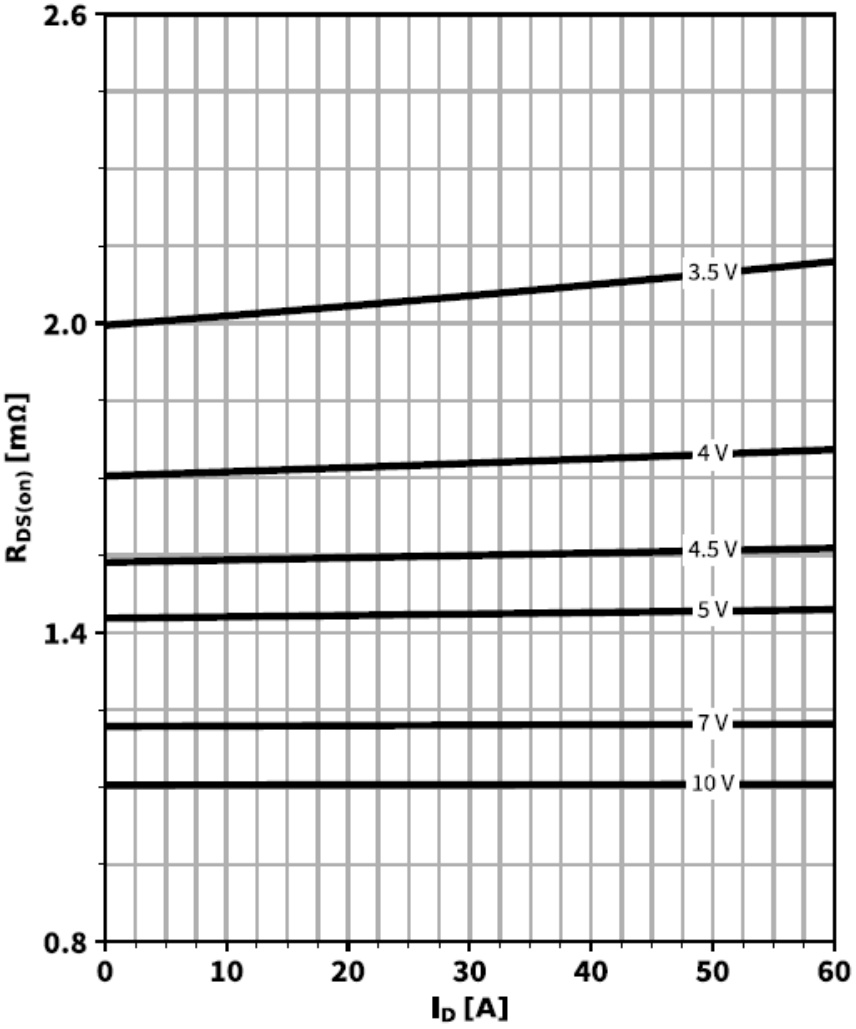


Figure 3.16: Transistor IAUZN04S7L012 R_{on} vs. Current from Infineon datasheet.

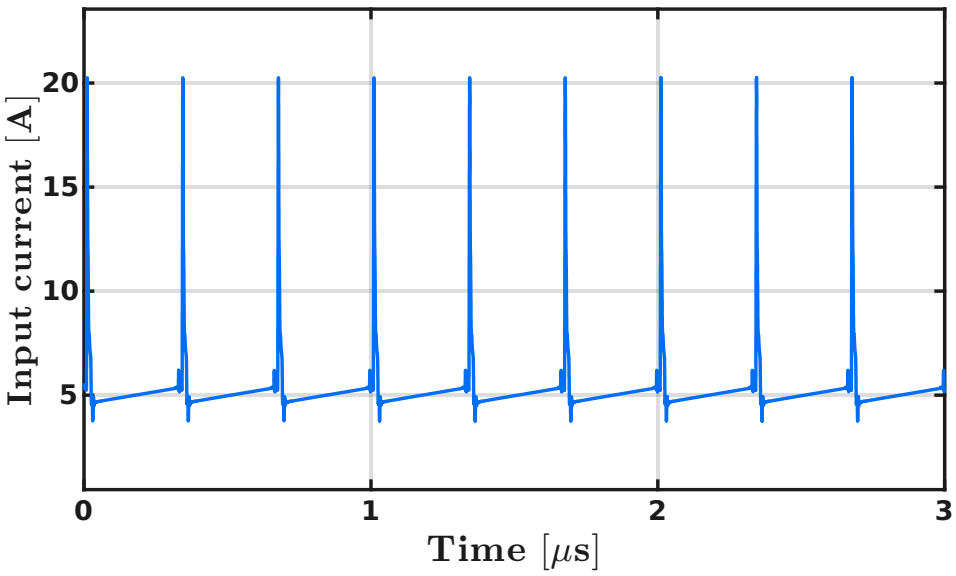


Figure 3.17: Input current to the 3-phase converter simulated at 15 A load.

and this is the reason switching losses can be very high.
The waveform presents very high overshoots before settling to the expected value of the inductor current. Choosing a lower rated discrete switch with less parasitic capacitance would be a better choice in this scenario to minimize the switching losses.
While it is true that the requirement for the power core of the system is 25 A, since the buck converter now operates in three phases, lower current rated switches can be used without any major concern.
Keeping the voltage rating reasonable to not incur in any issue, since constant switching can generate high spikes in the phase node that could break the transistor, a 30 V MOSFET is chosen for the last simulation.
Infineon MOSFET BSZ0506NS is a 30 V switch with a very low R_{on} of 4.4 $m\Omega$ which boasts very low parasitic capacitance in the datasheet compared to the transistors previously analyzed.
This transistor is paired with a very low DCR inductor to maximize the efficiency by minimizing both the switching losses as well as the conduction ones.
The chosen inductor is TDK B82477P4332M000: It is a 3.3 μH wire wound inductor rated for 13.5 A, occupying a 12.5 mm $\times$ 12.5 mm $\times$ 8.5 mm footprint and exhibiting an 8 $m\Omega$ DCR.

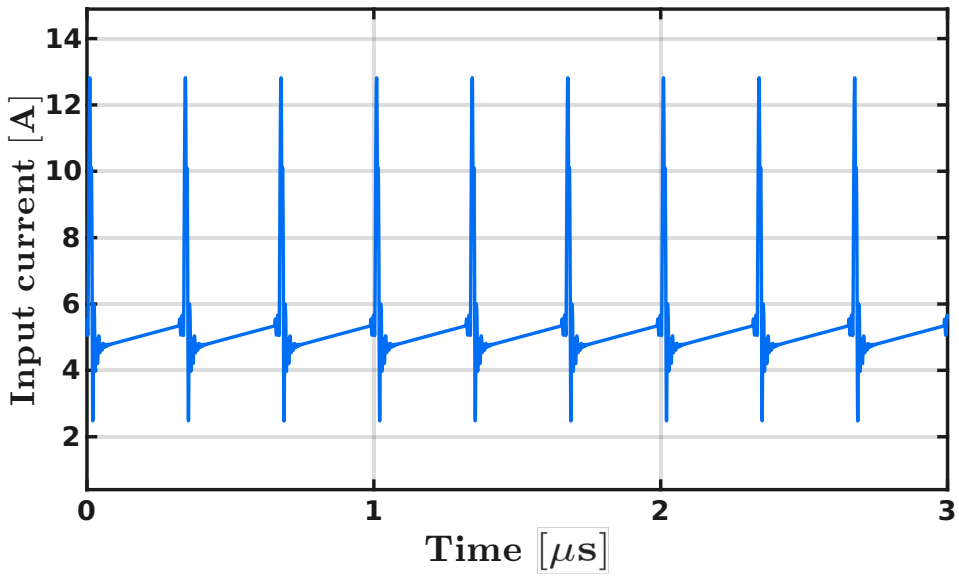


Figure 3.18: Input current to the 3-phase converter using transistor BSZ0506NS for the switches.

3.3.2 Results and efficiency

The input current to the converter is plotted in Fig. 3.18 where lower spikes compared to 3.17 are observed. This confirms the advantage gained when utilizing transistor BSZ0506NS in the design.
A transient simulation with 1 ms duration was conducted at 1 MHz switching frequency and the output voltage is plotted in Fig. 3.19: the output DC value is very close to target and the ripple amplitude is very low ($v_{pp} \approx 1$ mV).
Finally, the efficiency was calculated at different load conditions and the graph is shown in Fig. 3.20 (the efficiency graph at 0.5 MHz frequency starts at a higher load point because at lower frequency, the minimum current to guarantee CCM is higher).
At 1 MHz frequency the efficiency is higher than 90 % for the whole range of load current conditions, with a peak efficiency in medium load condition of around 96 %.

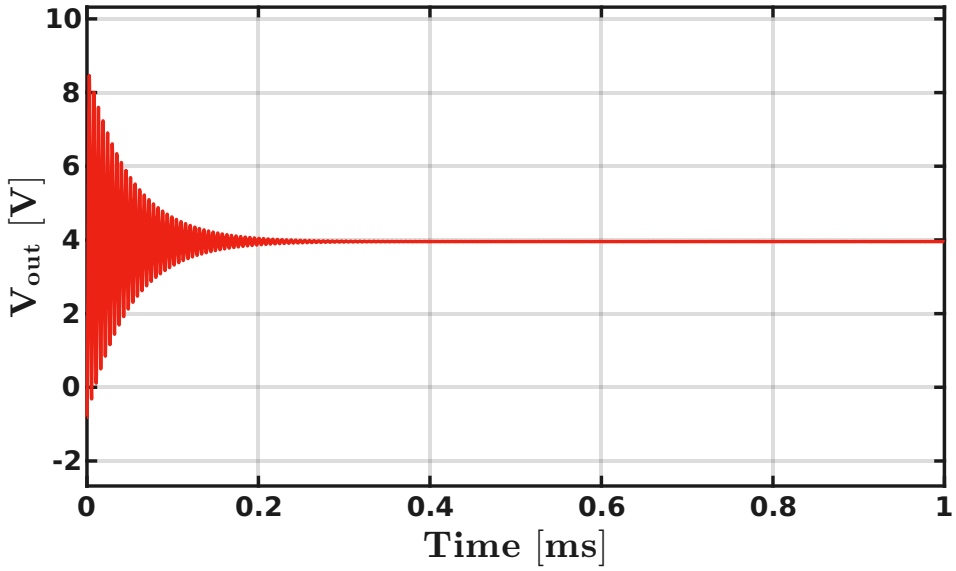


Figure 3.19: 3-phase converter Output voltage waveform.

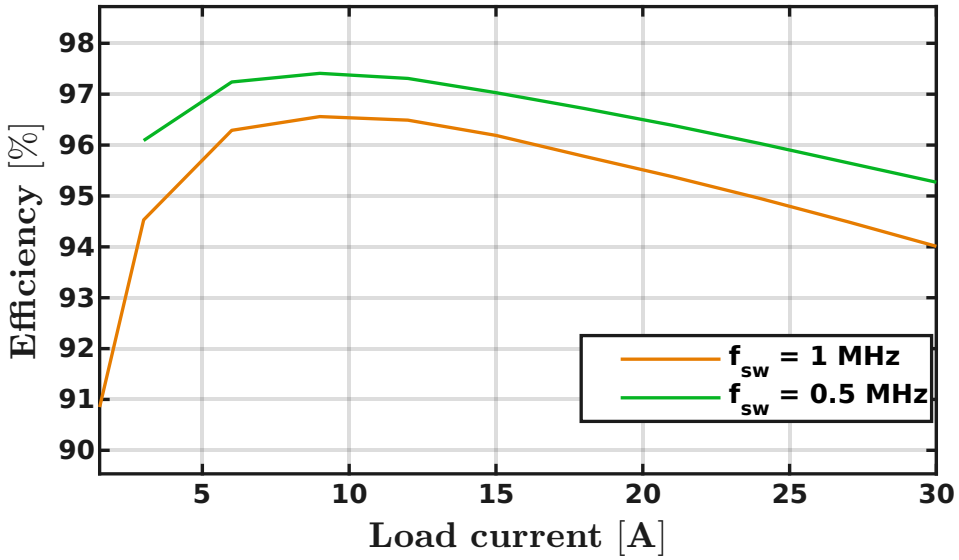


Figure 3.20: Efficiency vs. Load current of the 3-phase converter at 500 kHz and 1 MHz switching frequency.

Chapter 4

Digital domain power supply: architectural analysis and implementation

This chapter is dedicated to the analysis of the architecture that will supply the digital section of the headlamp system comprehending the memory and the control unit that manage the turn on/off of the pixels in the matrix. An LDO with a MOSFET pass transistor, based on TSMC BCD 180 nm technology, will be used to regulate the VDD_a rail to 1.8 V.

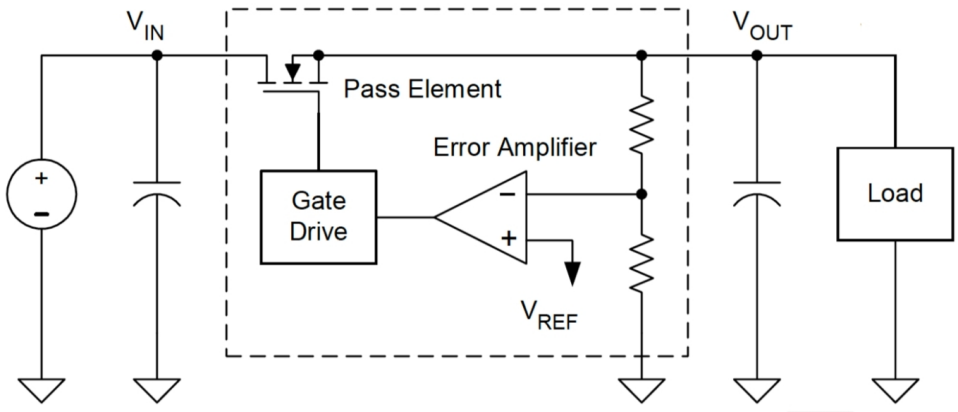


Figure 4.1: Schematic representation of the LDO. The series pass element and the control loop are highlighted [3].

4.1 Linear regulator working principle

The linear voltage regulator uses a series pass element between the input and output to continuously deliver power and regulate the output voltage. The output is compared to a reference voltage, that usually comes from a bandgap circuit, through an error amplifier and fed back to the gate of the pass transistor. This way the loop continuously controls the operating point to ensure the output voltage remains constant at the desired value.
In Fig. 4.1, the output voltage is not directly compared to the reference, but is scaled by a resistor divider beforehand. The reason is that a reference voltage exactly equal to the desired output value may not be available, hence the voltage needs to be scaled to match the available reference.
Since the pass element is a transistor, there will be some constraint on the voltage between the input and the output (source and drain terminals in a MOSFET) for the regulator to properly work.

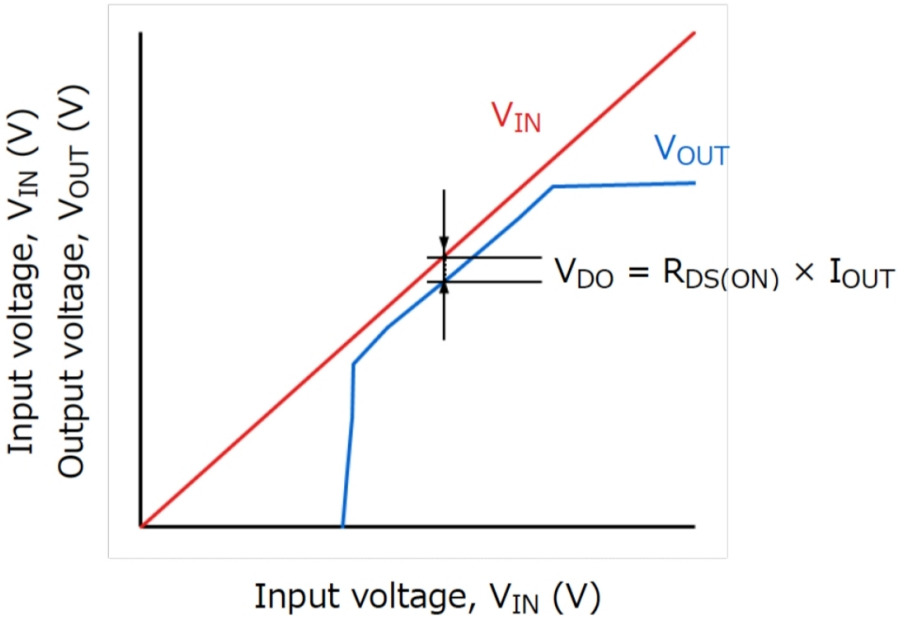


Figure 4.2: Input and Output voltage vs. Input voltage of an LDO.

In a MOSFET transistor, if the voltage between the drain and the source (V_{DS}) becomes too low, the transistor enters in the triode region and the output voltage will follow the input one, except for a voltage drop given by the product of the transistor R_{on} and the load current. In fact, in the triode region the transistor will act as a resistor (like the switches used in the buck converter) and the output voltage will not remain constant if any voltage change affects the input; output voltage regulation is thus lost.
The minimum required voltage for the regulator to properly work as intended

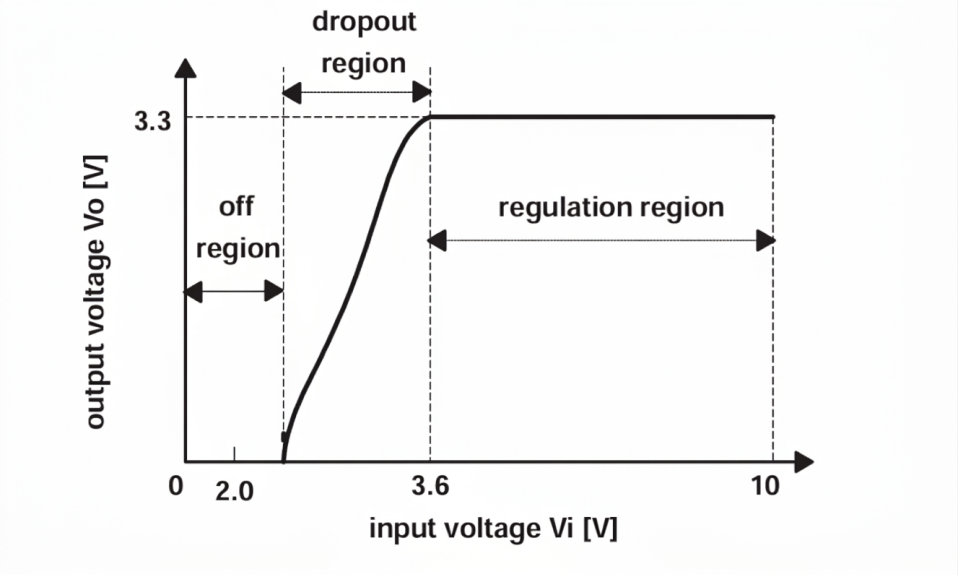


Figure 4.3: Dropout region of TPS76733 (3.3 V LDO).

is referred to as the voltage dropout of the regulator (V_{DO}).
If this dropout voltage is relatively small (usually, under 1 V), the linear regulator is categorized as a low dropout regulator.
The expected behavior of the regulator as the input voltage changes is illustrated in Fig. 4.2: when the input voltage is not high enough compared to the targeted output (at least above it by a V_{DO}), proper regulation cannot be maintained and the regulator is said to be in dropout.
The dropout region is highlighted in Fig. 4.3 for LDO TPS76733 from Texas Instruments: the dropout voltage of this LDO is around 350 mV, hence the regulation starts to drop when the input reaches 3.65 V given the aim of the regulator to maintain the output at 3.3 V.
When conditions vary in the load current or in the input voltage, the loop reacts and the error amplifier sets the V_{GS} of the pass transistor to the proper voltage required for regulation in said condition.
Fig. 4.4 illustrates an example of the operating points of the pass transistor at different conditions. The assumed initial operating point is A: the error amplifier sets the correct V_{GS} to achieve the target output voltage. Assuming this condition is static, the transistor could be replaced by an actual resistor that will yield the same result.
If now the load current increases, the regulator shifts to point B, where V_{DS} remains equal as in A, but the transistor is able to output more current. This is made possible by the error amplifier which set a higher V_{GS} to ensure that the transistor V_{DS} does not change even when higher current is drawn by the load.

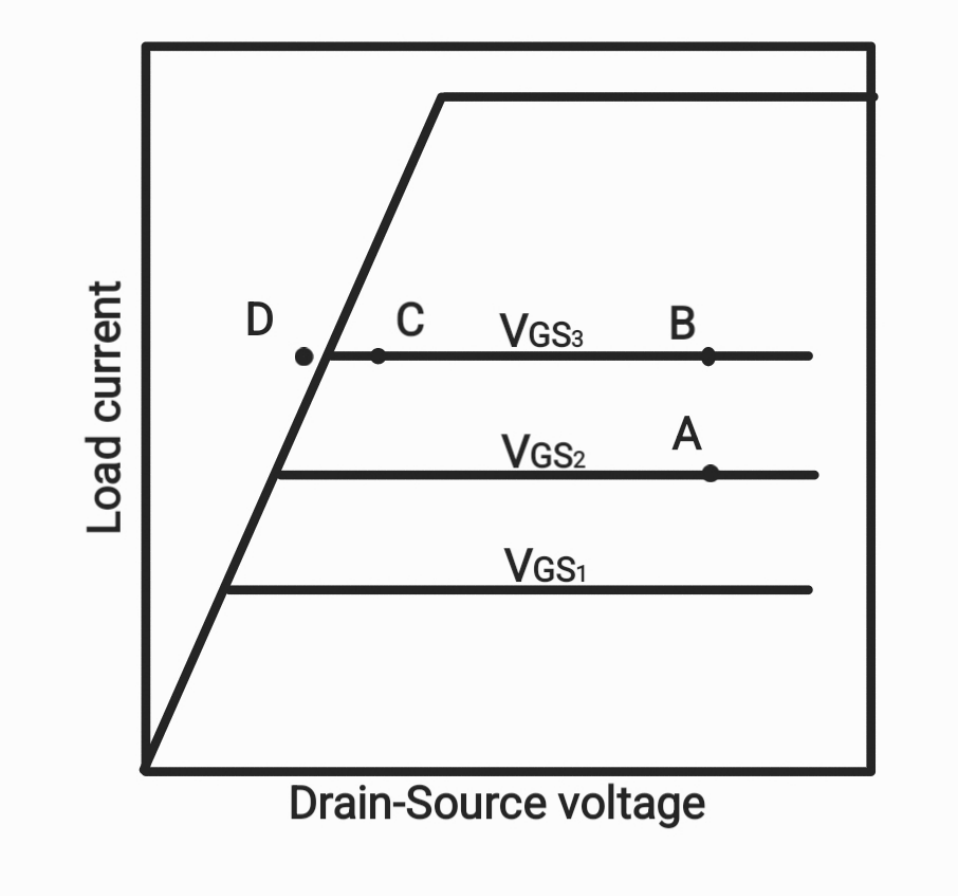


Figure 4.4: Operating points of the NMOS pass transistor in an LDO in different conditions (adapted from [3]).

Note that an analogous process would happen if the load current decreases: the error amplifier would set a lower V_{GS} and the V_{DS} would be maintained. Point C is the result of a decrease in the input voltage: V_{DS} is now lower since to maintain the output at the same voltage, a lower difference between the source and the drain is needed.
When the LDO is forced to point D, regulation cannot be achieved as the transistor is not able to reduce its drain to source voltage.
Note that this example describes the behavior of the regulator when an NMOS transistor is used as the pass element; when using a PMOS the process is complementary.

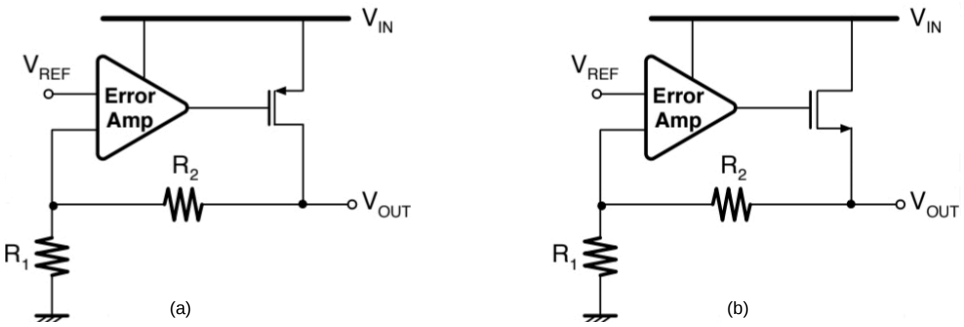


Figure 4.5: LDO implementation with a PMOS (a) or an NMOS (b).

4.1.1 Choice of the pass transistor

The choice of the type of MOSFET used in the regulator should be based on the advantages that it offers:
An NMOS transistor presents a low output impedance node (the output is its source terminal) and thus it is easier to implement a stable control loop around it; it could even be realized without an output capacitor (capless solution).
Due to the higher mobility, an NMOS can be smaller than its counterpart and introduces less parasitics, hence it is the best choice when area minimization is an objective.
The loop is faster in the case of the NMOS as it directly modulates the V_{GS} of the transistor (again, the output is the source terminal).
There is one main disadvantage in using the NMOS as the pass transistor though: the dropout voltage is higher compared to the PMOS.
Referring to Fig. 4.5, the minimum that v_{in} should be to maintain proper regulation is $v_{out} + V_{GS}$. The dropout will then be equal to V_{GS}, which is higher than the usual V_{DO} for a PMOS device. The reason is that the error amplifier cannot supply the gate of the transistor with a voltage greater than v_{in}. A solution to this problem is to supply the pass transistor and the error amplifier with different voltages so that the amplifier can output voltages higher than the input applied on the NMOS. This is done by implementing an additional charge pump circuit that boosts the input voltage and supplies the error amplifier. On another note, the charge pump can make the system slower and add noise and also increase the area consumption.
A PMOS device is less complex to implement in the design and guarantees the lowest dropout (the source terminal is now the input and the transistor acts like a current source), but adds a high impedance node at the output, making the loop more difficult to stabilize.

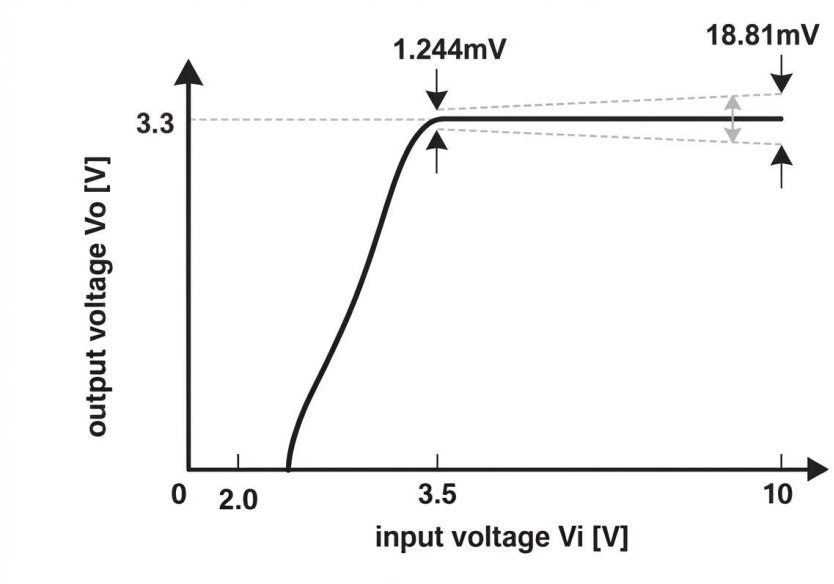


Figure 4.6: TPS76933 Output Voltage with respect to the Input Voltage.

4.1.2 Line and load regulation

Line regulation is the variation in the output voltage given a change in the input while the load current is constant. Ideally a good line regulation should be as close to zero as possible, meaning that the output does not change at all even when the input varies a lot.
Line regulation can be expressed in $[\frac{mV}{V}]$ as the ratio of the variation in the output from the target voltage with respect to input voltage or it can be expressed in percentage referring to the variation in the output from the target over a 1 V input change from nominal value. In the case of $v_{in} = 3.3\,\mathrm{V}$ and $v_{out} = 1.8\,\mathrm{V}$, 1 % line regulation would mean a variation of 18 mV when the input changes from 3.3 V to 4.3 V for example.
In Fig. 4.6, the change in the output voltage with respect to input is depicted for Texas Instrument TPS76733 3.3-V LDO. It can be observed that the output voltage deviates from target (3.3 V) more and more as the input voltage increases.
Note that line regulation is different from PSRR (Power Supply Rejection Ratio) which is also a parameter that quantifies output voltage variation with respect to input, but this relation is considered in a spectrum of frequencies (it is an AC parameter rather than a steady-state one). Since the LDO takes the input from a buck converter, noise at the input side should be suppressed by a good PSRR up to the switching frequency of the converter. The frequency behavior of the PSRR is primarily dictated by the control loop.
Load regulation has a similar definition to line regulation, but it relates to

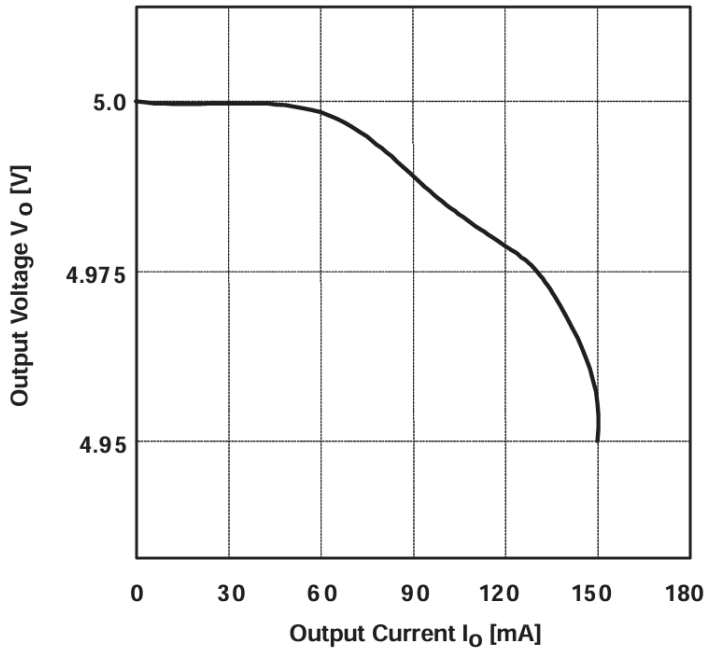


Figure 4.7: TPS76350 LDO regulator Output Voltage with respect to Output Current.

the variation in load current. It is the variation in the output voltage given a change in the load current (usually from the minimum load condition to the maximum) while the input voltage is kept constant.
Load regulation should be ideally as low as possible to not incur in significant output voltage variations when load conditions change.
A typical behavior for the output change due to load variations is depicted in Fig. 4.7 where it is shown that the output voltage deviates from the target as the load current increases.

4.2 Design of the LDO

The LDO design was modeled in the Virtuoso software using ideal blocks and a real pass transistor simulated for robustness at different temperatures. The targets are set as follows:

- $v_{in} = VDD_a = 3.3\ V$
- $v_{out} = VDD_d = 1.8\ V$
- Load current: 1 μA - 10 mA
- Line regulation < 1 %

- Load regulation < 1 %
- Reference voltage: $V_{REF} = 1.2\ V$

The first step of the design is to calculate the value of resistors that are used for the voltage divider. This divider has to scale the 1.8 V output down to the reference voltage which is set by a voltage source at 1.2 V to mimic a real bandgap reference which would be approximately equal to 1.2 V.
Referring to Fig. 4.5, R_1 must then be twice the value of R_2 so that the scale factor ($\frac{2}{3}$) is appropriate to set the voltage to be compared to the reference through the error amplifier.
This way the relative ratio between resistors R_1 and R_2 has been set, but the absolute value is also to be determined. While any resistance value is proper as long as the 1:2 ratio is respected, a low resistance value would mean high current consumption in the resistive branch (i.e. $R_1 = 2\,\Omega$ and $R_2 = 1\,\Omega$ result in a current of $\frac{v_{out}}{R_1+R_2} = 600\,\text{mA}$), conversely, high resistance would translate in a large area consumption to implement the resistors.
Given this reason, R_1 is set to 200 $k\Omega$ and R_2 to 100 $k\Omega$.
The error amplifier is modeled as an ideal voltage controlled voltage source (VCVS) in which the gain can be easily set.
A high gain in the amplifier will reduce the steady-state error in the output voltage and improve load and line regulation. There is a trade-off in terms of bandwidth though: the higher the gain of the amplifier is, the lower the expected bandwidth.
In this setup this is not an issue as the amplifier is an ideal VCVS and could achieve any gain at any bandwidth. To keep the design realistic and for a possible future implementation of a transistor level amplifier, the gain is set to a moderate value of 66 dB (2000).
The accuracy of the LDO mostly depends on the amplifier offset and the variation of the bandgap reference in temperature. In a real transistor level implementation, the overall offset of the amplifier should be minimized to achieve a low steady-state error at the output, while the bandgap reference should be accurately trimmed.
Given the ideal amplifier used, Bode diagrams that describe the stability of the regulator are not useful and will not be presented.
A PMOS device was chosen as the pass transistor to reduce complexity of the design. The stability issues related to the high output impedance node introduced by the PMOS will be countered in a real implementation by an external capacitor in the order of μF that would reduce the bandwidth of the system to ensure a stable loop.

4.2.1 Pass transistor sizing

The dimensions of the pass transistor determine the dropout voltage and the capability to carry the amount of current required by the load.

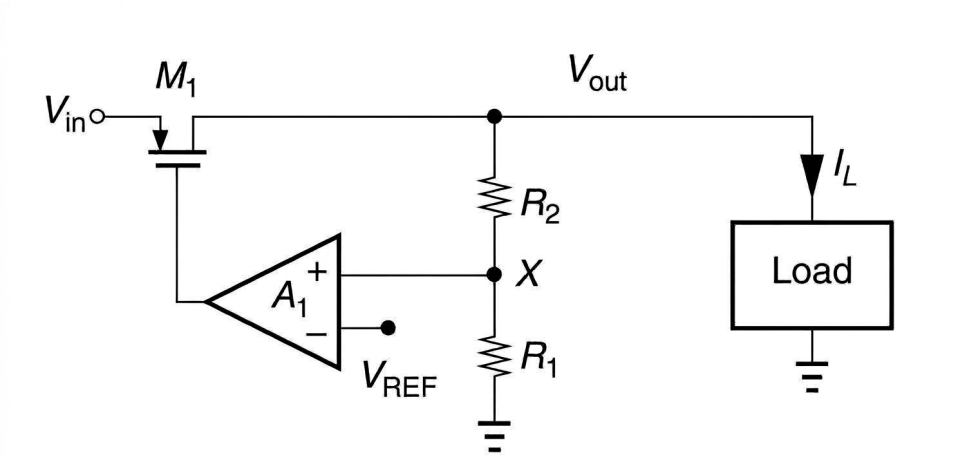


Figure 4.8: LDO using PMOS M_1 as the pass element.

In order to reduce the dropout and to carry a large current, a transistor with high aspect ratio ($\frac{W}{L}$) is needed; the drawback is that this transistor will occupy a large die area and will introduce a parasitic capacitance that will slow down the regulator.
Together with the error amplifier, the pass transistor also set the loop gain of the regulator. [14] Referring to Fig. 4.8, if the loop is broken at point X, the loop gain can be calculated as:

$$A_{LG} = A_1 g_{m1}[R_L||(R_1 + R2)]\frac{R_1}{R_1 + R_2} \tag{4.1}$$

Where R_L is the load resistance and the output resistance of the transistor is neglected.
Notice how node X (the scaled down output voltage) is connected to the non inverting input of the error amplifier while the reference is on the inverting terminal. If some variation in the circuit causes the output voltage to rise, node X will rise as well as it copies the behavior of the output through the resistor divider apart from a scaling factor; the error amplifier compares the now higher voltage on node X to the constant reference and amplifies the difference, raising its output which corresponds to the gate of the PMOS transistor M_1. The transistor now sees a lower source to gate voltage which causes a reduction in current flow, hence the reduction in the output voltage. Analogously, if the voltage were to drop below the target value, a complementary reaction would bring back up the output node.
It is clear that a variation on the output voltage is met by a reaction in the system that counters said variation to bring back the output to the target value. This is the effect of the negative feedback in the LDO and a larger loop gain would improve the effect of this reaction.

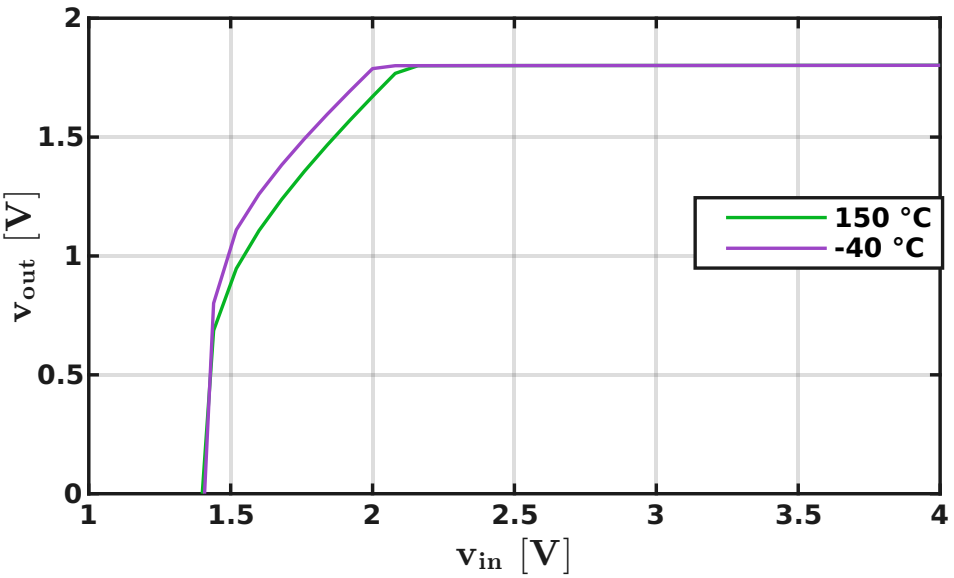


Figure 4.9: v_{out} vs. v_{in} simulation at $-40\,°C$ and $150\,°C$.

If the pass element had been an NMOS transistor, the input terminal connections to the amplifier would have been inverted to achieve negative feedback (Fig. 4.1).
5 V PMOS transistor pch_5_mac from TSMC 180 nm library was used as the pass element in the design.
The length was set to the minimum at L = 500 nm and simulations were conducted at a range of temperatures from $-40\,°C$ to $150\,°C$.
The input voltage is made to vary within a range of 1.4 V from the nominal value ($v_{in} \in [2.6\,V,\ 4\,V]$) and the regulator is expected to keep the output regulated at 1.8 V in this range.
To maintain the transistor in saturation over this range, a width of 450 μm was chosen.
The regulator was simulated, and the output voltage is plotted in Fig. 4.9, showing the results at the highest and lowest temperatures. A larger dropout voltage can be observed at $150\,°C$ compared to the minimum temperature. At $150\,°C$ the voltage starts to drop from the target at $v_{in} \approx 2.15\,V$ resulting in a dropout of 315 mV, while at the lowest temperature the value is just around 200 mV.
In the worst case, the output voltage deviates from 1 % of the nominal value at $v_{in} \approx 2.115\,V$, well below the 2.6 V minimum input assumed.
Results across the entire temperature range are depicted in Fig. 4.10, showing that line regulation is always under 1 %.
A transistor with smaller width could still achieve this result, but from simulation at lower W, the transistor can enter the triode region at high

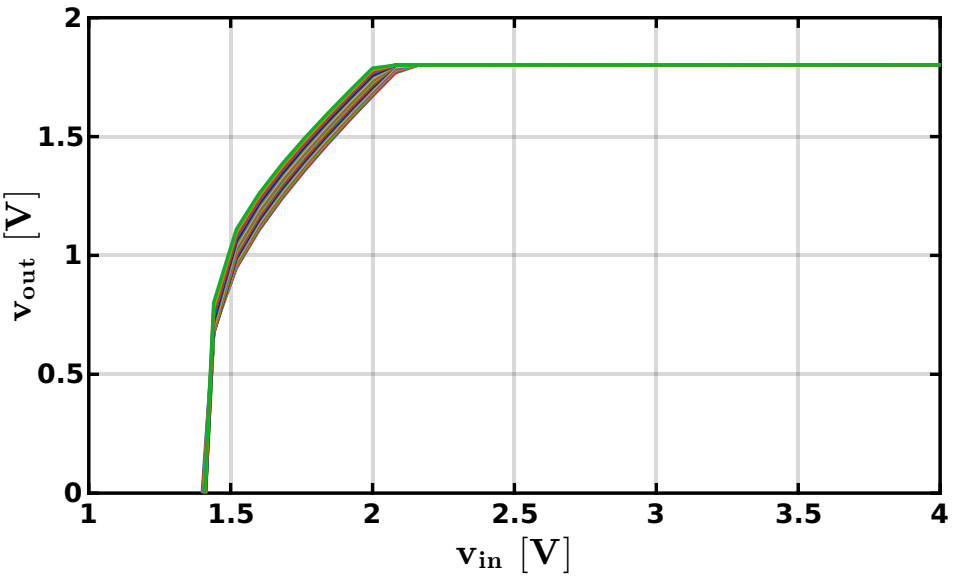


Figure 4.10: v_{out} vs. v_{in} simulation in the whole temperature range.

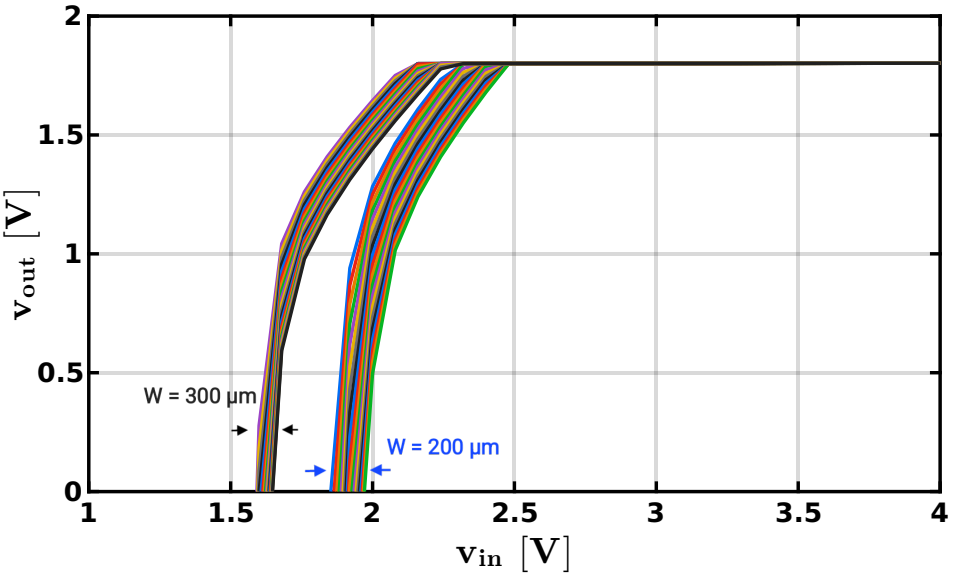


Figure 4.11: v_{out} vs. v_{in} simulations for transistor with $W = 200\,\mu\text{m}, 300\,\mu\text{m}$.

temperatures. For reference, another simulation was conducted at $W = 200\,\mu m,\ 300\,\mu m$ with results shown in Fig. 4.11.
Note how the dropout voltage reduces by increasing the transistor aspect ratio; this is to be expected as a larger transistor has a lower R_{on} that defines the border between regulation and the dropout region (Fig. 4.3).
For the load regulation, the output current was made to vary from 1 μA to 10 mA and the results are shown in Fig. 4.12 across the entire temperature range.
Load regulation is also kept under 1 % in all conditions.

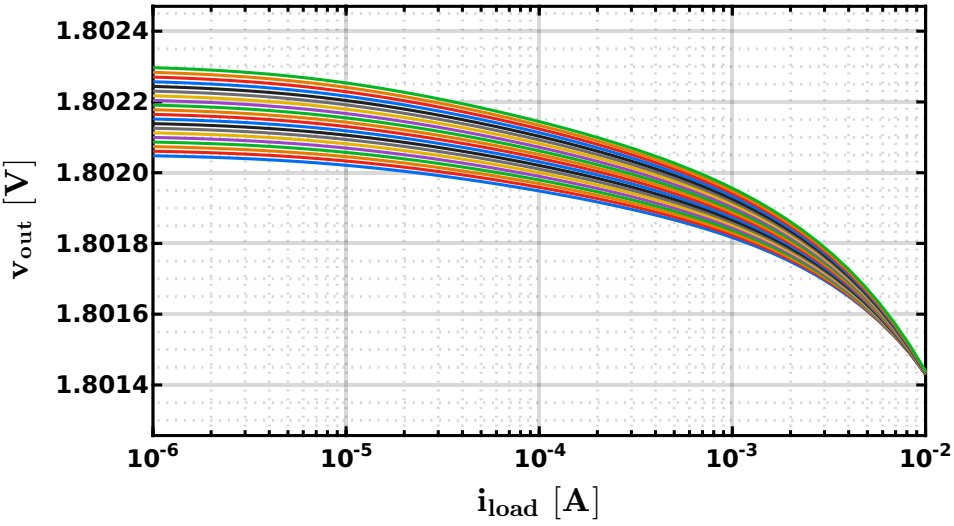


Figure 4.12: *vout* vs. i_{load} at different temperatures, with logarithmic X axis.

Conclusions

Power management solutions for driving an automotive matrix LED headlamp system were analyzed in order to select the best topology to supply the system and maximizing the efficiency.
To supply the analog section of the headlamp system, a buck converter implemented in TSMC BCD 180 nm technology was designed and simulated, achieving a 96 % peak efficiency.
For the power core supplying the LEDs, a 3-phase buck converter was implemented with discrete components to deliver the high current necessary for the LED matrix, also achieving 96 % peak efficiency, while an LDO was used to supply the digital core.
The analysis of these blocks was conducted first in SIMPLIS for a behavioral level verification and then in Cadence Virtuoso software for more accurate analysis.
The entire system can be driven using solely the 12 V vehicle battery as the power source.
This work was done using some ideal components alongside a transistor level implementation, so some improvements could be introduced in future revisions.
For the buck converters, gate driver circuits for the switches could be implemented as well as a control loop for stability.
The error amplifier for the LDO could be implemented incorporating techniques like adaptive or dynamic biasing to improve transient performance.

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