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UNIVERSITY OF PAVIA
FACULTY OF ENGINEERING
DEPARTMENT OF ELECTRICAL, COMPUTER AND BIOMEDICAL ENGINEERING

MASTER'S DEGREE IN ELECTRONIC ENGINEERING - MICROELECTRONICS

MASTER THESIS

Design and Area Optimization of an Isolation Switch for Synchronous Boost Converter in OLED Display Panel Applications

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A.Y. 2025/2026

Abstract

OLED technology has gained significant attention in recent years as an attractive display solution, combining performance advantages over LCD technology with a higher degree of commercial maturity than Micro-LED displays. In this context, Power Management Integrated Circuits (PMICs) play a key role in supplying OLED panels, where competitiveness depends not only on electrical performance but also on manufacturing cost. Since silicon area has a direct impact on integrated circuit cost, area-efficient design techniques are essential.

This thesis focuses on the area optimization of a synchronous boost converter used to generate the supply voltages required by OLED display panels. Particular attention is devoted to the output isolation switch, which enables the true shutdown function by ensuring complete output isolation when the converter is disabled. Because the isolation switch is usually implemented with large-area power devices to satisfy both voltage and conduction requirements, it represents one of the main area contributors within the converter.

For this reason, different isolation switch implementations are analyzed and compared, with particular emphasis on architectural choices affecting silicon area. The study focuses on optimization strategies based on pin-count reduction and on the selection of the MOSFET type used to implement the isolation switch. Through this analysis, the trade-offs associated with the different approaches are evaluated and the most area-efficient solutions are identified. Circuit-level simulations are used to assess the operation of the proposed architectures and to verify compliance with the converter functional requirements.

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Introduction

Displays have become a key component of modern electronic devices. They have established themselves as an integral part of daily life, being incorporated into numerous applications, ranging from automotive products to consumer electronics, including televisions, desktop monitors, smartphones, tablets and augmented reality devices.

A major milestone in the evolution of display technology was the introduction of liquid crystal displays (LCDs) in the early 1970s. These devices have gradually replaced bulky cathode ray tubes (CRTs) by offering a thinner, lighter and more energy-efficient solution, and since the 2000s they have become the dominant technology.

However, LCDs are non-emissive devices, and their reliance on a backlight unit has prompted research into alternative technologies capable of overcoming their inherent limitations. The most relevant developments have focused on self-emissive displays, in which each pixel generates its own light and can be independently switched on and off. These properties address the limited ability of LCDs to reproduce true blacks and achieve high contrast ratios, as well as other performance-related parameters that will be discussed in more detail later.

In recent years, among the most promising technologies in this category, organic light-emitting diodes (OLEDs) have attracted significant investment in advanced manufacturing processes and are already widely deployed as strong competitors to LCDs in TVs, smartphones and premium automotive cockpits, owing to their excellent dark-state performance, rich color reproduction and mechanical flexibility. However, this technology still faces challenges in terms of lifetime and durability, for which micro-light-emitting diodes (Micro-LEDs) have been proposed as a promising long-term successor. Despite their superior brightness, lifetime and environmental stability, Micro-LEDs face significant manufacturing challenges, such as mass transfer yield and defect repair, which inevitably pose cost-related barriers to large-scale production and currently favour OLEDs as the dominant technology in advanced display applications. The first chapter of this thesis provides a detailed overview of the main structural and performance differences between these technologies, with particular attention to key performance metrics used to assess their respective advantages and limitations.

The continuous advancement of display technologies has not only improved image quality but has also increased the complexity of the power management integrated circuits (PMICs) required for their operation. Consequently, the second chapter

reviews the state of the art of display power management solutions and presents a comprehensive analysis of one of the key PMIC building blocks, namely the DC-DC boost converter. Particular emphasis is placed on introducing the architectural modifications proposed in this work to achieve a more area-efficient implementation.

To assess the effectiveness of the proposed boost-converter architecture, the third chapter first introduces a behavioral and circuit-level model of the existing solution used as a reference throughout this study. The analyses presented in this chapter establish the basis for understanding the fundamental differences between the conventional and the proposed architectures, as well as their impact on overall system performance.

The design process begins in the fourth chapter with the selection and dimensioning of the isolation switch employed in the boost-converter topology. Since the silicon area occupied by this device represents a significant contribution to the overall implementation cost, particular attention is devoted to identifying a solution capable of achieving the desired area reduction while maintaining the required electrical performance.

The isolation switch requires dedicated driving circuitry to ensure its correct operation under all operating conditions. Since the proposed switch differs from the one adopted in the existing implementation in both device type and dimensions, a new driving architecture must be developed. For this reason, Chapter 5 presents an in-depth analysis of the currently adopted driver architecture and its operating principles, providing the foundation for the subsequent design activities.

Building upon the concepts introduced in the previous chapter, Chapter 6 describes the design process of the driver for the proposed isolation switch. A first architectural approach is presented and analyzed, highlighting its limitations and the challenges encountered during the design phase. These considerations ultimately motivate the development of the final driver architecture proposed in this thesis, which preserves the functionality of the original solution while addressing its main drawbacks.

Finally, Chapter 7 investigates the proposed isolation-switch driving architecture through a comprehensive analysis of its stability, robustness, and performance under process variations and mismatch conditions. The results demonstrate that the proposed modifications enable a significant reduction in silicon area while maintaining the required functionality and reliability of the boost-converter system.

Chapter 1

Display Technology Overview

This chapter provides a technical overview of the structural and performance differences among the LCD, OLED and Micro-LED display technologies. Additionally, particular emphasis is placed on examining the main building blocks of a typical power management integrated circuit (PMIC) required to supply and drive OLED display panels.

1.1 Operating principles and structures of LCD, OLED and Micro-LED pixels

The basic structure of a non-emissive liquid-crystal (LC) display panel (Figure 1.1) consists of an M x N passive array of pixels driven by an active thin-film transistor (TFT) matrix, which regulates the panel luminance by controlling the transmission of the backlight.

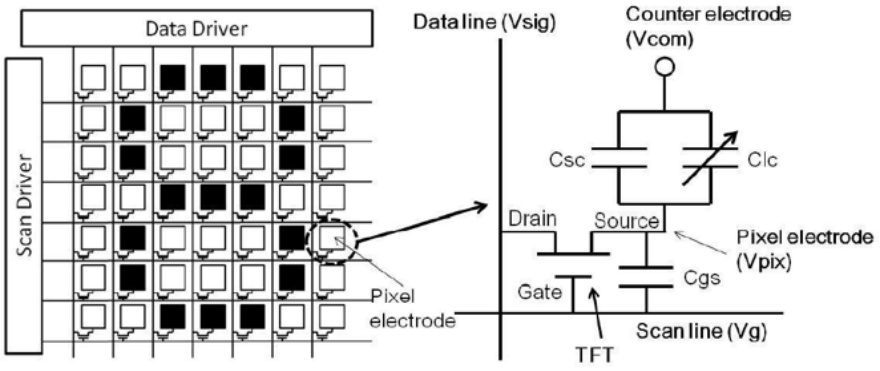


Figure 1.1: Equivalent circuit of an LCD panel with active matrix driving

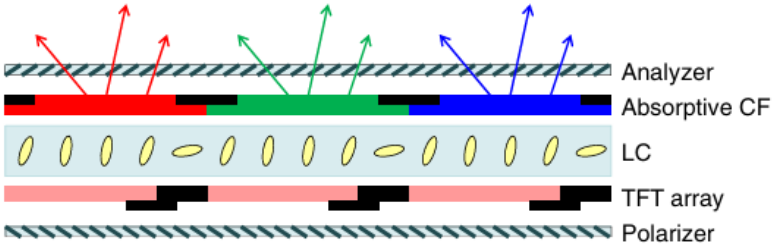


Figure 1.2: TFT RGB Liquid Crystal pixel [1]

Each pixel is composed of RGB subpixels (Figure 1.2), which are independently addressed by TFTs deposited on the glass substrate. Each liquid-crystal cell (Figure 1.3) is voltage-driven through its electrodes to control the orientation of the liquid-crystal molecules, thereby allowing more or less backlight to pass through. The full-colour range is then generated by combining the appropriate contributions from the individual RGB subpixels.

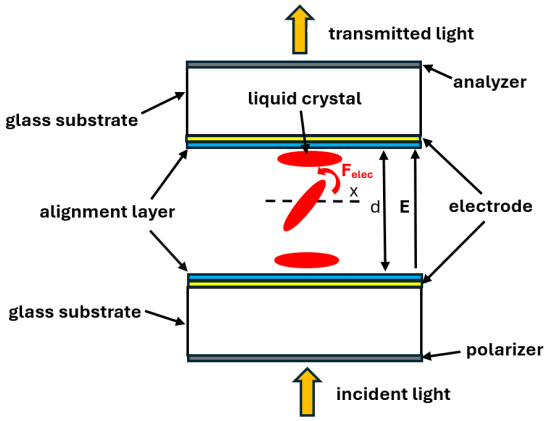


Figure 1.3: Liquid Crystal cell

Each row of the TFT matrix (Figure 1.1) is independently controlled by a scan line, which applies the gate voltage required to switch the corresponding TFTs on. When a TFT is turned on, the voltage carried by the data line, containing the image information for the pixel, is sampled and stored on the pixel node. The pixel capacitance is typically modelled as the sum of the LC cell capacitance, C_{lc}, and the additional storage capacitor, C_{sc}. As the scan signal turns off the TFT, the stored charge on C_{lc} and C_{sc} maintains the pixel voltage until the next frame update.

In emissive displays, such as Micro-LED and OLED technologies, a backlight is not required.
Each OLED pixel consists of three RGB light emitting diodes (LEDs) (Figure 1.4a) or, alternatively, three monochromatic LEDs combined with a colour conversion (CC) layer (Figure 1.4b). In the latter case (Figure 1.4b), blue LED chips act as the excitation source, illuminating a patterned color-conversion (CC) layer, typically composed of quantum dots or phosphors, which converts part of the incident blue light into red and green light. An absorptive colour filter (CF) array is subsequently deposited to suppress any unconverted blue light.[1]

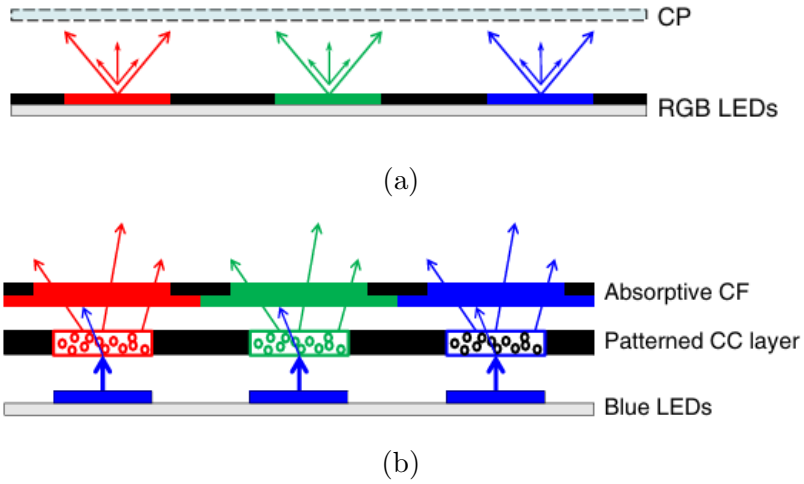
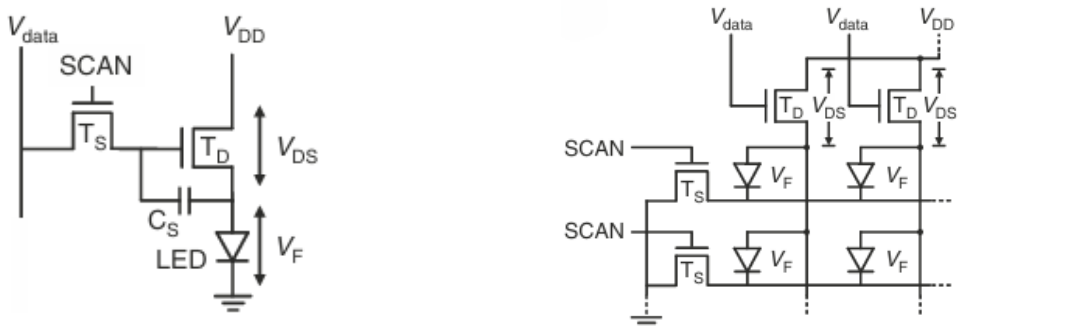


Figure 1.4: OLED pixel (a) with RGB LEDs (b) with CC layer [1]

In OLED display panels, a TFT matrix drives thin films of organic semiconductor materials (carbon-based molecules or polymers) that emit light directly when electrically excited. Unlike liquid crystal cells, OLED pixels are current-driven devices. Pulse amplitude modulation (PAM) is commonly used in emissive display driving schemes, for which both active matrix (AM) and passive matrix (PM) techniques can be adopted (Figure 1.5).



(a) Active Matrix driving scheme (b) Passive Matrix driving scheme

Figure 1.5: LED driving schematics [1]

For a display panel consisting of M x N pixels, the AM driving circuitry (Figure 1.5a) is arrayed in 3M columns and N rows. Three columns are required for each pixel, as every pixel is composed of RGB subpixels. In each row, the switching transistor T_S is sequentially activated to address the corresponding LED, while the driving transistor T_D regulates the current flowing through the LED, acting as a current source. With this driving scheme, T_S remains in conduction only for 1/N of the whole frame period (T_f), during which the data voltage (V_{data}) is loaded at the gate of T_D. For the remainder of the frame, T_S is switched off and a storage capacitance C_S holds the gate voltage, allowing T_D to remain in the on-state. As a result, in AM driving, the LED emits light throughout the entire frame period T_f.[1]

In contrast, PM driving (Figure 1.5b) does not employ a storage capacitor. To achieve the same effective luminance, each LED is driven only during its corresponding row-addressing interval equal to T_f/N. Consequently, the instant luminance in a PM display must be N times higher than that of the AM display to produce the same average luminance over a frame period.[1]

Each OLED pixel (Figure 1.6) consists of a stack comprising the hole-transporting layer (HTL), the emitting layer (EML) and the electron-transporting layer (ETL), positioned between the anode and cathode of the diode.[2] When current flows through the device and charges are injected, electron-hole recombination occurs within the organic emission layer, resulting in photon emission and thus light generation. Therefore, by controlling the injection current, the emitted light intensity (directly proportional to it) can be modulated.

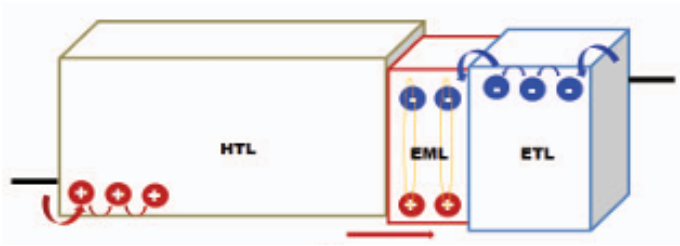


Figure 1.6: Schematic of charge transfer mechanism [2]

The structure of a Micro-LED is similar to that of a conventional LED (Figure 1.7).

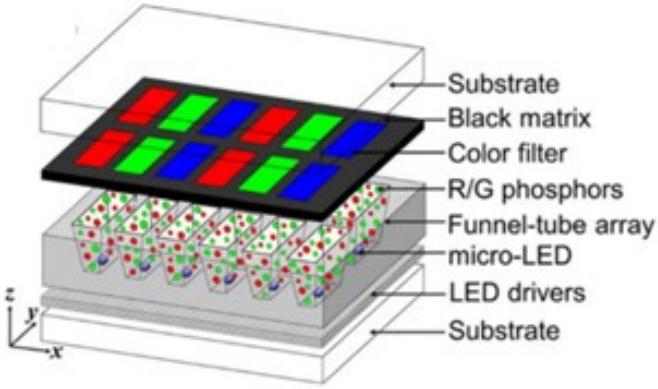


Figure 1.7: Micro-LED pixel layers [3]

Multiple InGan/GaN quanta wells (MQWs) are sandwiched between n-type and p-type GaN injection layers, forming the core region of the device. The emission wavelength can be tailored by adjusting the composition and thickness of the MQWs. In this case, when voltage is applied, electrons and holes are injected from the n-type and p-type layers, respectively, into the MQWs, where they recombine to emit photons. Although the operating principle is similar to that of traditional LED, the reduced device dimensions enable MicroLED technology to achieve faster response times and greater display resolution.[3]

In conclusion, LCD, OLED and Micro-LED technologies rely on fundamentally different operating principles. OLEDs have the simplest emissive structure, as light is generated directly through charge-carrier recombination within the organic emission layer. Micro-LEDs employ a MQW structure, where light is produced by driving electrons and holes to recombine. In contrast, LCDs require a backlight and rely on the modulation of liquid-crystal orientation by an applied electric field to control light transmission. As a result, LCDs exhibit the most complex structure, while OLED and Micro-LED displays benefit from simpler pixel structure and self-emissive operation.

1.2 Performance comparison

The comparison of different display technologies requires the introduction of appropriate performance metrics.

POWER CONSUMPTION

Power efficiency has become a critical requirement, especially in modern mobile consumer devices, where battery lifetime directly affects user experience and device usability. The overall power consumption of a display system depends not only on the display technology itself but also on the power required by the pixel driving circuitry. Therefore, evaluating display efficiency requires considering both the optical characteristics of the panel and the electrical behaviour of its driving architecture.

OLED displays exhibit a significant advantage in terms of power efficiency due to their self-emissive nature, because each pixel emits light independently and can be individually controlled. Therefore, as a result, OLED displays can completely turn off pixels when displaying black content, reducing power consumption considerably. In contrast, LCDs require a continuously operating backlight, making the power consumption less dependent on the displayed image. Consequently, power-saving strategies for LCDs mainly rely on backlight optimization.

Several studies conducted on mobile devices have compared the power consumption of LCD and OLED displays under different operating conditions, including black screen, dark mode (idle operation), white screen, and screen-off scenarios [4]. The results indicate that LCD displays exhibit an almost constant power consumption regardless of the displayed content, as the backlight remains active. OLED displays, on the other hand, show a strong dependence on image content. Under black screen, dark mode, normal mode and screen-off conditions, OLED panels consume significantly less power because many pixels are either partially active or completely turned off. Experimental measurements show that LCD displays may consume approximately from 200% to 260% more power than OLEDs in these scenarios (Figure 1.7)[4].

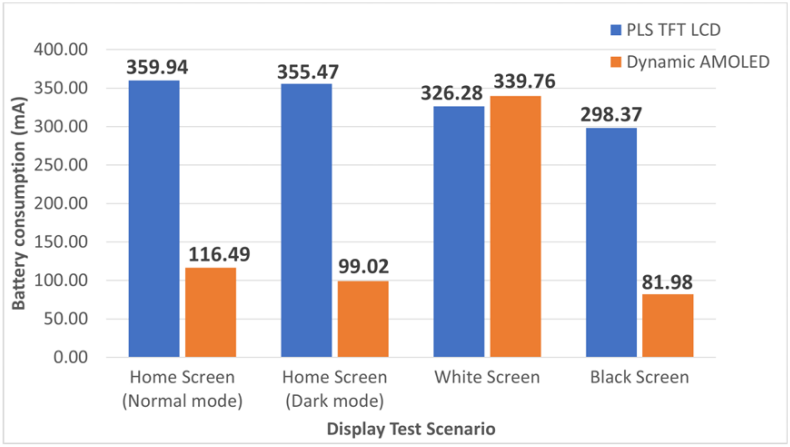


Figure 1.8: Battery consumption measurements over proposed scenarios [4]

However, under white screen conditions the power consumption of OLED and LCD displays becomes comparable, as both technologies require all subpixels to operate at high luminance levels. As a result, OLED displays may consume significantly more power than under dark-content conditions when displaying bright user interfaces or other high-luminance images [4].

The comparison can also be extended to the current consumption observed under different user interaction patterns, such as inactive states, swipe operations, and voice-input processing [5]. Experimental results demonstrate that OLED, and particularly AMOLED (Active Matrix OLED) technology, consistently outperforms LCDs across all tested scenarios. The most significant difference is observed during inactive operation, where LCDs continue to draw power to maintain display readiness even when the screen is not actively updating. Additional advantages are found during swipe-based interactions and voice-input processing. Overall, AMOLED displays reduce current consumption by approximately 30%-35% on average compared with LCD technology, with improvements reaching up to 40% in specific operating conditions [5].

Beyond the LCD-OLED comparison, it is also important to evaluate the energy efficiency of Micro-LED technology. Unlike LCDs, both OLED and Micro-LED displays are self-emissive technologies, therefore they both benefit from the ability to completely switch off pixels when displaying black content. As a result, the main difference in power consumption between OLED and Micro-LED displays does not come from their operating principle, but rather from the electrical efficiency of the light-emitting device itself. [1]

The static power consumption of both technologies is mainly determined by the power dissipated by the emissive device (P_{LED}) and by the TFT driving circuitry (P_{TFT}),as shown in Eq. 1.1 [1]

$$P_{static} = P_{LED} + P_{TFT} = (V_F + V_{DS})I \tag{1.1}$$

As represented in (Figure 1.5a), V_F is the forward voltage of the emissive device,

V_{DS} is the drain-source voltage across the driving TFT, and I is the driving current. In addition to the static component, a dynamic power contribution is generated by the storage capacitor C_s and by the parasitic capacitances of the data and scan lines. However, this contribution is generally much smaller than P_{static} and can therefore be neglected in the overall power budget [1].

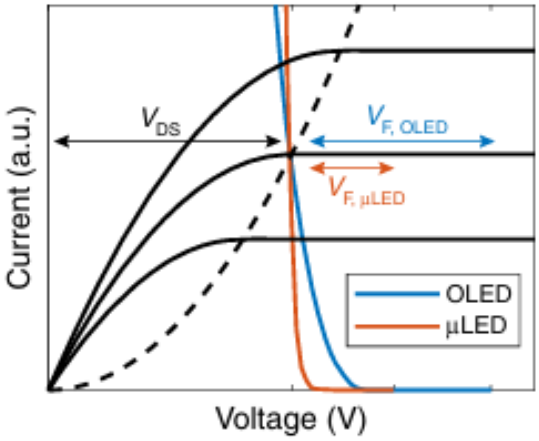


Figure 1.9: Operating spots of OLED displays and Micro-LED displays [1]

In Figure 1.9 the black curves represent the output $I - V_{DS}$ characteristics of the driving TFT at a given V_{GS}. The dashed black line denotes the border between the linear region (the left) and saturation region (the right). It then considers the current-voltage characteristics of OLED and MicroLED devices. The blue curve shows the OLED $I - V_F$ characteristics with the voltage axis flipped, while the red curve corresponds to MicroLED. The intersection between each TFT curve and the corresponding LED characteristic defines the operating point of the pixel.

Although both technologies exhibit a similar electrical behavior, the Micro-LED characteristic is shifted toward lower forward-voltage values. Consequently, for a given operating current, Micro-LED devices tend to require a lower V_F and therefore, since power consumption is directly proportional to voltage and current, the reduced V_F of MicroLEDs results in improved energy efficiency.[1]

Micro-LEDs are fabricated using inorganic semiconductor materials, characterized by high carrier mobility and efficient charge transport. In contrast, OLEDs rely on organic semiconductor materials, whose lower carrier mobility limits charge transport efficiency. Moreover, OLEDs exhibit a relatively small intrinsic charge density, leading to space-charge effects that further constrain carrier injection.[1] These limitations result in a higher threshold voltage and require OLED devices to operate at higher voltages to achieve the same luminance level.

As a result, the power consumption of OLED and Micro-LED displays is relatively similar when displaying dark content, since both technologies can switch off black pixels completely. However, under bright scenes and high-luminance operating conditions, the superior electrical efficiency of Micro-LED devices becomes more evident thanks to their lower forward voltage and higher carrier mobility.

HIGH DYNAMIC RANGE and BIT DEPTH

High dynamic range (HDR) is an important display standard that reflects a technology's ability to faithfully reproduce natural scenes by providing high contrast ratio, hence high peak luminance, a deep dark state, increased bit depth and a wide colour gamut.

The human eye is capable of perceiving an extremely wide dynamic range, spanning from very low luminance levels of 0.005 cd/m^2 to highlights exceeding 10,000 cd/m^2. Conventional standard dynamic range displays typically target a peak luminance of 100 cd/m^2. For Ultra HD Premium, displays are required to achieve wider luminance ranges, typically from 0.05 to 1000 cd/m^2 for LCDs and from 0.0005 to 540 cd/m^2 for OLED and Micro-LED displays.[2] By employing indium gallium-zinc-oxide (IGZO) TFTs and boosting the backlight luminance, it has been possible to manufacture a 8K LCD TV panels capable of exceeding 10,000 cd/m^2.[1] However, one of the main limitations of high-brightness LCDs is their relatively low optical efficiency, which leads to thermal management challenges. These issues can be partially mitigated through local dimming techniques.

On the other hand, OLED displays suffer from efficiency roll-off [6] and fast aging at high luminance levels [7], making them susceptible to image retention and burn-in, a phenomenon caused by the deterioration of the organic materials within the pixels under prolonged display of static content. Furthermore, issues with maintaining very high brightness levels over extended operating lifetimes limits their suitability for application requiring sustained high luminance output.

Micro-LED displays address these challenges and have emerged as a promising alternative. By employing inorganic semiconductor materials, such as GaN, instead of organic ones, this technology offers superior temperature resistance and is inherently immune to burn-in degradation. Furthermore, Micro-LEDs combine high energy efficiency at elevated luminance levels with excellent contrast and long operational lifetimes. As a result, Micro-LED technology is regarded as one of the most promising candidates for next-generation HDR displays due to its potential to outperform OLEDs in demanding high-brightness applications.

With the expansion of luminance range, 8 bits per colour is no longer sufficient to provide smooth colour transitions; therefore, modern HDR display systems require 12 bits per colour. In LCDs, achieving such a high effective bit depth is challenging due to the limited precision of the light modulation process and the relatively slow response time of the liquid crystal cells. By employing dual modulation units, which combine local dimming of the backlight with pixel-level transmission control, LCD displays can effectively share the luminance modulation burden between the two stages, enabling the realization of 12-bit HDR performance. [1]

On the other hand, in order to achieve the required bit depth, emissive displays demand extremely high accuracy in the current control managed in the pulse amplitude modulation (PAM) commonly used for driving OLEDs/Micro-LEDs (Figure 1.5), leading to high electronics cost. [1]

AMBIENT CONTRAST RATIO

Contrast ratio (CR) is a crucial performance metric for achieving bright colors, deeper blacks, and a wider color range, all of which contribute to high-quality image reproduction. It is generally defined as the ratio between the luminance of the brightest white state and that of the darkest black state. A higher contrast ratio results in more vivid images and improved visual perception.

LCD displays are inherently limited in contrast performance due to the presence of the backlight, which cannot be completely suppressed when displaying black content. This limitation originates from the depolarization effect of Liquid Crystals and the imperfect alignment of liquid crystal molecules, which leaves a residual light leakage even in the dark state [1]. As a result, conventional LCDs typically achieve contrast ratios ranging from approximately 1000:1 to 5000:1. One effective strategy to improve the contrast performance is local dimming, where different backlight zones are independently controlled. However, this approach increases both system complexity, therefore cost, and display thickness.

In contrast, self-emissive technologies such as OLED and Micro-LED inherently achieve much higher contrast ratios because they don't rely on a backlight. OLED displays typically exhibit contrast ratios on the order of 1,000,000:1, while Micro-LED displays can achieve values exceeding 1,000,000:1 [3]. The superior contrast performance of Micro-LEDs is primarily attributed to their ability to sustain significantly higher peak brightness levels while maintaining very low black-state luminance. In this case, pixel-level dimming can be exploited to independently adjust different areas of the display panel to different brightness levels and therefore further enhance perceived contrast [3].

While the conventional contrast ratio characterizes display performance under ideal dark conditions, real-world viewing environments are strongly influenced by ambient illumination. For this reason, the Ambient Contrast Ratio (ACR) is commonly used to evaluate the perceived contrast of a display in practical operating conditions. ACR accounts for the ambient light reflected by both the display surface and its internal structures, which contribute to the effective luminance perceived by the viewer in addition to the luminance generated by the displayed image.

In emissive displays, part of the generated light propagates both upward and downward. The downward-emitted light is typically utilized by placing a reflective electrode at the bottom of the LED chip [1]. Although this improves light extraction efficiency, internal electrodes also become potential sources of ambient light reflection. Consequently, both external surfaces and internal metallic structures contribute to the reflected ambient light that affects the ACR.

The ambient contrast ratio can be expressed as:

$$ACR = \frac{L_{\text{on}} + \frac{I_{\text{am}}}{\pi} R_L}{L_{\text{off}} + \frac{I_{\text{am}}}{\pi} R_L} \approx 1 + \frac{\pi L_{\text{on}}}{I_{\text{am}} R_L} \tag{1.2}$$

where L_{on} and L_{off} are the on-state and off-state luminance of the display, I_{am} the ambient illuminance, and R_L is the luminous reflectance of the display panel.

According to this relationship, a high ACR can be achieved by increasing L_{on} or reducing R_L. The display luminance can be enhanced by increasing the input power, whereas the panel reflectance mainly depends on the optical architecture and surface reflection characteristics.[1]

Different display technologies employ specific strategies to reduce reflectance. LCD panels typically use polarizing layers to suppress reflected light (Figure 1.2). OLED displays achieve low reflectance when using an anti-reflection coating, implemented either as a circular polarizer (CP) for RGB OLED architectures (Figure 1.4a), or as a colour filter (CF) in color-conversion OLEDs displays (Figure 1.4b).

Micro-LED displays, however, exhibit inherently higher reflectance because of the reflective metallic structures required by the device architecture. To improve the ACR, one possible approach is to remove the circular polarizer, which approximately doubles the optical efficiency and increases the L_{on}. However, this also increases the panel reflectance R_L. To compensate for this effect, the emitting area can be reduced, while the nonemittive area is covered with a black matrix to absorb the incident ambient light and reduce the overall panel reflectance (Figure 1.7).

Such an approach is less effective for OLED displays because a large chip size is beneficial for achieving a long device lifetime and high luminance. Moreover, even for inorganic semiconductor technologies such as Micro-LED, a trade-off exists between reflectance reduction and device efficiency. Although reducing the chip dimensions helps improve the ACR, it also increases the surface-to-volume ratio of the emitter, which can lead to higher surface-related losses.

Overall, OLED displays currently offer excellent CR and ACR performance thanks to their self-emissive operation and low-reflectance optical structures. Micro-LED displays provide similarly high contrast ratios while achieving substantially higher peak brightness, making them particularly attractive for high-ambient-light environments.

VIEWING ANGLE

Viewing angle is an important performance metric particularly in multi-viewer applications where image quality should remain consistent for observers positioned at different viewing directions. As the viewing angle increases, displays generally suffer from color distortion and an apparent reduction in brightness. In particular, the color shift, commonly quantified by the chromaticity variation Δu'Δv', increases significantly when the viewing angle exceeds approximately 60°.

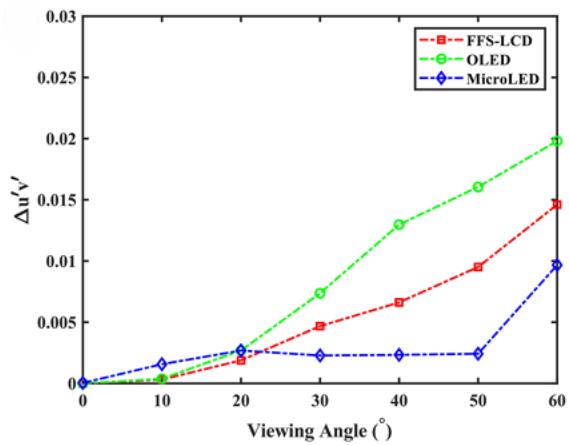


Figure 1.10: Colour shift Δu'Δv' of LCD, OLED and Micro-LED under different viewing angles [8]

LCD displays exhibit a strong dependence of image quality on viewing angle. As the observation angle increases, the contrast ratio gradually decreases due to the angular dependence of the liquid crystal modulation mechanism. Furthermore, the color shift of LCD panels reaches approximately Δu'Δv'=0.015, while the brightness decreases to about 40% of its maximum value at a viewing angle of 60°(Figure 1.10). To mitigate these effects, compensation layers are commonly introduced to correct angular color distortions, and although these optical compensation films improve performance at moderate viewing angles, they become increasingly ineffective at wider angles [3].

Unlike LCDs, self-emissive displays exhibit a contrast ratio that is not viewing-angle-dependent because each pixel can be individually controlled. However, angular color shift remains a significant challenge [8].

In OLED displays, viewing-angle performance is mainly affected by the micro-cavity effect. To improve optical efficiency, OLED devices employ small optical cavities, however, the emission spectrum shifts toward shorter wavelengths as the viewing angle increases due to the reduced effective cavity length. Additionally, RGB OLED subpixels exhibit unmatched radiation patterns, causing the relative contribution of each color component to vary with the viewing angle[8]. Consequently, OLED displays experience a color shift of approximately Δu'Δv'=0.02 at 60°, which is slightly higher than that observed in LCD panels(Figure 1.10)[3]. Moreover, the brightness decreases to approximately 50% of its peak value at a 60° angle. Despite these limitations, OLED displays generally provide superior overall viewing-angle performance compared with LCD technology because their contrast ratio remains essentially unchanged and the perceived image quality is better preserved at oblique angles.

Micro-LED displays offer further improvements in viewing-angle characteristics. In contrast to OLEDs, the cavity effect is relatively weak, and the central wavelengths of the RGB subpixels remain nearly unchanged as the viewing angle increases. Therefore, Micro-LED displays exhibit significantly lower spectral shifts and improved color stability.

Nevertheless, some limitations still exist. The extremely small chip dimensions lead to non-negligible sidewall emissions, while differences in the refractive indices of red, green, and blue LEDs produce unmatched RGB angular radiation patterns. These effects may introduce angular color variations at wide viewing angles (Figure 1.10) [8]. To compensate for these issues a specially designed black-matrix structure can be placed to help suppress unwanted sidewall emissions and improve color uniformity. However, this solution introduces a trade-off with light extraction efficiency, since part of the emitted light may be blocked or absorbed by the black matrix.

Despite these challenges, MicroLED technology exhibits excellent brightness retention at large viewing angles. Compared with LCD and OLED displays, the brightness of a MicroLED panel at 60° remains approximately 70% of its maximum value, demonstrating significantly better angular luminance performance [3].

1.3 Manufacturing and cost considerations

MANUFACTURING PROCESSES

Another factor that differentiates display technologies and influences their commercial viability is the precision level required by their manufacturing processes.

The manufacturing process of LCD is relatively complex. The liquid crystal material is injected between a transparent conductive layer and an orientation layer coated to adjust by friction the arrangement of the LC molecules. High process uniformity and precision are required throughout these fabrication steps to ensure consistent performance across the entire panel [3].

The manufacturing of Micro-LED is even more challenging, since high precision is required during the epitaxial growth of the InGaN/GaN multi-quantum wells. Furthermore, large-scale display fabrication requires the transfer, assembly, and testing of millions of individual Micro-LED chips, making the manufacturing process particularly time-consuming and costly [3].

In contrast, the manufacturing process of OLED is comparatively simpler. The only aspect warranting particular attention is the packaging, designed to protect the organic layers from degradation caused by moisture and oxygen exposure. Moreover, OLED materials can be processed at relatively low temperatures and are compatible with high-throughput fabrication techniques, such as roll-to-roll printing. These advantages enable large-scale production at reduced manufacturing costs, making OLED technology well suited for mass-market applications [3].

LIFETIME AND PANEL FLEXIBILITY

LCD and Micro-LED displays employ inorganic materials in their backlight and light-emitting sources respectively. As a result, their operational lifetime can exceed 50000 h [8].

In the case of OLED displays, an encapsulation layer is needed to protect the organic materials from environmental degradation due to their sensitivity to moisture, oxygen, heat and DC current. This technology is also affected by image retention (burn-in), as well as differential aging among the three primary colors. In particular, red and green OLEDs can achieve a lifetime of 80000 h, whereas blue phosphorescent OLEDs exhibit 20 times shorter operational lifetimes. Nevertheless, continuous research into novel materials and device architectures is expected to further improve the reliability and longevity of OLED technology [8].

Despite these limitations, one of the key structural advantages of OLED technology is the exceptional mechanical flexibility of the organic materials, which makes it particularly attractive for applications such as vehicle displays, smartphones and even TVs. The introduction of ultrathin substrates, polarizers and electrodes has further enhanced this capability, enabling the development of flexible and foldable displays. In contrast, the backlight unit required by LCDs inherently limits their flexibility, although flexible LCD implementations have been demonstrated requiring bendable backlight structures based on organic materials [8].

COST

Cost is often a decisive factor in the commercial success of a display technology, as it directly influences product affordability and market adoption. Due to decades of development and large-scale manufacturing, LCDs remain the most affordable display solution. Mature manufacturing processes, high production yields, and a well-established supply chain have significantly reduced production costs. However, performance-enhancing technologies such as Mini-LED backlighting significantly increase manufacturing complexity, and a mini-LED LCD panel (mLCD) can cost up to five times more than an OLED panel of the same size and resolution [8].

Similarly, after more than 30 years of research, development and commercialization, OLED technology can now be considered a mature display platform. Continuous improvements in manufacturing yield, materials, and fabrication processes have progressively reduced production costs, making OLED displays strong candidates to replace LCDs in many applications due to their superior performance [8].

In contrast, Micro-LED technology is still in an early stage of industrial development and remains significantly more expensive than both LCD and OLED displays. Although reducing chip size increases the number of devices per wafer, it lowers the mass-transfer yield, leading to higher repair costs and longer production times. Furthermore, smaller chips generate more material waste during the singulation process, simultaneously introducing additional manufacturing challenges that negatively affect production efficiency and cost [8].

Overall, LCD technology remains the most cost-effective display solution due to its highly mature manufacturing ecosystem. OLED technology has reached a comparable level of maturity and continues to benefit from decreasing production costs while offering superior display performance. Micro-LED technology, despite its outstanding optical and electrical characteristics, still faces significant manufacturing challenges that result in substantially higher production costs; therefore, it represents a next-generation solution once manufacturing hurdles are overcome, but not a direct short-term competitor.

The key advantages and limitations of LCD, OLED, and MicroLED technologies are summarized in Table 1.1, providing an overall comparison of their performance and cost characteristics.

Characteristic	**LCD**	**OLED**	**Micro-LED**
Power Consumption	Higher	Low for dark content	Low
Dark Content Display	Limited	Very good	Very good
Brightness	High	Medium	Highest
Contrast	Medium	High	High
Lifetime	Good	Medium	Good
Environmental Stability	Good	Medium	Good
Maturity	High	Medium	Low
Cost	Low	Medium	High

Table 1.1: Display Technology Comparison: LCD, OLED and Micro-LED

1.4 Requirements in automotive applications

VEHICLE MOUNT DISPLAY (VMD)

In the industrial sector, LCDs are currently the most widely used technology for vehicle mount displays (VMDs) due to their low cost, long lifetime, high stability, especially over a wide temperature range, and suitability for mass production. However, LCDs present some limitations that are becoming increasingly relevant for VMD applications. Their relatively low contrast ratio can make the display difficult to read in bright environments and, in critical situations, may even increase the risk of accidents. In addition, the limited viewing angle and relatively slow response time of LCDs can negatively affect the readability and viewing experience. These limitations are encouraging the market to investigate alternative display technologies [3].

Micro-LED displays offer several advantages that make them particularly attractive for VMD applications, including high brightness, high contrast ratio, and low power consumption. The latter is especially important in vehicle applications where the available battery capacity may be strictly limited. Moreover, the use of inorganic materials provides Micro-LEDs with a long lifetime and high temperature resistance [1]. However, the complexity of the Micro-LED manufacturing process, together with its extremely high cost and the currently low production yield, significantly limits its ability to penetrate the large-scale market. Therefore, despite their excellent performance, further improvements in manufacturing processes and cost reduction are required for Micro-LEDs to become a widespread alternative to LCDs [3].

OLED displays have also emerged as a promising alternative for vehicle-mounted applications due to their ability to perform well in bright environments, mainly thanks to their high contrast ratio, as well as their improved image fluency and viewing experience. However, the main limitation of OLED technology is related to the properties of its organic materials. When exposed to high temperatures, these materials are susceptible to accelerated aging, colour shift, and a shorter lifetime. This represents an important issue for vehicle applications, since the temperature inside a vehicle can reach temperatures of up to 90 °C during summer. In addition, the risk of burn-in occurring after long-term use may lead to persistent residual images on the display [3].

Nevertheless, with continued progress in materials research, manufacturing technology, and cost reduction, OLED technology has the potential to expand further into the vehicle display market and increasingly compete with LCDs as a mainstream display solution.

POWER MANAGEMENT BLOCKS FOR OLED PANEL SYSTEMS

As discussed in the previous section, OLED technology represents an attractive solution for automotive display applications. However, the operation of an OLED panel requires multiple voltage domains and carefully controlled biasing conditions, making the power management architecture a fundamental element of the overall

display system.

Power management has become a key aspect of modern electronics, as it directly affects the overall dimensions and cost of a system. The efficiency of the power conversion chain determines the amount of power losses that must be handled, impacting thermal dissipation requirements and the sizing of passive components. As a result, higher efficiency generally translates into smaller and lower-cost solutions. For this reason, the power management architecture plays a crucial role in automotive OLED display systems, where several voltage rails are required to properly power and drive the display panel.

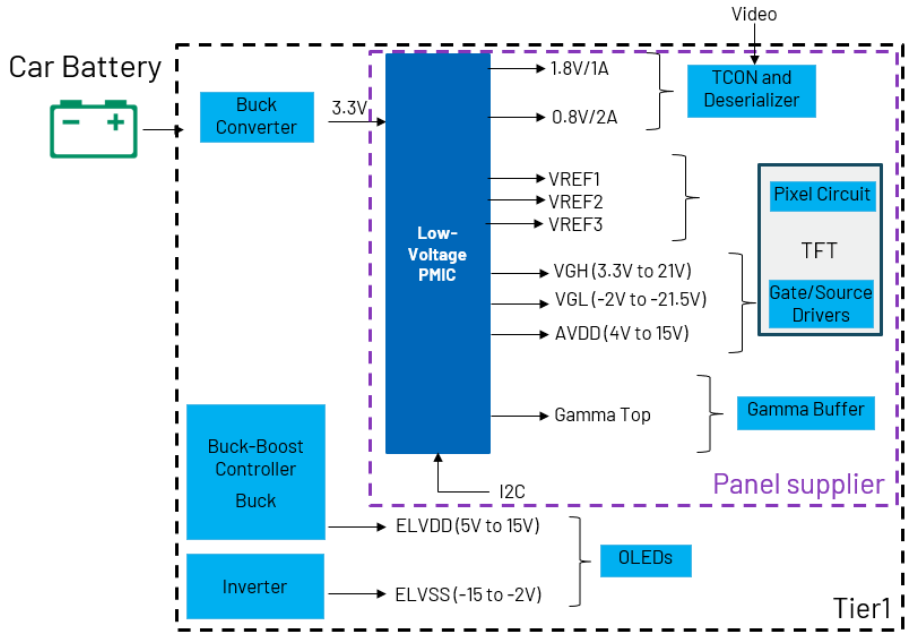


Figure 1.11: Simplified power management architecture of a typical automotive OLED display system

(Figure 1.11) shows a simplified block diagram of a typical power management solution for an automotive OLED panel. The display system is powered from the vehicle battery through a front-end DC-DC buck converter stage that generates a regulated low-voltage rail, typically 3.3 V, which serves as input to a dedicated low-voltage PMIC (Power Management Integrated Circuit). The PMIC then generates the various voltage levels required by the display and the pixel-driving circuitry. In parallel, additional power converters generate the positive and negative supply voltages (ELVDD and ELVSS) needed to directly bias the OLED emissive devices.

The main outputs provided by the PMIC are the dedicated supply rails for the TCON (Timing Controller) and deserializer, which are responsible for receiving the video data stream and converting it into the timing and control signals required by the display panel. Such outputs include low-voltage rails of 1.8V and 0.8V, compatible with the I/O interfaces and the digital circuitry.

Another group of outputs consists of the reference voltages (VREF1, VREF2,

and VREF3) used by the pixel-driving circuitry. The reference voltages establish accurate bias conditions for the TFTs to regulate the current flowing in the OLED, enabling uniform brightness and compensating for process, voltage, and temperature variations across the panel.

The PMIC also provides the input voltages for the gamma buffer, that implements the desired gamma correction curve for ensuring that the relationship between input pixel values and displayed luminance matches the characteristics of human vision, resulting in accurate grayscale reproduction and image quality.

Finally, for the TFT pixel driving circuitry, the PMIC generates three key supply rails: AVDD, VGH, and VGL. The AVDD rail is the main analog supply of the panel and typically ranges from a few volts up to approximately 15 V depending on panel characteristics. It powers the analog circuitry responsible for pixel driving and data conversion. VGH and VGL are the positive and negative gate-driving supplies used by the TFT gate drivers. VGH is a high positive supply, typically ranging from 3.3 V to 21 V, used to turn the TFTs on, while VGL is a negative supply, typically between -2 V and -21.5 V, used to ensure complete turn-off of the TFTs.

Overall, the power management subsystem plays a crucial role in OLED panel systems by generating and regulating the multiple voltage domains required for digital processing, TFT operation, and OLED emission, while meeting the stringent reliability and efficiency requirements of automotive applications.

Chapter 2

Synchronous DC-DC Boost Converter

As discussed in the previous chapter (chap.1.4), OLED panel systems require dedicated high-voltage supplies, such as AVDD and VGH, to properly power the pixel circuitry and TFT gate drivers. These voltages are typically generated by DC-DC boost converters starting from the low-voltage supply available within the power management system. Since the focus of this thesis is the analysis and enhancement of a synchronous boost converter architecture for OLED display applications, this chapter first reviews the operating principles of boost converters and presents representative state-of-the-art solutions. Subsequently, the limitations of existing implementations are discussed, introducing the objectives and motivations of the proposed work.

2.1 Basic structure and working principle

Power converters can be broadly classified into two main categories: linear converters and switching converters. In linear converters, power is transferred continuously from the source to the load through a regulating element operating in its linear active region. However, these converters cannot perform voltage step-up conversion.

More specifically, DC-DC converters are designed to convert an input DC voltage into a regulated DC output voltage. Depending on the conversion ratio, they can be classified as buck converters, which produce an output voltage lower than the input voltage, or boost converters, which generate an output voltage higher than the input voltage.

In contrast to linear regulators, switching converters transfer energy discretely by periodically turning power switches ON and OFF. This operating principle enables efficient voltage conversion while supporting both step-down (buck) and step-up (boost) functions.

The main advantage of switching-mode operation lies in the behaviour of the power transistor, which alternates between the ON and OFF states. In the OFF

state, only a small leakage current flows through the device, while in the ON state the voltage drop across the transistor is ideally very small. As a result, the power dissipated by the switching elements is minimized, enabling very high conversion efficiencies.

Energy storage devices play a fundamental role in switching converters. In particular, inductors and capacitors can ideally store and transfer energy without dissipating power, making them key elements of efficient power conversion. Switching converters can therefore be classified as inductor-based converters or inductorless switched-capacitor converters, depending on the energy transfer mechanism employed.

The focus of this thesis is on an inductor-based switching DC-DC boost converter intended to generate the high-voltage rails required in OLED panel systems, converting input voltages of a few volts into output voltages ranging from approximately 5 V to 21 V. Since the converter investigated in this work relies on magnetic energy storage, the following discussion focuses on the operating principles of inductor-based boost converter architectures.

IDEAL BOOST CONVERTER

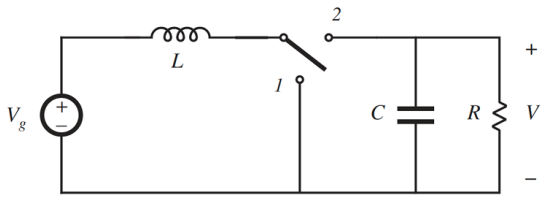


Figure 2.1: Ideal DC-DC Boost converter configuration

Figure 2.1 shows the ideal boost converter. Its operation can be divided into two switching phases. Therefore, the relationship between the output voltage and the input voltage can be derived by analyzing the inductor voltage waveform during each phase of operation.

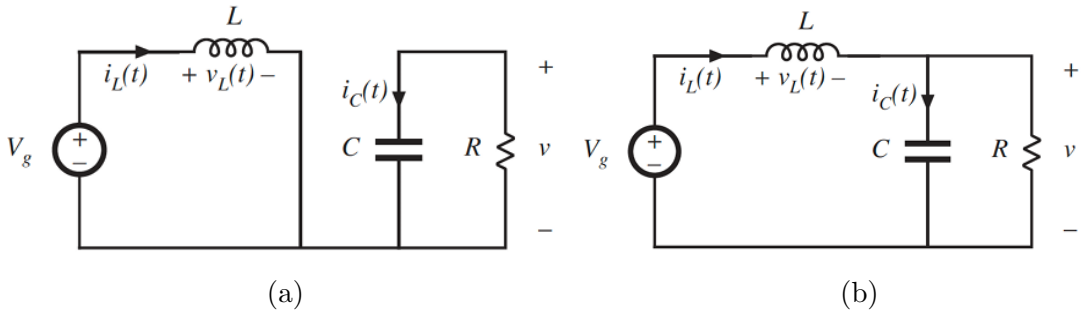


Figure 2.2: (a)Ideal boost converter with switch in position 1, (b)Ideal boost converter with switch in position 2

During the first phase (Figure 2.2a), switch is in position 1, allowing the input

source to charge the inductor and store energy in its magnetic field. The inductor voltage and capacitor current are

$$v_L = V_g \tag{2.1a}$$

$$i_C = -\frac{v}{R} \tag{2.1b}$$

Assuming a small output-voltage ripple, the instantaneous output voltage can be approximated by its average value

$$v(t) \approx V, \tag{2.2}$$

which leads to

$$i_C = -\frac{V}{R} \tag{2.3}$$

During the second phase (Figure 2.2b), the energy previously stored in the inductor is transferred to the output, supplying both the load and the output capacitor. In this interval, the inductor voltage and capacitor current become

$$v_L = V_g - v \tag{2.4a}$$

$$i_C = i_L - \frac{v}{R} \tag{2.4b}$$

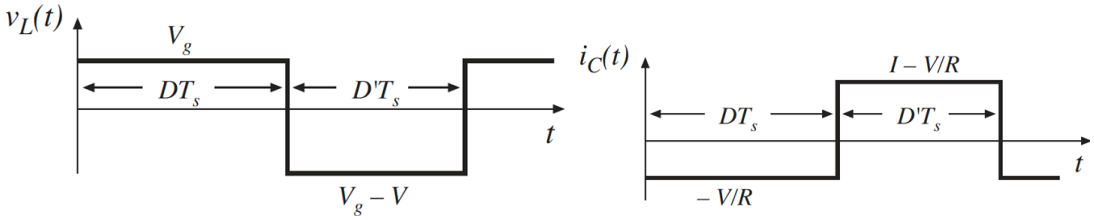
Applying the small-ripple approximation (eq. 2.2) to both the inductor current and the output voltage yields

$$v_L = V_g - V \tag{2.5a}$$

$$i_C = I - \frac{V}{R} \tag{2.5b}$$

where I denotes the average inductor current.

Based on these expressions, the waveforms of the inductor voltage and capacitor current can be sketched. Let T_s denote the switching period and D the duty cycle, with $D' = 1–D$. The interval DT_s corresponds to the transition instant between the first and the second operating phase.



(a) Inductor voltage waveform (b) Capacitor current waveform

Figure 2.3

CONVERSION RATIO

The conversion ratio of the ideal boost converter can be derived by applying the principle of *inductor volt-second balance*. According to this principle, under steady-state conditions, the average voltage across the inductor over one switching period must be zero.

$$0 = \frac{1}{T_s}\int_0^{T_s} v_L(t)\,dt = \langle v_L \rangle \tag{2.6}$$

Applying eq. 2.6 over one switching period

$$0 = \frac{1}{T_s}\left[\int_0^{DT_s} V_g\,dt + \int_{DT_s}^{T_s} (V_g - V)\,dt\right] \tag{2.7}$$

We then find

$$0 = DV_g + D'(V_g - V) \tag{2.8}$$

Rearranging,

$$V = \frac{V_g}{D'} = \frac{V_g}{1-D} \tag{2.9}$$

And therefore the conversion ratio M(D) of the boost converter is equal to:

$$M(D) = \frac{V}{V_g} = \frac{1}{1-D} \tag{2.10}$$

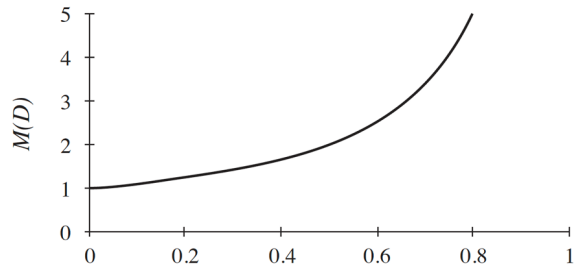


Figure 2.4: Conversion ratio as a function of the duty cycle

Hence, the output voltage is always greater than or equal to the input voltage and increases as the duty cycle approaches unity.

INDUCTOR CURRENT WAVEFORM

Having already determined the inductor voltage waveform $v_L(t)$, the inductor current waveform can be directly derived using the fundamental inductor relation

$$v_L(t) = L\frac{di_L(t)}{dt} \tag{2.11}$$

From eq. 2.11, the slope of the inductor current is proportional to the voltage applied across the inductor. Referring to Fig. 2.3a, during Phase 1 ($0 < t < DT_s$),

the inductor is connected to the input source. In this interval, the inductor voltage is equal to V_g, yielding

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g}{L} \tag{2.12}$$

Whereas during Phase 2 ($DT_s < t < T_s$), the energy stored in the inductor is transferred to the output stage. Since the inductor voltage becomes $V_g - V$, the current slope is

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g - V}{L} \tag{2.13}$$

The resulting inductor current waveform (Fig. 2.5) is therefore triangular with an average value I and a peak-to-peak ripple amplitude equal to $2\Delta i_L$. It exhibits a positive slope in the interval DT_s and, since $V > V_g$, a negative slope during the interval $D'T_s$.

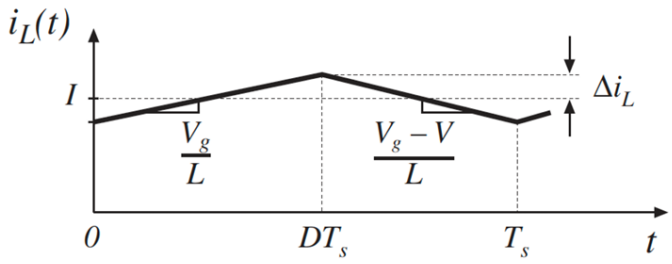


Figure 2.5: Inductor current waveform

From fig. 2.5 it can be observed that the ripple magnitude is equal to the current slope multiplied by the duration of the corresponding subinterval. Therefore,

$$2\Delta i_L = \frac{V_g}{L} DT_s \tag{2.14}$$

Solving for Δi_L yields

$$\Delta i_L = \frac{V_g}{2L} DT_s \tag{2.15}$$

Equation 2.15 shows that the inductor current ripple increases with the duty cycle and switching period, while it decreases for larger values of inductance.

INDUCTOR CURRENT DC COMPONENT

The DC component of the inductor current can be derived by applying the principle of capacitor charge balance. According to this principle, the average value, or DC component, of the capacitor current must be zero under steady-state conditions:

$$0 = \frac{1}{T_s} \int_0^{T_s} i_C(t)\, dt = \langle i_C \rangle \tag{2.16}$$

During the first subinterval (switch position 1), the inductor is energized while the capacitor alone supplies the load, causing a partial discharge of the capacitor. During the second subinterval (switch position 2), the inductor current delivers

power to the load and simultaneously recharges the capacitor. The net variation of the capacitor charge over one switching period can therefore be obtained by integrating the capacitor current waveform:

$$\int_0^{T_s} i_C(t)\,dt = \left(-\frac{V}{R}\right) DT_s + \left(I - \frac{V}{R}\right) D'T_s \tag{2.17}$$

Substituting eq. 2.17 into eq. 2.16 and collecting terms yields

$$-\frac{V}{R}(D + D') + ID' = 0 \tag{2.18}$$

With $D + D' = 1$, and substituting V derived in eq 2.9 the DC inductor current becomes

$$I = \frac{V_g}{RD'^2}. \tag{2.19}$$

The inductor current, which corresponds to the DC input current of the boost converter, is larger than the load current and increases as D approaches 1.

OUTPUT VOLTAGE WAVEFORM

Knowing the capacitor current waveform, it is possible to derive the output voltage waveform, since the capacitor voltage coincides with the converter output voltage ($v_C(t) = v(t)$). Referring to Fig. 2.3b, the capacitor voltage slope can be obtained from the capacitor constitutive relation

$$i_C(t) = C\frac{dv_C(t)}{dt} \tag{2.20}$$

Therefore, during the first switching subinterval

$$\frac{dv_C(t)}{dt} = \frac{i_C(t)}{C} = -\frac{V}{RC} \tag{2.21}$$

During the second switching subinterval

$$\frac{dv_C(t)}{dt} = \frac{i_C(t)}{C} = \frac{I}{C} - \frac{V}{RC} \tag{2.22}$$

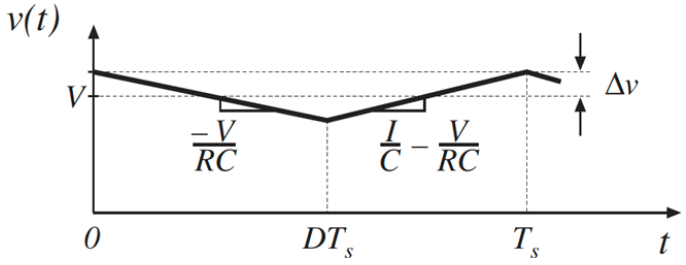


Figure 2.6: Output voltage waveform

Using these slopes, the output voltage waveform shown in Fig. 2.6 can be constructed. The waveform exhibits a small triangular ripple around its average value

V. The voltage variation during the first subinterval is equal to the corresponding slope multiplied by the interval duration DT_s:

$$-2\Delta v = -\frac{V}{RC}DT_s \tag{2.23}$$

Solving for the output voltage ripple yields

$$\Delta v = \frac{V}{2RC}DT_s \tag{2.24}$$

Equation 2.24 shows that the output voltage ripple increases with the duty cycle and switching period, while it decreases for larger values of capacitance and load resistance.

BOOST CONVERTER IMPLEMENTATIONS

The power switch implementation of a boost converter can be realized using different circuit topologies, the most common being the non-synchronous and synchronous boost converter configurations.

- **Non-synchronous boost converter**

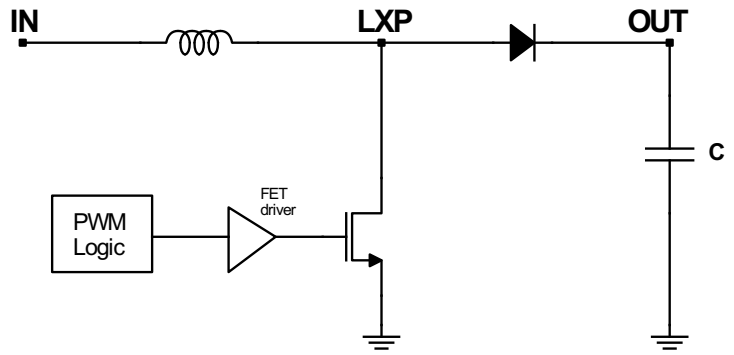


Figure 2.7: Non-synchronous boost converter scheme

In the non-synchronous boost converter, the switching network is implemented using an active switch, typically a MOSFET, and a diode, as shown in Fig. 2.7. The Pulse Width Modulation (PWM) control logic drives the low-side switch, periodically turning it on and off to establish the two operating phases described in the previous section (chap. 2.1). During the interval in which the MOSFET is turned on, the diode is reverse biased and the inductor stores energy from the input source. When the MOSFET is turned off, the inductor current is forced through the diode toward the output, transferring the stored energy to both the load and the output capacitor.

The main advantage of this topology is its simplicity, requiring only a single actively controlled switch. However, the diode introduces an unavoidable forward voltage drop, resulting in additional conduction losses and reduced conversion efficiency, particularly in low-voltage applications where the diode

voltage represents a significant fraction of the output voltage.

- **Synchronous boost converter**

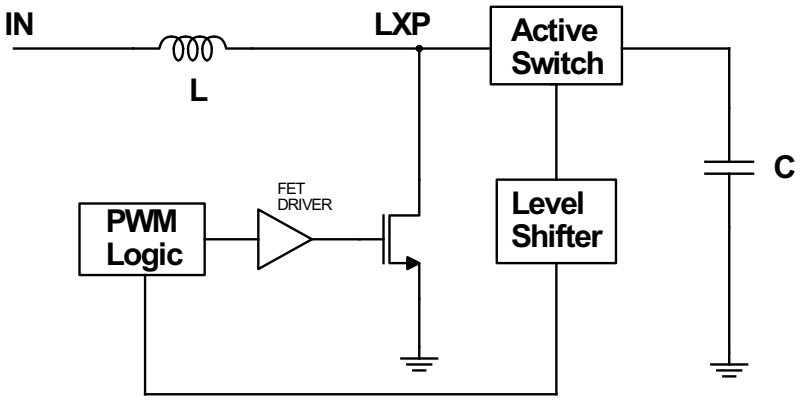


Figure 2.8: Synchronous boost converter scheme

In this topology, the switching function is implemented using two active switches: a low-side switch driven directly by the PWM control logic and a high-side switch driven by a level-shifted PWM signal referenced to the switching node voltage.

Although the additional circuitry required to drive the high-side device increases the overall design complexity, the synchronous architecture is widely adopted because of its superior efficiency. In particular, replacing the rectifying diode with an actively controlled switch significantly reduces conduction losses, leading to improved thermal performance and higher conversion efficiency.
Furthermore, unlike a passive diode, the active does not inherently block reverse current. As a result, a temporary reverse current path can be established during switching transitions, helping to reduce output voltage ringing and noise.

Another important characteristic to consider is that the output is not completely isolated from the input. In the non-synchronous topology, the rectifying diode provides a direct current path from the input to the output. Similarly, in the synchronous implementation, the body diode of the high-side MOSFET creates an equivalent conduction path. As a result, the output capacitor is charged even when the switching action is disabled. Consequently, the output voltage naturally rises to approximately $V_{OUT} \approx V_{IN} - V_D$ where V_D is the forward voltage drop of the conducting diode. Therefore, residual output voltage is always present whenever an input voltage is applied.

A key requirement in OLED panel power supplies is to achieve a true shutdown condition, in which the output can be completely discharged and maintained at $0V$ when the converter is disabled. To meet this requirement, an additional isolation switch may be placed in series with the output.

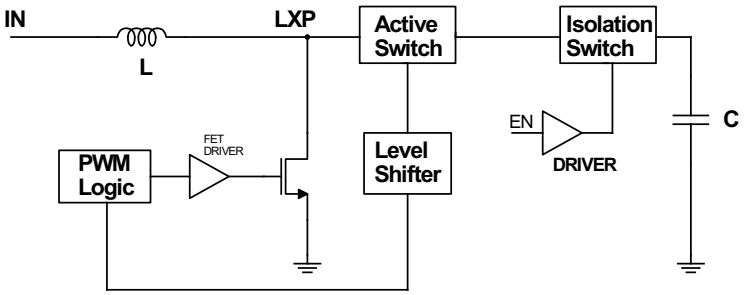


Figure 2.9: Scheme of a synchronous boost converter with Isolation Switch

The isolation switch is typically implemented using a MOSFET whose body diode is oriented opposite to that of the high-side device, thereby blocking any current path from the input to the output when the converter is turned off.

CONTROL LOOP

In order to regulate the switching activity and maintain the desired output voltage, a feedback control loop is required. Among fixed-frequency switching converters, the two most common control strategies are *voltage-mode control* and *current-mode control*.

A simplified voltage-mode control loop is shown in Fig. 2.10.

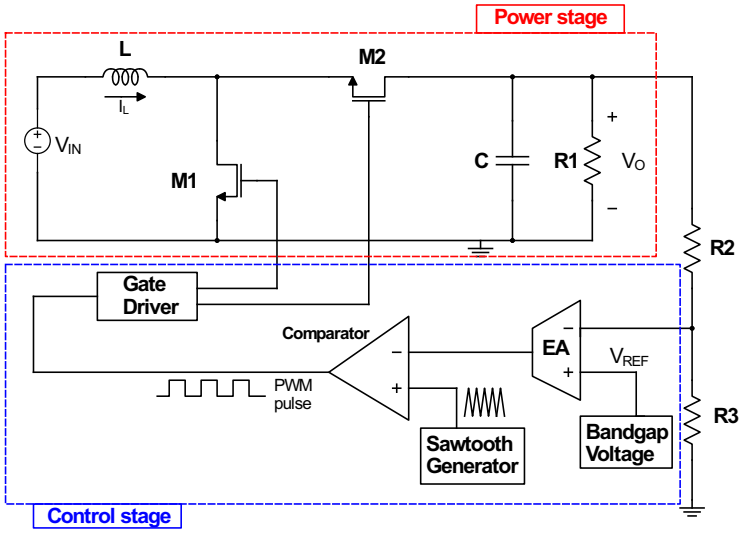


Figure 2.10: Simplified block diagram of a voltage-mode controlled boost converter

The output voltage V_O is sensed through a resistive feedback network and compared with a precise reference voltage V_{ref}. The resulting error signal is amplified by the error amplifier and processed by the compensation network to generate the control voltage. The control voltage is then compared with a periodic ramp generated by the oscillator inside the PWM modulator. The intersection between the two signals determines the duty cycle of the switching signal driving the power stage. Therefore, output voltage regulation is achieved by modulating the converter duty cycle according to the voltage error.

The main advantages of voltage-mode control are its simple implementation and good noise immunity. However, the control action is based only on the output voltage information, resulting in slower transient response and limited capability to react to sudden load variations. For these reasons, current-mode control is often preferred in modern high-performance boost converters.

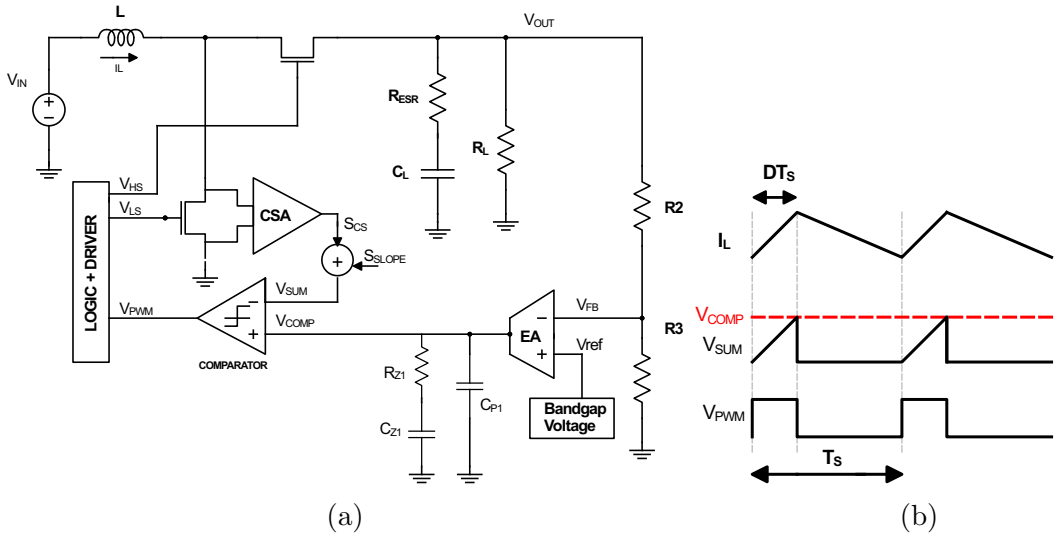


Figure 2.11: (a)Simplified block diagram of a peak current-mode controlled boost converter, (b)Generation of the PWM signal

Figure 2.11a shows the simplified block diagram of a peak current-mode controlled boost converter. Unlike voltage-mode control, this architecture employs two nested feedback loops: an inner current loop and an outer voltage loop.

The outer voltage loop operates similarly to the previous case. The output voltage is sensed through the feedback divider, generating the feedback voltage V_{FB}, which is compared with the reference voltage V_{REF}. The resulting error is amplified by the transconductance error amplifier (EA), producing the compensation voltage V_{COMP}.

The inner current loop regulates the inductor peak current on a cycle-by-cycle basis. The inductor current is sensed by the current-sense amplifier (CSA), generating a signal proportional to the instantaneous inductor current. Since peak current-mode control becomes susceptible to subharmonic oscillations for duty cycles greater than 50%, an artificial stabilizing ramp (S_{SLOPE}), known as *slope compensation*, is added to the sensed current signal S_{CS}. The sensed current and the slope compensation signal are summed together to generate V_{SUM}. As Figure 2.11b illustrates, when the inductor current increases, V_{SUM} rises until it intersects the control voltage V_{COMP} generated by the outer voltage loop. At this instant, the PWM comparator generate a pulse signal that turns the low side switch off, terminating the conduction interval. The duty cycle is therefore determined by the crossing point between V_{SUM} and V_{COMP}.

Since V_{COMP} is proportional to the output voltage error, any variation in the output voltage automatically results in a modification of the peak inductor cur-

rent and, consequently, of the converter duty cycle. This mechanism allows stable regulation of the output voltage while maintaining fast current-loop dynamics.

As a result, peak current-mode control is widely adopted in modern boost converters, particularly in applications requiring high conversion ratios and fast transient response. For these reasons, the synchronous boost converter investigated in this thesis is based on this control strategy.

2.2 State-of-the-art for OLED display application

As discussed previously, OLED power supply ICs typically generate multiple voltage rails while also requiring an isolation function to disconnect the outputs from the input source during shutdown. Commercial products implement this function in different ways, leading to different trade-offs in terms of external component count, silicon area, and pin requirements.

Since the main objective of this work is the area optimization of the isolation switch, it is important to first review how this function is implemented in current state-of-the-art OLED power management ICs.

A representative example is the TPS65131-Q1 from Texas Instruments [9]. This device integrates a boost converter for the generation of a positive voltage rail (V_{POS}) and an a negative voltage rail (V_{NEG}), making it suitable for small-to-medium size OLED and TFT-LCD panels.

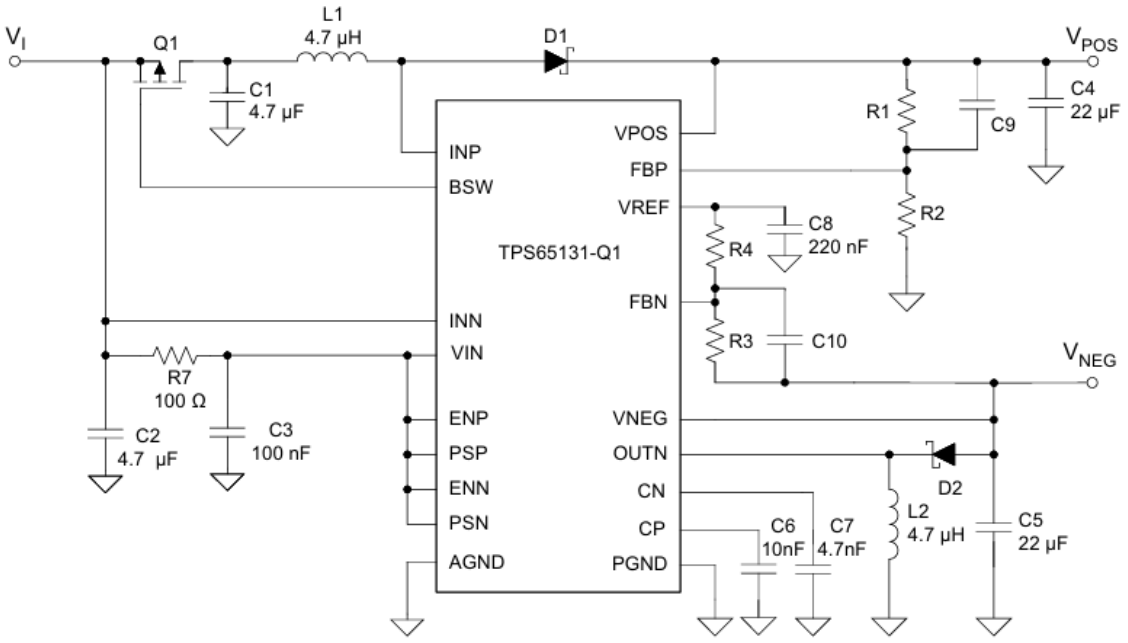


Figure 2.12: Typical application schematic of TPS65131-Q1 [9]

As shown in Fig 2.12, the isolation switch is implemented as an external component placed between the input supply V_I and the boost converter inductor $L1$.

The device provides a dedicated control pin, denoted as BSW, to drive the external switch. Although this approach simplifies the implementation of the isolation function, it increases the overall system cost and PCB area because an additional external MOSFET is required. Furthermore, the dedicated control pin contributes to the total pin count of the PMIC.

An alternative approach is adopted in the MAX25520 from Analog Devices [10], which shares a similar architecture with other devices of the same family, such as the MAX25220 [11] and MAX25169 [12].

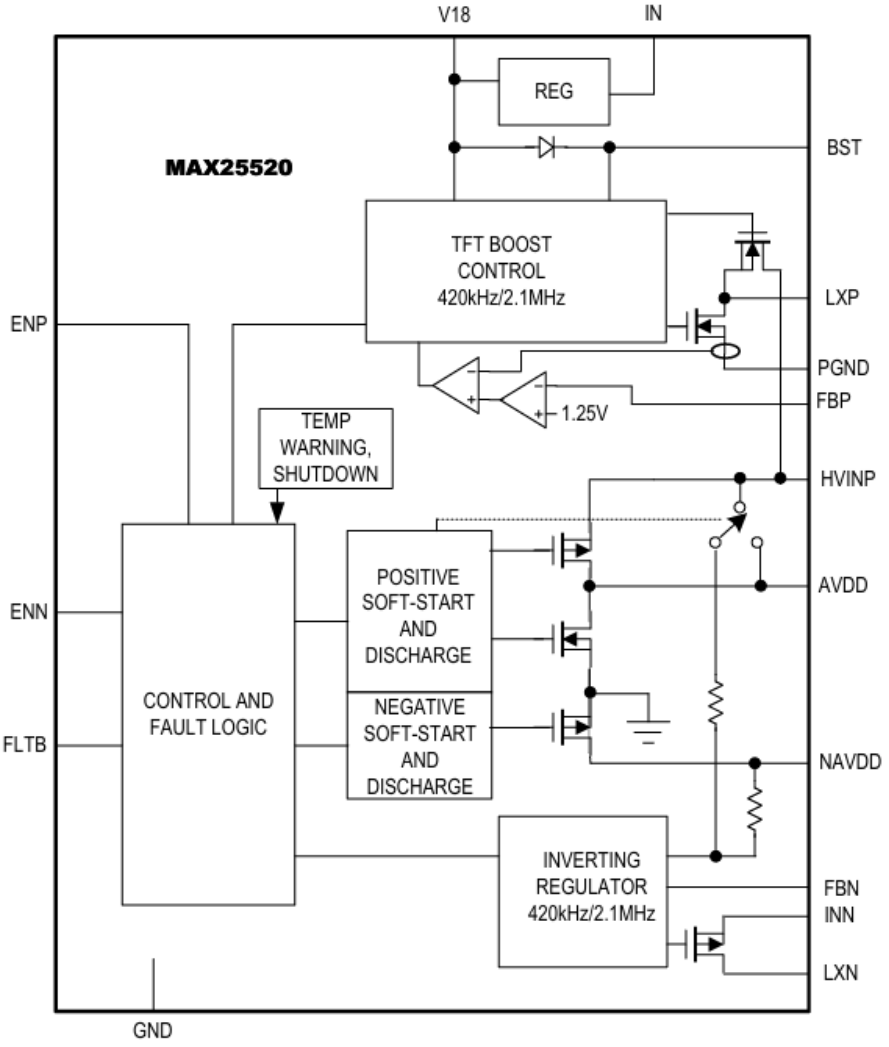


Figure 2.13: Simplified block diagram of MAX25520 [10]

In this case (Fig 2.13), the isolation function is integrated within the PMIC. The isolation switch is implemented using a PMOS transistor connected between the non-isolated boost output node HVINP and the isolated output node AVDD. By integrating the switch on-chip, the need for an external isolation device is eliminated, reducing the component count.

However, although the external transistor is removed, the architecture still requires access to both the non-isolated node HVINP and the isolated output AVDD.

Consequently, the overall pin count remains comparable to solutions employing an external isolation switch, since an additional pin is still required for the non-isolated output node.

The use of a PMOS device simplifies the implementation of the gate-driving circuitry, since no bootstrap circuit, external capacitor, or charge pump is required to generate the appropriate gate voltage. For this reason, PMOS-based solutions can be particularly attractive in low-current applications where simplicity and reduced design complexity are important considerations.

However, the choice of a PMOS isolation switch also introduces an area penalty. In CMOS technologies, PMOS transistors exhibit a significantly larger $R_{ON} \cdot Area$ product than NMOS devices due to the lower hole mobility. As a consequence, a PMOS transistor must typically occupy a substantially larger silicon area than an equivalent NMOS device to achieve the same on-resistance.

Although an NMOS-based implementation would require additional circuitry, such as an integrated charge pump, the superior area efficiency of the NMOS device itself can compensate for this overhead. Therefore, when low on-resistance and area optimization are key design objectives, the overall silicon area of an NMOS-based solution may be smaller than that of a PMOS-based implementation despite the increased driver complexity.

These examples [9] [10] highlight the main design trade-offs currently adopted in commercial OLED power supplies. External isolation switches offer implementation simplicity at the expense of additional components and cost, whereas integrated solutions reduce the component count but may introduce area overhead and maintain additional interface requirements. Therefore, the implementation of an area-efficient integrated isolation switch remains an important research and design topic.

2.3 Thesis objective and contributions

This thesis focuses on the boost converter blocks integrated within a PMIC for automotive OLED display applications, specifically those responsible for generating the AVDD and VGH supply voltages introduced in the previous chapter (chap. 1.4). Although the two converters are based on the same architecture, they operate under different output conditions. Assuming an input voltage ranging from approximately 2.8 V to 5 V, the AVDD converter generates an output voltage in the range of 5 V to 10 V while delivering load currents up to 1 A. In contrast, the VGH converter operates at higher output voltages, from 11 V up to 21 V, with output currents typically limited to 100 mA. These differences mainly affect the sizing of the circuit components.

As discussed in the previous section (chap. 2.1), OLED panel supplies often require output isolation from the input source in order to avoid unwanted current consumption when the supplies are disabled and to achieve a true shutdown condition.

A common solution is to introduce an additional isolation transistor in series with the output stage.

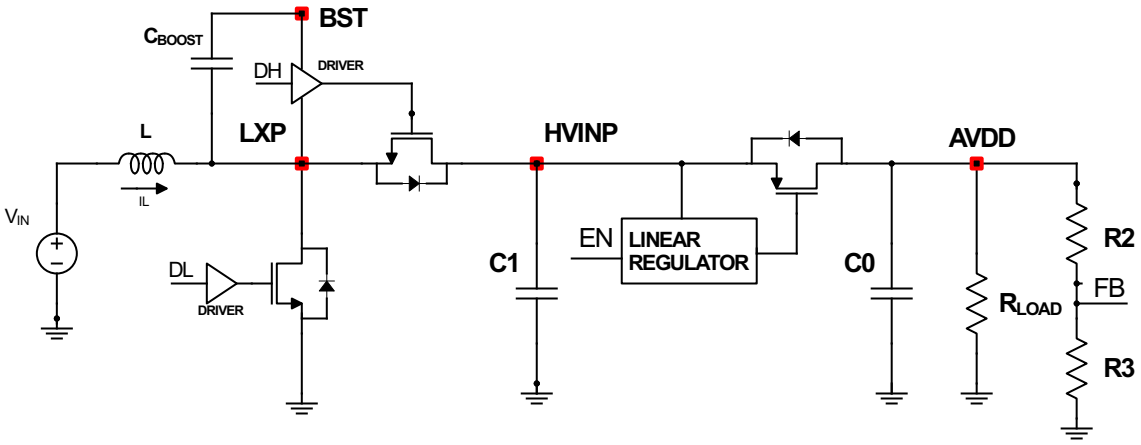


Figure 2.14: Simplified block diagram of a boost converter with high-voltage PMOS isolation switch

Figure 2.14 shows a simplified block diagram of a state-of-the-art implementation adopted for AVDD generation, with a similar architecture also used for VGH generation. The boost converter employs two N-type DMOS devices as low-side and high-side power switches, while output isolation is achieved through a high-voltage PMOS connected between the non-isolated output node, denoted as HVINP, and the isolated output node AVDD. The PMOS isolation device is controlled through a dedicated linear regulator that generates the appropriate gate voltage required to keep the transistor on during normal operation. In addition, the driving circuitry incorporates a current-limitation function that limits the maximum output current to 1 A.

Another important characteristic of this solution is the pin count required for the active switch and isolation switch circuitry. Four external pins are necessary: BST, used to connect the external bootstrap capacitor supplying the high-side driver; LXP, corresponding to the switching node where the external inductor is connected; HVINP, where the intermediate output capacitor C_1 is connected; and AVDD, which represents the isolated converter output.

This architecture presents some drawbacks from an area and cost perspective since silicon area is a critical parameter in integrated circuit design as it directly impacts manufacturing cost. In particular, PMOS transistors exhibit a $R_{ON} \times Area$ figure of merit up to 3 times worse compared to NMOS devices due to the lower mobility of holes [13]. For a given technology and conduction resistance requirement, a PMOS device may require several times the silicon area of an equivalent NMOS transistor. Consequently, the isolation PMOS represents a significant area overhead.

Furthermore, in high-pin-count integrated circuits the die size may become pad-limited rather than core-limited. In such conditions, the minimum chip dimensions are dictated by the number and pitch of the I/O pads rather than by the actual cir-

cuitry area. Therefore, reducing the number of required pins can directly contribute to reducing die size and manufacturing cost.

Motivated by these considerations, the architecture proposed in this work, shown in Fig. 2.15, replaces the PMOS isolation device with an NMOS transistor and simultaneously eliminates the HVINP pin.

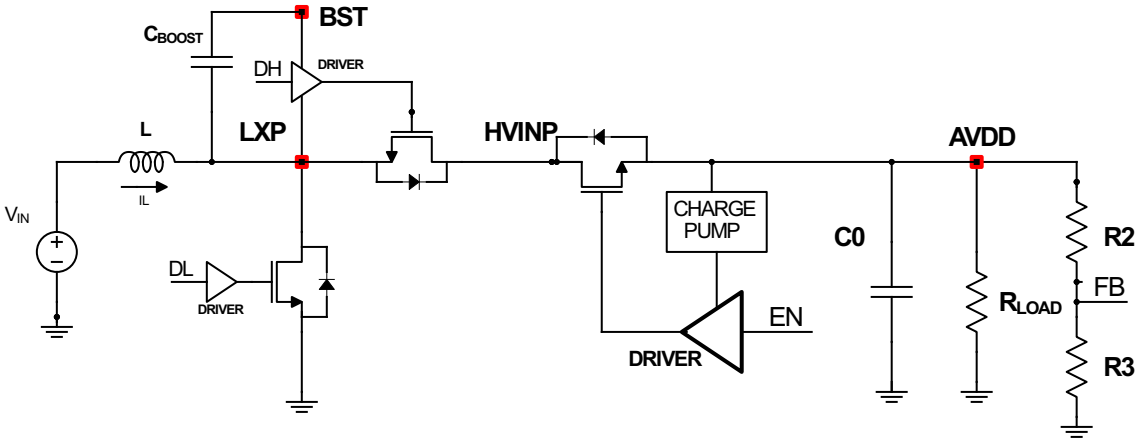


Figure 2.15: Simplified block diagram of a boost converter with NMOS isolation switch

As a result, the number of external pins is reduced from four to three. Since both the AVDD and VGH converters employ a similar isolation structure, the resulting area savings can be replicated across both power-conversion blocks, leading to a significant reduction in the overall PMIC area.

However, the proposed solution introduces new design challenges that must be carefully addressed.

First, eliminating the HVINP node also eliminates the external capacitor C_1. Consequently, the isolation transistor is no longer separated from the switching stage and becomes directly connected in series with the high-side power switch. Unlike the original architecture, where the PMOS mainly conducts the load current, the isolation device now conducts the inductor current during the high-side conduction interval. This modification changes both the current stress and the current waveform experienced by the device and must therefore be considered when implementing the current-limitation function for protection of the device.

A second challenge is related to gate driving. While the PMOS isolation transistor can be controlled using a gate voltage lower than its source voltage, the proposed NMOS device requires a gate voltage higher than the output voltage in order to keep the transistor on. For this reason, an additional integrated charge pump is required to generate a suitable supply voltage for the isolation-switch driver.

The objective of this thesis is therefore to investigate the feasibility and advantages of replacing the conventional PMOS-based isolation architecture with an NMOS-based solution while removing the HVINP pin. To support this transition,

the work first analyzes the operation and limitations of the existing architecture and evaluates its impact on silicon area and pin count with respect to the proposed solution. Subsequently, the isolation-switch driving and current-limiting circuitry of the conventional PMOS implementation is studied in detail. Finally, a new driver architecture suitable for an NMOS isolation device is designed and implemented, including the required protection functionality while achieving the targeted area reduction.

Chapter 3

Analysis of the Boost Converter Current Architecture

The work presented in this thesis began with a comprehensive analysis of boost converter's current architecture (Fig 2.14) with the aim of understanding its main operating principles. Starting from a simplified representation of the system, the circuit functionalities were investigated under various operating scenarios.

This chapter first presents the Cadence model developed to reproduce the existing boost converter architecture. A preliminary analysis then provides a reference framework for understanding the operation of the individual functional blocks and their interaction within the overall converter architecture. The analysis is initially performed using an idealized circuit representation, allowing the functionality of the converter to be evaluated without the influence of non-ideal effects. Subsequently, real active switches are implemented into the model to investigate their behaviour and obtain a more realistic representation of the converter. Finally, the main characteristics of the existing architecture are analyzed, and the aspects targeted for modification in the subsequent stages of the thesis are identified.

3.1 Modeling and functional analysis of the Boost converter architecture

The first stage of the analysis involved the development of an idealized Cadence model of the existing boost-converter architecture, including its main functional blocks. At this stage, key components such as comparators, amplifiers and power switches were modelled as ideal building blocks, resulting in a simplified system-level representation of the converter.

The purpose of this model is to capture the main functional behaviour of the existing boost converter architecture while providing a baseline platform for analysis. Starting from this idealized implementation, design modifications can be progressively introduced, enabling the evaluation of non-ideal effects.

IDEAL BOOST CONVERTER MODEL

The analysis starts from an ideal representation of the boost converter, adopted to investigate its operating principles and the interaction among the main functional blocks. The resulting Cadence model is shown in Fig. 3.1.

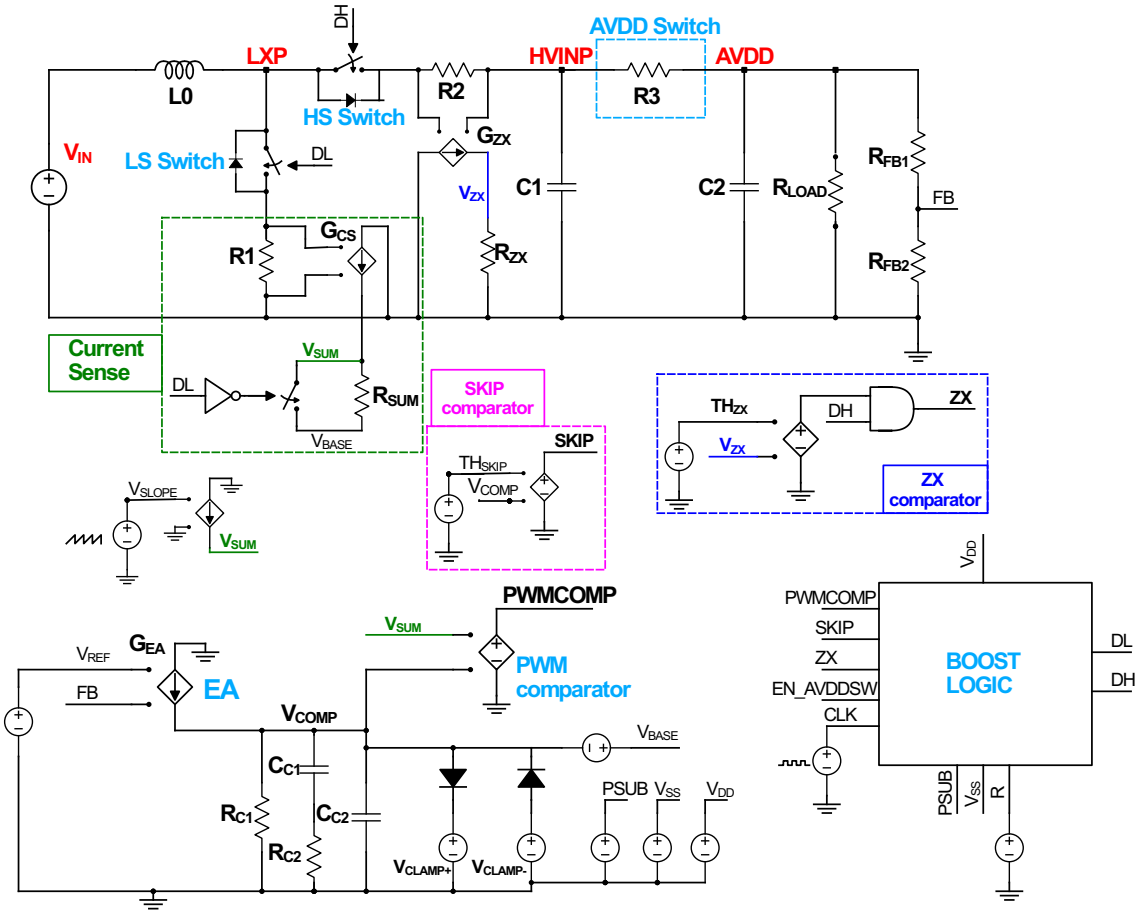


Figure 3.1: Cadence implementation of the ideal boost converter model

Figure 3.1 shows the Cadence implementation of the ideal boost converter architecture derived from the peak current-mode control loop presented in Chapter 2 (Fig 2.11). The model includes the main functional blocks of the converter while idealizing elements such as comparators, amplifiers, and power switches in order to focus on the operating principles of the control architecture.

The Error Amplifier (EA) is modeled as an ideal voltage-controlled current source (VCCS). Its inputs are the feedback signal FB, obtained from the output voltage through a resistive divider, and the reference voltage V_{REF}. The amplifier generates the control voltage V_{COMP}, which represents the main feedback signal of the regulation loop and is applied to the negative input of the PWM comparator.

The positive input of the PWM comparator is the signal V_{SUM}, obtained as the sum of the inductor current information and the slope compensation ramp. As discussed in the previous chapter (chap. 2.1), slope compensation is required in current-mode controlled converters operating with duty cycles larger than 50% in

order to prevent subharmonic oscillations [14]. The inductor current information is extracted through a current-sense network composed of a sensing resistor ($R1$) connected to the source of the low-side switch and an ideal transconductance amplifier. The amplifier converts the sensed voltage into a current flowing through resistor R_SUM, generating the voltage V_{SUM}, which is proportional to the low-side switch current and therefore to the rising inductor current during the energy storage phase.

The PWM comparator, modeled as an ideal VCVS, generates the logic signal $PWMCOMP$. As shown in Fig. 2.11b, the signal switches high whenever V_{SUM} reaches V_{COMP}, corresponding to the peak value of the inductor current. This event terminates the conduction interval of the low-side switch and initiates the activation of the high-side switch.

An additional block is included to manage the operating condition in which the inductor current reaches zero, allowing the converter to enter Discontinuous Conduction Mode (DCM). In a conventional boost converter employing a passive high-side rectifier, the diode naturally prevents reverse current flow from the output to the input when the inductor current becomes zero. This mechanism is not inherently present when the rectifier is replaced by an actively controlled high-side switch. Therefore, a Zero-Crossing (ZX) detection circuit is introduced to emulate the blocking action of the diode and prevent negative inductor current.

The control voltage V_{COMP} generated by the error amplifier is constrained by two voltage clamps. In the model, this behavior is reproduced using two diodes, as shown in Fig. 3.2.

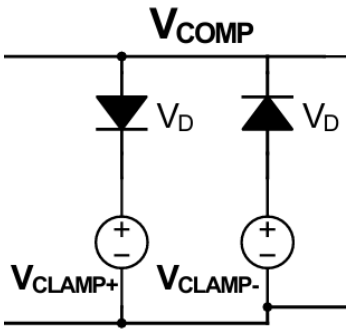


Figure 3.2: Voltage clamps for V_{COMP}

When V_{COMP} exceeds $V_{CLAMP+} + V_D$, the upper diode becomes forward biased, preventing any further increase of the control voltage. Similarly, when V_{COMP} falls below $V_{CLAMP-} - V_D$, the lower diode becomes forward biased and prevents any further decrease of V_{COMP}. Therefore, the lower clamp prevents the control voltage from reaching zero.
The upper clamp defines the maximum value that V_{COMP} can attain and therefore limits the maximum value of V_{SUM} required to terminate the low-side conduction interval. Consequently, it limits the maximum peak inductor current achievable by the converter, thereby implementing the converter's intrinsic current-limitation function.

A further block, composed of an ideal comparator, generates the logic signal *SKIP*.
The signal becomes active when V_{COMP} falls below a predefined threshold TH_{SKIP}. When V_{COMP} decreases below this threshold, the output voltage is sufficiently close to its target value and only a limited amount of energy must be delivered to the load. Under these light-load conditions, switching cycles can be selectively skipped without compromising voltage regulation. The skip mode significantly reduces switching activity and associated switching losses, thereby improving the converter efficiency at light load. However, since power is transferred only during selected switching cycles, the effective switching frequency is no longer constant. As a consequence, low-frequency components may appear in the output voltage ripple.

Finally, the low-side and high-side power switches are modeled using ideal controlled switches including their intrinsic body diodes. Their gate-drive signals, respectively denoted as DL and DH, are generated by a control block referred to as *BOOST LOGIC* in figure 3.1. In the actual implementation, these signals are produced by a more complex digital control circuitry that manages the different operating modes of the converter. In the present ideal model, this functionality is condensed into a simplified block whose purpose is to coordinate the operation of the power switches under the various operating conditions.

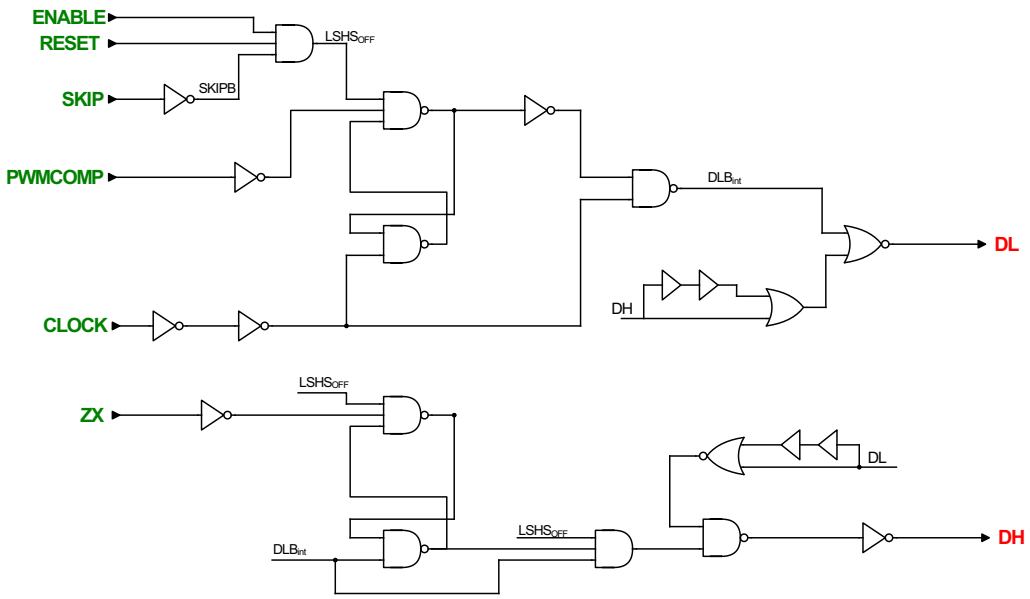


Figure 3.3: Simplified boost PWM control logic

Figure 3.3 shows the internal implementation of the simplified Boost Logic block used in the ideal converter model.

During normal operation, the low-side switch is turned off when the PWM comparator detects that V_{SUM} reaches V_{COMP}. A short dead time is then introduced before enabling the high-side switch. This delay prevents simultaneous conduction of the two power switches, avoiding shoot-through currents and ensuring safe operation of the power stage. The high-side switch subsequently conducts the inductor current to the output stage.

The logic also includes additional control signals used to manage different operating conditions. The signals *ENABLE* and *RESET* have the highest priority. When *ENABLE* is low or *RESET* is high, both gate-drive signals DL and DH are forced low, ensuring that the low-side and high-side switches remain turned off. Similarly, when the *SKIP* signal is asserted, the switching activity is suspended and both switches are kept off.
Finally, the logic processes the Zero-Crossing signal ZX. When the high-side switch is conducting and the inductor current falls below the zero-crossing threshold, the signal ZX becomes active and immediately forces DH low, turning off the high-side switch and preventing reverse current flow from the output towards the input.

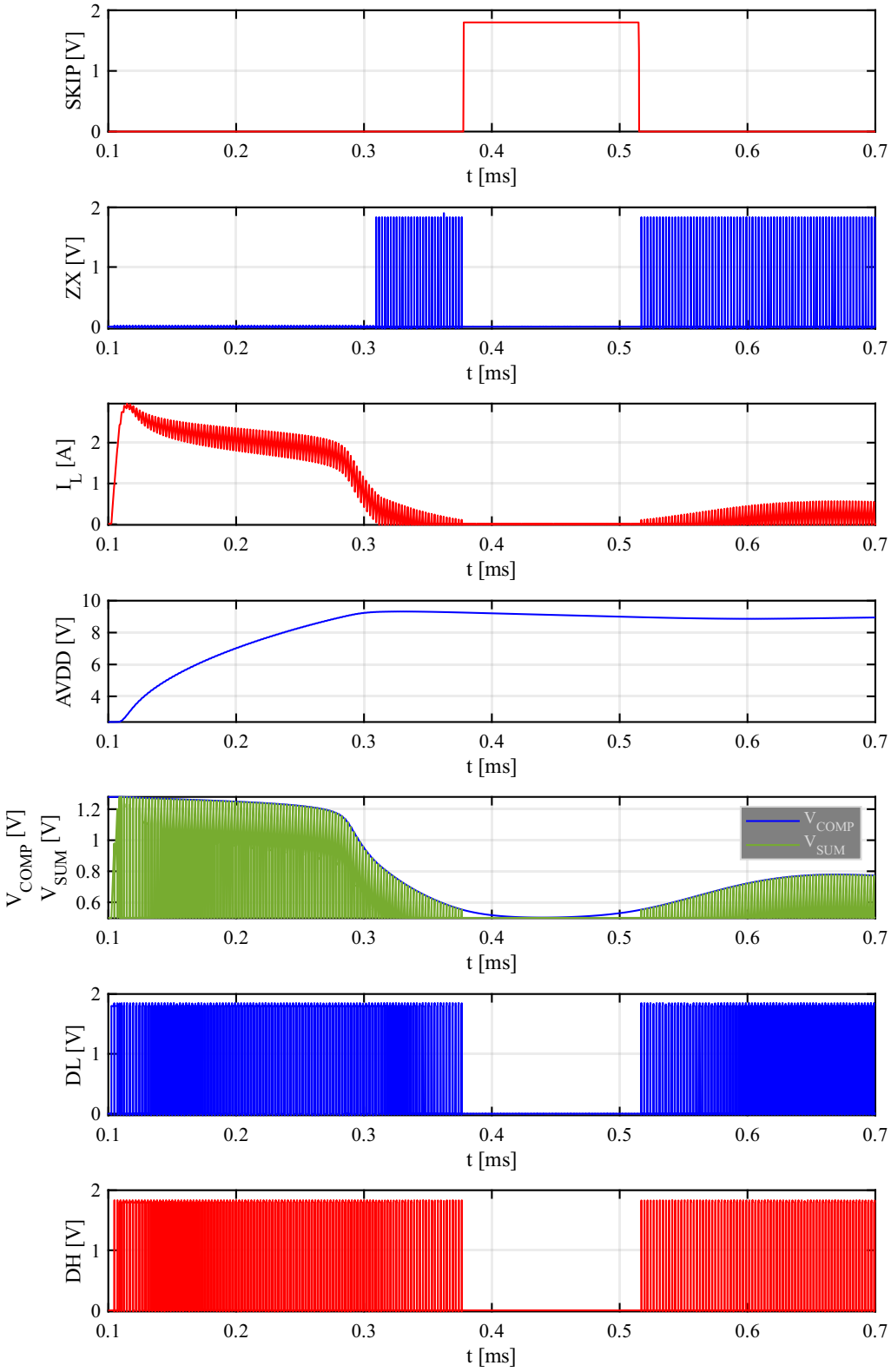
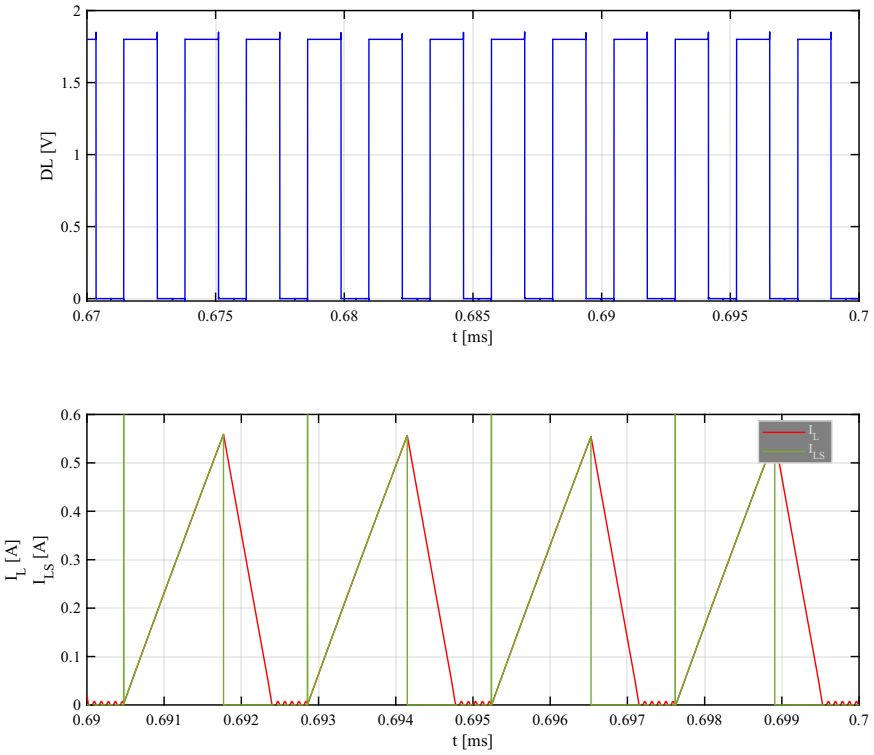


Figure 3.4: Transient simulation of the ideal boost converter model with $VIN = 3V$, $VOUT = 9V$ and a load current $ILOAD = 50mA$

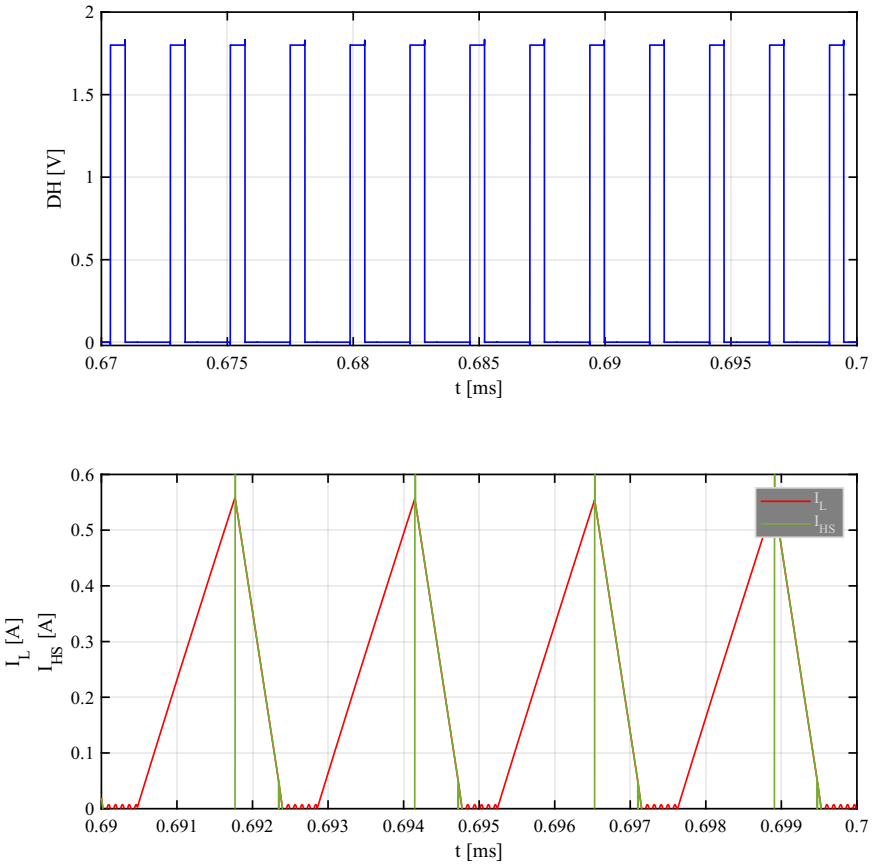
The functionality of the implemented control logic was verified through a transient simulation.
The figure 3.4 provides an overall view of the boost converter's behaviour by highlighting the interaction between the current-mode control signals (V_{SUM}, V_{COMP} and

$PWMCOMP$), the gate-drive signals (DL and DH), the zero-crossing detection signal (ZX) and the skip-mode activation signal (SKIP).

To confirm the expected operation of the power stage, the resulting current waveforms are reported in Fig. 3.5.



(a) Inductor current (I_L) and low-side switch current (I_{LS}) waveforms with respect to the gate-driving signal DL



(b) Inductor current (I_L) and high-side switch current (I_{HS}) waveforms with respect to the gate-driving signal DH

Figure 3.5

During the low-side conduction interval, the inductor current flows entirely through the low-side switch, therefore I_L and I_{LS} overlap (Fig. 3.5a).
Conversely, when the high-side switch is activated, the inductor current is transferred to the output stage and I_L coincides with I_{HS} (Fig. 3.5b).

Finally, the isolation switch, denoted as the "AVDD Switch"' in Fig. 3.1, is ideally modeled as a resistor. This simplification is justified by the fact that, when enabled, the switch operates in the linear region and therefore behaves as a low-resistance conduction path between its terminals.

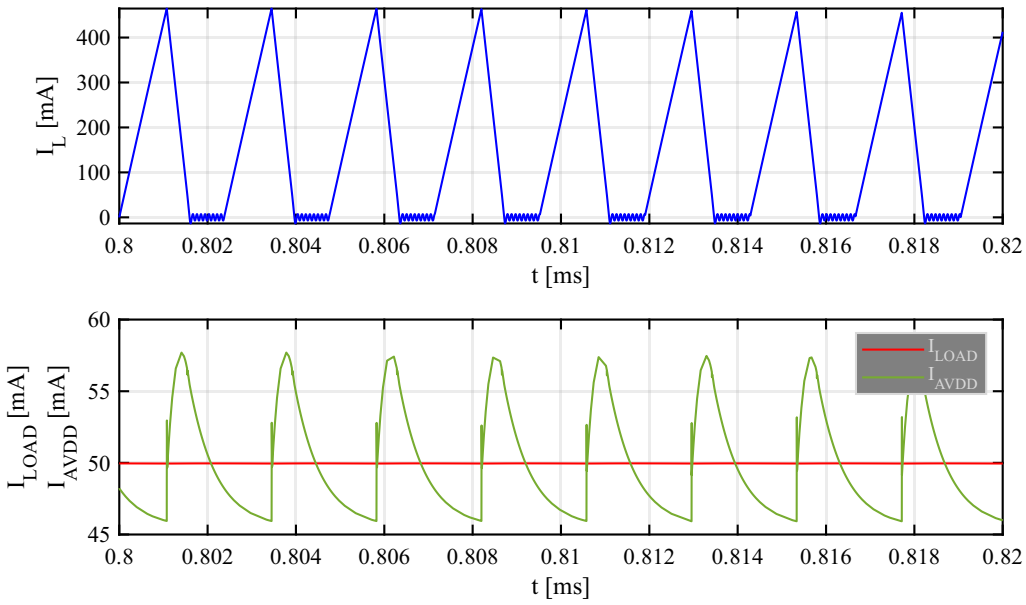


Figure 3.6: Current waveforms that show the current flowing through the inductor I_L, the AVDD isolation switch (I_{AVDD}) and the load current I_{LOAD}

The figure 3.6 shows the current I_{AVDD} flowing through the modeled AVDD switch. The simulation performed under the same conditions as Fig. 3.4 shows that the I_{AVDD} average value is approximately 50 mA, which is in agreement with the imposed load current of 50 mA and confirms that the output load current is properly delivered through the isolation switch.

REAL SWITCHES BOOST CONVERTER MODEL

To obtain a more accurate description of the system behavior, the ideal switches and the isolation switch resistance are replaced with transistor-level models that account for finite on-resistance, parasitic capacitances, switching delays, and body-diode conduction.

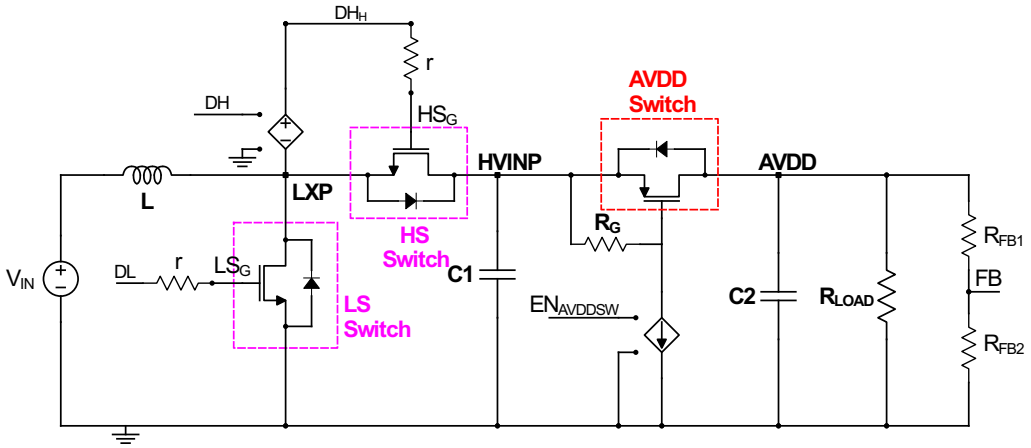
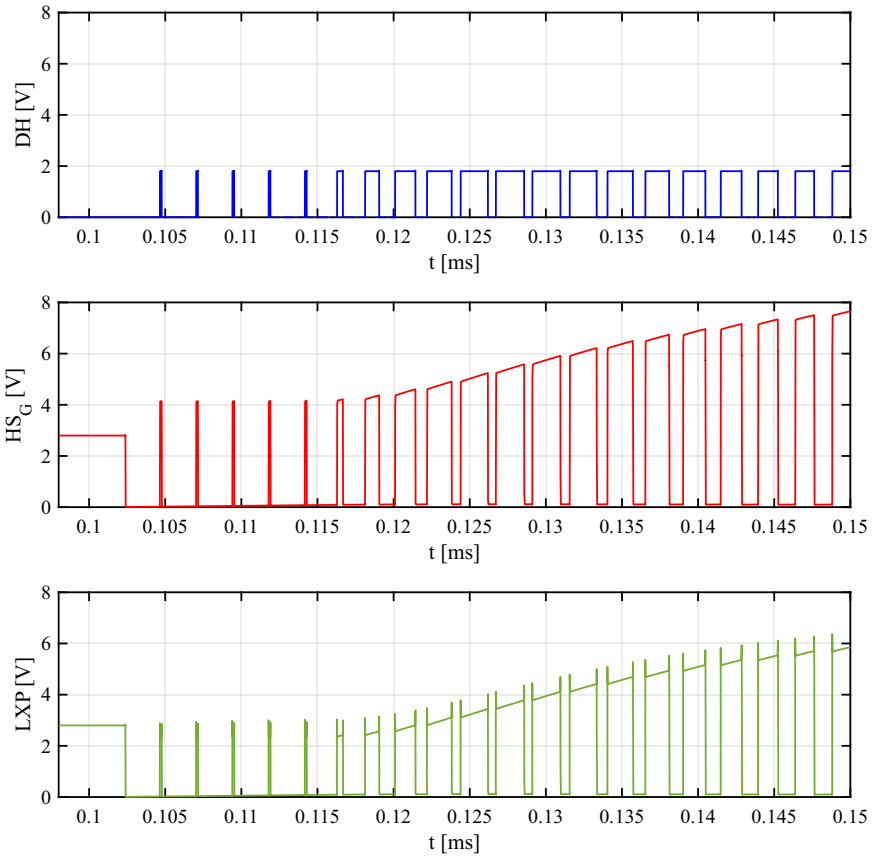


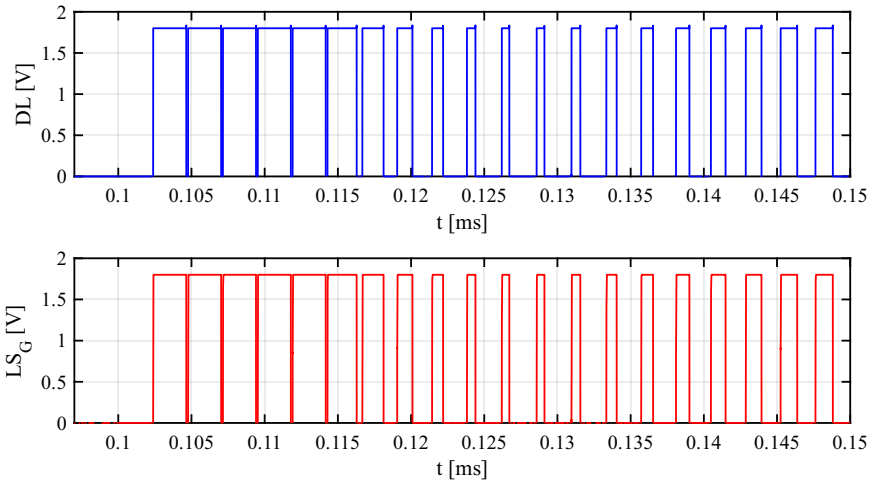
Figure 3.7: Simplified model of the power stage of a boost converter with real switches

In the real-switch implementation, the gates of the power transistors must be driven by a realistic driver rather than by ideal voltage sources. This choice avoids unrealistically fast switching transitions and reproduces the finite charging and discharging time of the MOS gate capacitances. The purpose of the driver is to turn the transistors on and off while imposing a gate-to-source voltage V_{GS} of approximately $1.8V$.

The adopted driver model consists of a VCVS and a resistance r connected to the gate of the power switch. For the low-side switch, the driving signal DL is applied directly to the driver input. For the high-side switch, the control signal DH is first level-shifted with respect to the source node LXP. The resulting gate voltages of the low-side and high-side transistors are denoted as LS_G and HS_G respectively, and are shown in fig. 3.8.



(a) Waveforms of high side switch driving signal DH, gate voltage HS_G, and source voltage LXP



(b) Waveforms of low side switch driving signal DL and gate voltage LS_G

Figure 3.8

As highlighted in Fig. 3.9, the presence of the finite resistance r causes the gate capacitances to charge and discharge with a finite time constant. Consequently, the gate voltages LS_G and HS_G follow the corresponding control signals while exhibiting smoother rising and falling edges. This behavior more accurately reproduces the switching transitions of a practical gate driver and allows the switching dynamics of the converter to be evaluated under realistic operating conditions.

The implementation of the isolation switch (AVDD switch) requires additional

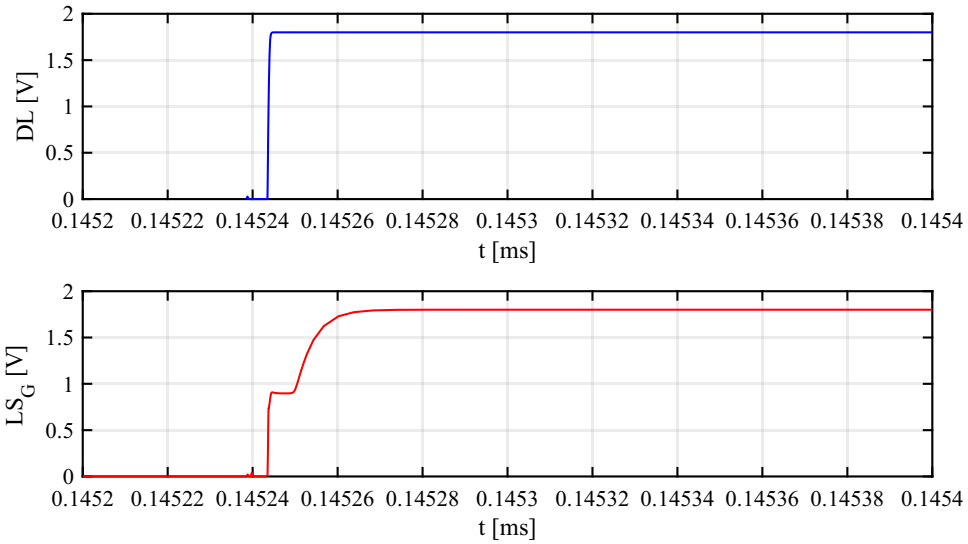


Figure 3.9: Focus on rising edge of low side switch driving signal DL and gate voltage signal LS_G

considerations when replacing the ideal resistor used in the previous model with a transistor-level device.

First, an appropriate gate-drive circuit must be included to provide the required source-to-gate voltage and control the switch according to the enable signal. When the signal EN_{AVDDSW} is asserted, the transistor is turned on and the isolated output AVDD is connected to the boost output node. In the proposed model (Fig. 3.7), the gate-drive circuit is implemented in order to generate a source-to-gate voltage V_{GS} of approximately 1.8 V, sufficient to operate the transistor in the triode region.

Unlike the ideal switch adopted in the previous model, the transistor exhibits parasitic capacitances that influence its switching behavior. In particular, the gate-drain capacitance gives rise to the well-known Miller effect. During turn-on, as soon as the drain current starts to flow and drain-to-source voltage starts do decrease, the gate-drain capacitance C_{gd} must be charged, therefore a significant portion of the gate current is diverted to charging C_{gd}, causing the gate-to-source voltage to remain nearly constant. This phenomenon, known as the Miller plateau, delays the complete turn-on of the device.

Therefore, as shown in fig 3.10, although a gate voltage of $1.8\,V$ is eventually applied, the transistor does not reach its fully enhanced state instantaneously. This results in a smoother transition between the off-state and the on-state compared to an ideal switch.

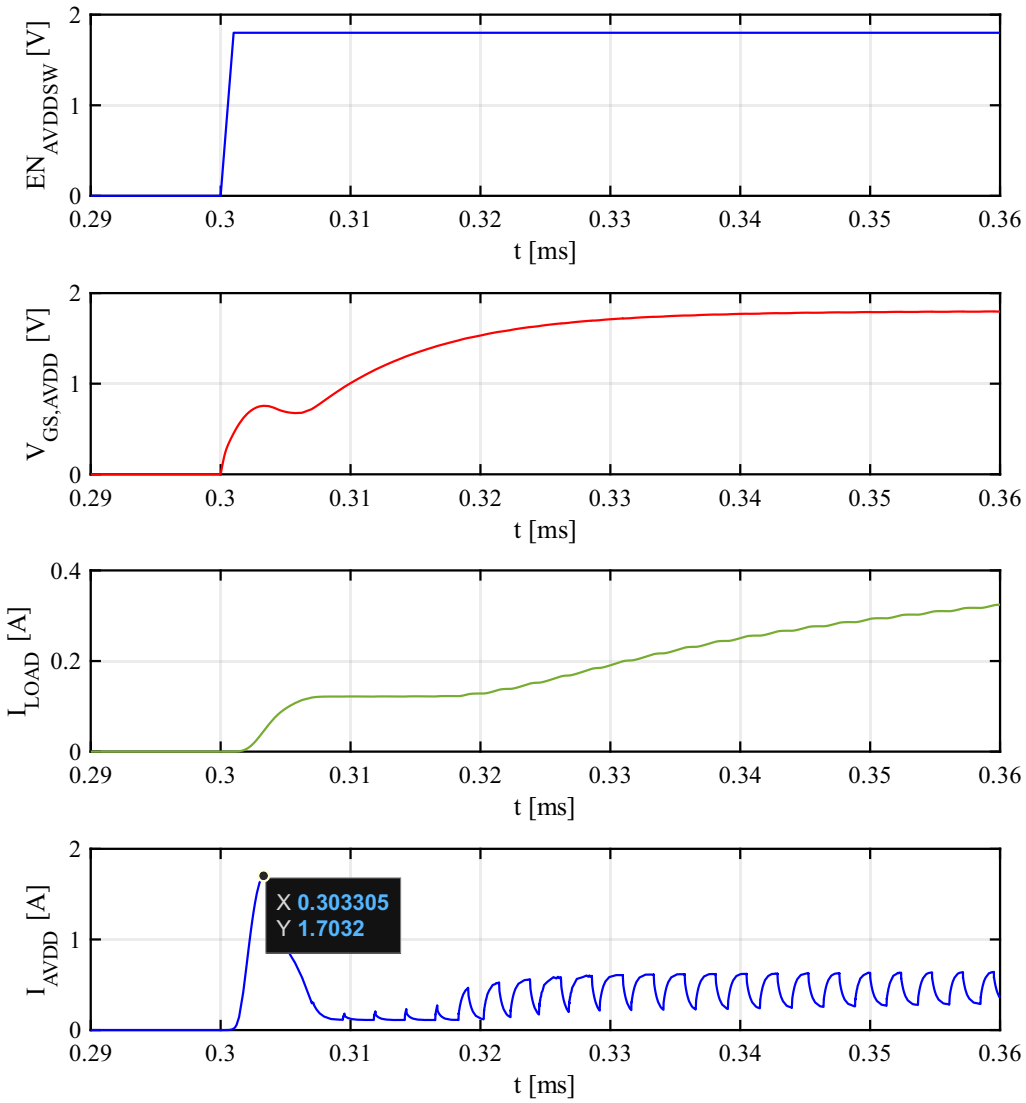


Figure 3.10: Simulation of EN_{AVDDSW}, $V_{GS,AVDD}$, I_{LOAD} and I_{AVDD} waveforms, performed at $V_{IN} = 2.8V$, $AVDD = 10V$ and $I_{LOAD} = 500mA$, that display the Miller Plateau effect when the boost is enabled and the switch is turned on

Interestingly, this non-ideal behavior proves beneficial during the charging transient of the AVDD output. At startup, charge sharing between capacitors $C1$ and $C2$ generates an inrush current through the AVDD switch. Owing to the finite turn-on time introduced by the Miller effect, this current spike is significantly reduced, limiting the electrical stress on the device.

Another important aspect of the isolation switch design is its voltage rating. In the considered architecture, the node HVINP is not only the input of the isolation switch but also serves as an internal supply node for additional circuit blocks. Consequently, HVINP may remain regulated at the boost output voltage even when the isolated output AVDD is disabled. The most critical operating condition for the AVDD switch therefore occurs when HVINP is at its maximum output voltage while AVDD is held at 0 V, therefore the maximum drain-to-source voltage that the isolation switch must withstand is

$$V_{DS,max} = V_{OUT,max}.$$

During normal operation with the boost converter disabled, the voltage at HVINP is approximately equal to $V_{IN} - V_D$, while AVDD remains discharged. Consequently, the isolation switch initially experiences a drain-to-source voltage close to V_{IN}. Once the switch is enabled, AVDD is charged from the HVINP node and the transistor progressively enters the triode region. In steady-state conditions, the voltage across the device is reduced to the on-state voltage drop associated with its finite on-resistance R_{ON}, which is typically on the order of a hundred of mV.

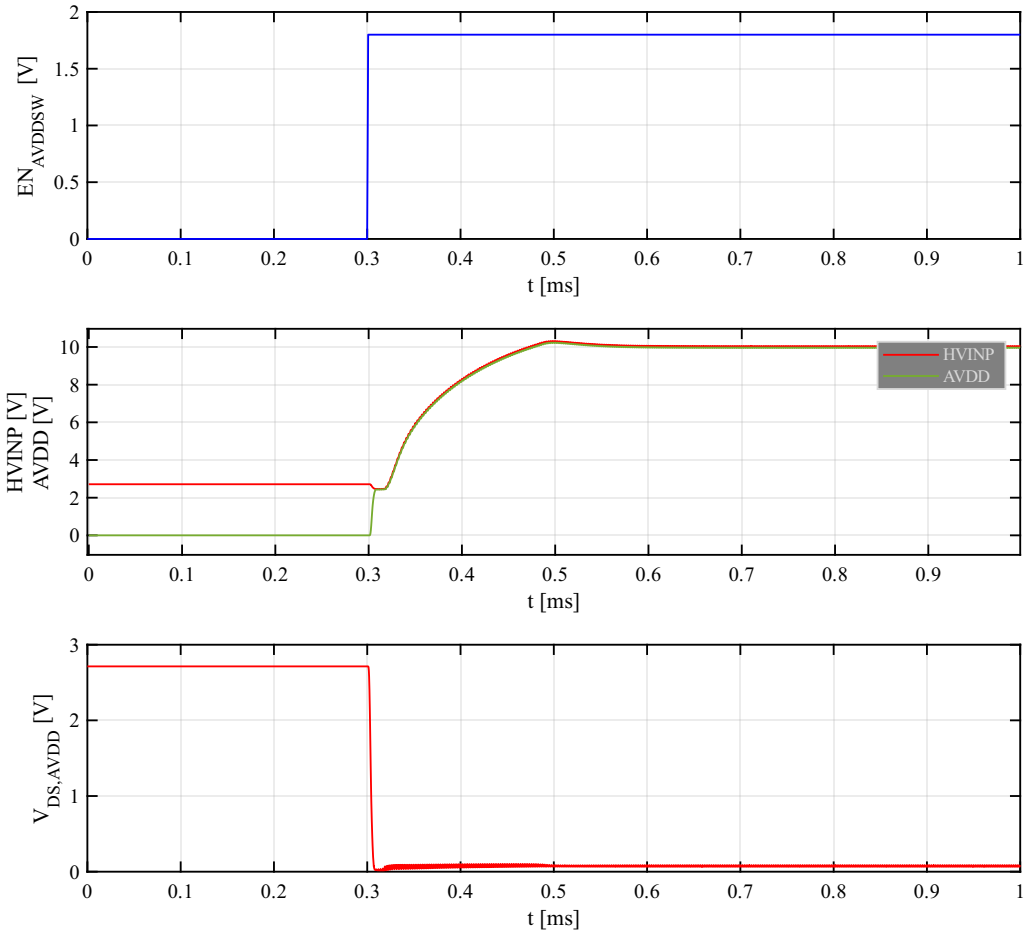


Figure 3.11: Simulation waveforms of nodes $HVINP$ and $AVDD$ and voltage drop across the switch $V_{DS,AVDD}$ with respect to the EN_{AVDDSW} signal

Fig. 3.11 shows the simulated waveforms of HVINP and AVDD for $V_{IN} = 2.8\,\text{V}$ and $V_{OUT} = 10\,\text{V}$. The figure also reports the evolution of $V_{DS,AVDD}$, highlighting the transition from the off-state condition to the low-voltage-drop operating regime achieved after enabling the isolation switch.

3.2 Preliminary considerations for the implemented solution

In order to reduce the overall silicon area of the boost converter, several architectural modifications are introduced. These choices, however, impact the converter operation and impose additional design constraints. Therefore, the main implications of

these modifications are briefly discussed in this section, as they motivate and guide the design choices presented in the remainder of this work.

ANALYSIS of CURRENT FLOW

One of the first architectural modifications considered for area reduction is the removal of the HVINP pin. As discussed in the previous chapter (chap. 2.3), eliminating this node reduces the overall pin count and contributes to lowering the silicon area.

From a circuit perspective, removing the HVINP pin also implies removing the external capacitor C_1 connected to it. Since this modification significantly affects the current distribution within the power stage, a preliminary current analysis is required.

Consider first the original architecture, in which the HVINP pin is present and connected to the external capacitor C_1. In this case, the current flowing through the high-side switch, I_{HS}, which is equal to the inductor current I_L when the switch is on, is split between the capacitor current I_{HVINP} and the current flowing through the isolation switch I_{AVDD}.

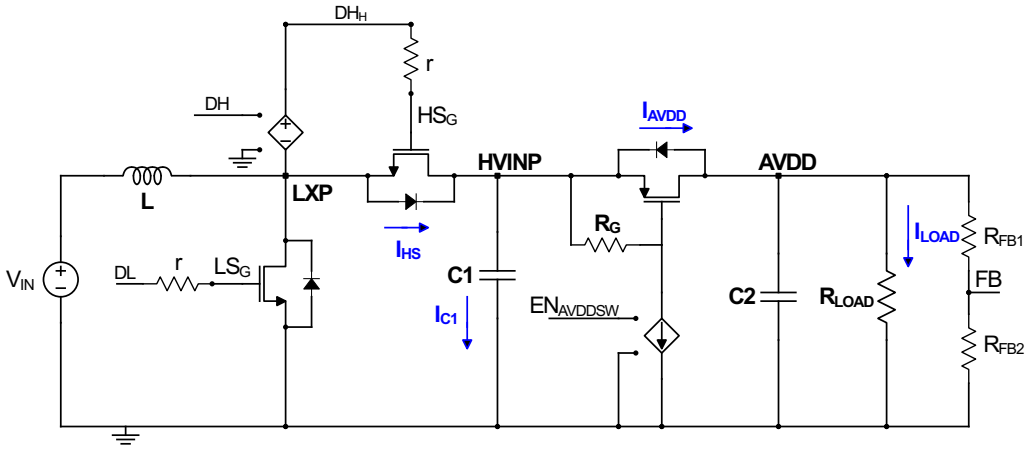


Figure 3.12: Boost converter schematic with HVINP pin highlighting the current distribution between the external capacitor C_1 and the isolation switch

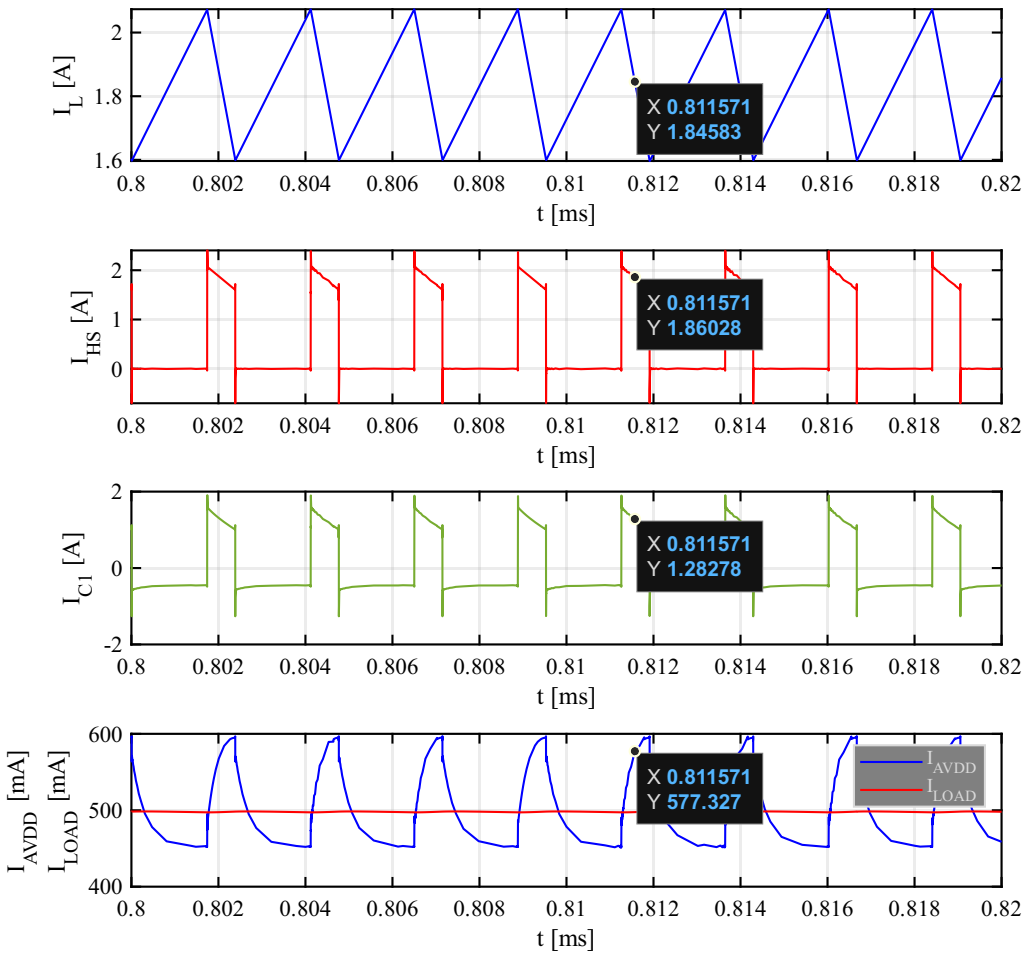


Figure 3.13: Simulation of current distribution: inductor current I_L, high side switch current I_{HS}, capacitor C1 current I_{C1}, isolation switch current I_{AVDD} and load current I_{LOAD}

For the operating conditions $V_{IN} = 2.8\,\text{V}$, $V_{OUT} = 10\,\text{V}$, and $I_{LOAD} = 500\,\text{mA}$, the simulation results shown in fig 3.13 confirm that the average value of I_{AVDD} is approximately equal to the load current. Therefore, in the original architecture, the isolation switch mainly carries the output load current.

Let us now consider the modified architecture in which the HVINP pin and the external capacitor C_1 are removed.

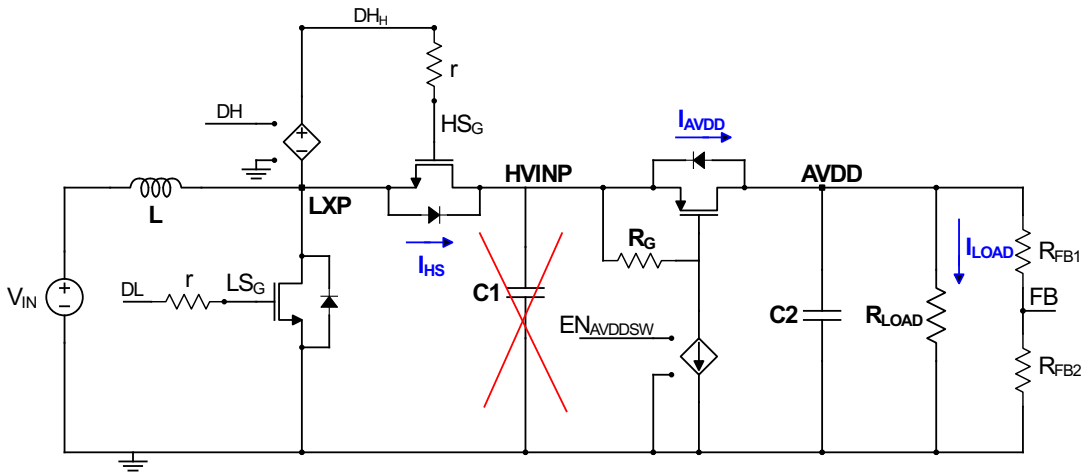


Figure 3.14: Boost converter schematic without HVINP pin and C1 capacitor, highlighting the current distribution

Under these conditions, the isolation switch is placed directly in series with the high-side switch and no current splitting can occur.

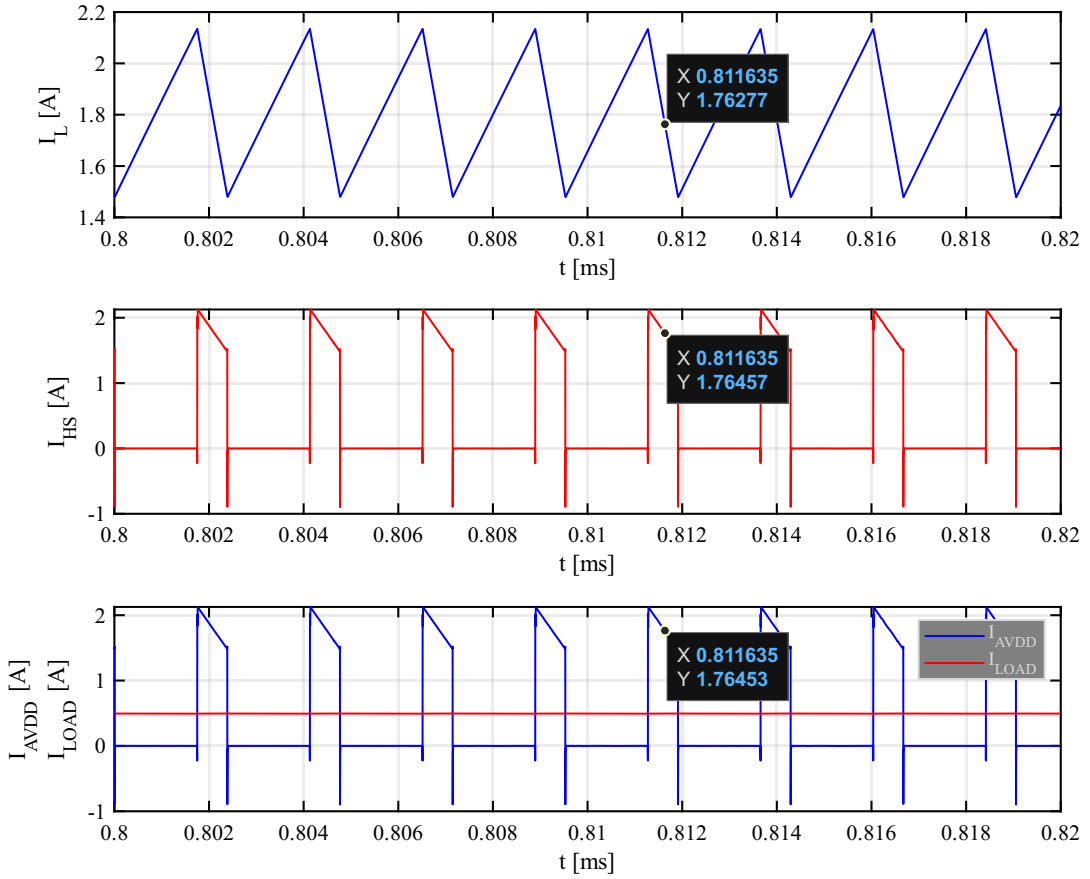


Figure 3.15: Simulation of current distribution of the configuration without C1: inductor current I_L, high side switch current I_{HS}, isolation switch current I_{AVDD} and load current I_{LOAD}

For the same operating conditions as fig 3.13, fig. 3.15 shows the simulation results of the current analysis. Unlike the previous architecture, I_{AVDD} no longer

corresponds to the load current but follows the waveform of the high-side switch current. As a result, I_{AVDD} is zero while the low-side switch is conducting and becomes equal to the inductor current I_L during the interval in which the high-side switch is turned on.

The comparison highlights an important consequence of removing the HVINP node. While in the original architecture the isolation switch was required to carry a maximum current approximately equal to $I_{LOAD,max}$, in the modified architecture it must withstand the peak inductor current required to supply the same load. Since the peak inductor current is significantly larger than the output load current, this aspect must be carefully considered during the implementation of both the isolation switch and its current-limiting circuitry. In particular, the current limit can no longer be defined solely on the basis of $I_{LOAD,max}$, but must account for the maximum inductor current that can occur during converter operation.

TRANSISTOR VOLTAGE RATING

Another important consideration is the voltage rating of the isolation-switch transistor. The voltage rating corresponds to the maximum drain-to-source voltage that the device can withstand without undergoing breakdown and, ultimately, influences the minimum device dimensions available in the technology. In general, transistors designed for lower voltage ratings occupy a smaller silicon area than higher-voltage devices.

As discussed in the previous section, when the HVINP node is used as a non-isolated supply rail for other circuit blocks, the worst-case voltage stress across the isolation switch occurs when HVINP is regulated at the maximum output voltage while AVDD is disabled. Under these conditions, the maximum drain-to-source voltage sustained by the device is approximately equal to $V_{OUT,max}$.

Let us now consider the modified architecture in which the HVINP pin is removed, and the node is exclusively dedicated to the source terminal of the isolation switch. In this case, the worst-case voltage condition occurs when the converter outputs are disabled. While AVDD remains discharged at 0 V, the body diode of the high-side switch precharges the HVINP node to approximately $V_{IN} - V_D$. As a result, the maximum drain-to-source voltage across the isolation switch becomes

$$V_{DS,max} \approx V_{IN,max}.$$

Since $V_{IN,max}$ is significantly lower than $V_{OUT,max}$, the required voltage rating of the isolation switch can be substantially reduced. This enables the use of a lower-voltage transistor, which typically occupies less silicon area and therefore contributes to the overall area reduction of the proposed architecture.

NMOS ISOLATION SWITCH DRIVING REQUIREMENTS

Another important consideration arises from the replacement of the PMOS isolation switch with an NMOS device. As discussed previously (chap. 2.3), the use of an NMOS transistor can significantly reduce the silicon area required to achieve a given on-resistance. However, this choice introduces additional constraints related to the gate-driving circuitry.

In the original architecture, the PMOS switch was driven by a relatively simple circuit that generated a gate voltage lower than the source voltage by the amount required to establish the desired gate-to-source voltage V_{GS}. Moreover, the driving circuitry included a current-limitation function, which is a feature that must be preserved in the proposed implementation.

When the isolation switch is implemented with an NMOS transistor, the driving requirements become different. In order to turn the device on, the gate voltage must be higher than the source voltage by at least the threshold voltage and, more generally, by the V_{GS} required to achieve the target on-resistance. Since the source terminal of the isolation NMOS is connected to the output node AVDD, the gate driver must therefore generate a voltage higher than AVDD. This requirement cannot be fulfilled using the available supply rails alone and typically requires the adoption of an integrated charge pump.

Consequently, the design of the driving circuitry must be compatible with the integration of the charge pump, both in terms of the output current that can be supplied and the generated output voltage. In particular, the charge pump must provide a sufficiently high voltage to guarantee the required overdrive across the entire operating range of AVDD.

Furthermore, as highlighted by the current analysis presented previously, the current flowing through the isolation switch is no longer limited to the load current but follows the high-side switch current and can reach the peak inductor current. Therefore, maintaining the current-limitation functionality becomes even more important for device protection. The current limit can no longer be designed solely on the basis of the maximum load current $I_{LOAD,max}$, but must instead be sized according to the maximum current that may flow through the isolation switch during converter operation.

The analyses presented in this section highlight the main implications arising from the proposed area-reduction strategies. In particular, the removal of the HV-INP pin and the adoption of an NMOS-based isolation switch introduce new constraints in terms of current handling, voltage rating, and driving circuitry. Taking these considerations into account, the next step is the sizing of the isolation switch, with the objective of minimizing its silicon-area contribution while ensuring compliance with the required electrical specifications.

Chapter 4

Isolation Switch Sizing and Area Optimization

In the proposed architecture, where the HVINP node is no longer externally available, the first design aspect that must be addressed is the implementation of the isolation switch. In particular, the choice of the device type and its sizing play a key role in determining the overall area efficiency of the solution.

Consequently, this chapter presents the methodology adopted to identify the minimum-area isolation switch implementation for the two operating scenarios considered in this work. The analysis is developed through successive design steps and is complemented by layout-level comparisons, providing a qualitative evaluation of the area impact associated with each implementation alternative and of the advantages offered by the proposed architecture with respect to the original one.

4.1 Area Impact Analysis and Sizing Methodology

The selection of the isolation switch device depends on several factors. First, a fundamental physical difference exists between the two MOSFET types considered in this work. As mentioned previously (chap. 2.3), PMOS transistors rely on holes as majority carriers, whereas NMOS transistors rely on electrons. Since the mobility of holes is typically two to three times lower than that of electrons, PMOS devices exhibit a higher on-resistance per unit area than equivalent NMOS devices [13]. As a consequence, for a given target R_{ON}, an NMOS generally requires a smaller silicon area, making it a potentially more area-efficient solution.

A second aspect to be considered is the operating range of the boost converter. In particular, the input voltage, output voltage and maximum load current determine both the voltage stress across the isolation switch and the current it must conduct. Up to this point, the discussion has mainly focused on the AVDD panel supply application. However, from an architectural perspective, the same analysis can be extended to the VGH gate-driver supply application, since the operating principle of the proposed architecture remains unchanged. The two scenarios mainly differ in terms of output voltage and maximum load current requirements.

Parameter	AVDD	VGH
Vin	2.8 V - 5.5 V	2.8 V - 5.5 V
Vout	5 V - 10 V	11 V - 21 V
Iout,max	1 A	100 mA

Table 4.1: Operating conditions considered for the two scenarios

Table 4.1 summarizes the operating ranges considered for the AVDD and VGH supply scenarios. Since these parameters strongly influence both the device selection and its sizing, the area impact analysis is carried out separately for the two cases. This makes it possible to evaluate how the area impact of the isolation switch varies with the operating conditions and to quantify the area savings achievable with the proposed architecture in each application.

SIZING METHODOLOGY

The design methodology adopted to identify the minimum-area isolation switch implementation is applied to both operating scenarios introduced in the previous section.

To ensure a fair comparison among the different implementations, all sizing simulations are performed under worst-case operating conditions, namely minimum input voltage, maximum output voltage, and maximum load current. These conditions maximize the current stress on the isolation switch and therefore determine the largest device size required to satisfy the design specifications.

As a first step, simulations are carried out on the original architecture to establish a reference point for the subsequent comparisons. This isolation-switch implementation serves as a baseline for evaluating the area impact of the modifications introduced in the following design steps.

In the second step, the analysis is repeated on the proposed architecture after removing the capacitance connected to the HVINP node. This modification reproduces the effect of eliminating the external HVINP pin and allows the impact of the resulting increase in current stress on the isolation-switch area to be quantified.

The third step takes into account the voltage-rating considerations discussed in the previous chapter(chap. 3.2). In the original architecture, the isolation switch must withstand the maximum output voltage generated by the boost converter. In the proposed architecture, instead, the maximum voltage across the switch is limited by the input-voltage range. This enables the replacement of the original high-voltage PMOS device with a lower-voltage-rated PMOS, allowing the area savings associated with the reduced voltage rating to be evaluated.

Finally, the PMOS isolation switch is replaced with an NMOS device. Owing to the lower on-resistance per unit area achievable with NMOS transistors, this step evaluates the maximum area reduction that can be obtained from the isolation switch itself. At this stage, only the device area is considered, while the gate-

driving circuitry is intentionally excluded from the comparison. The results obtained for both operating scenarios are then compared to assess whether an NMOS-based implementation represents the most area-efficient implementation in each case.

4.2 Panel Supply Scenario

The sizing methodology described in the previous section is now applied to the panel-supply scenario. Simulations are performed under worst-case operating conditions, namely $V_{IN} = 2.8V$, $V_{OUT} = 10V$, and $I_{LOAD} = 1A$. These conditions maximize the stress on the isolation switch and therefore determine the largest device size required to satisfy the design specifications. The results obtained at each design step are used to evaluate the impact of the proposed architectural modifications on the isolation-switch implementation and its associated layout area.

1. **Reference HV PMOS Implementation**

   As a reference case, the original boost-converter architecture is first considered, where the HVINP node is externally available and the capacitor C_1 is connected to it. The isolation switch is implemented using a 14-V PMOS device, selected to provide sufficient voltage margin with respect to the maximum output voltage of $10V$ considered in this scenario.

   The objective of this first simulation is to characterize the operating conditions experienced by the isolation switch and to extract the parameters required for the subsequent comparisons. In particular, the maximum current flowing through the device and its on-resistance are evaluated under the worst-case operating conditions defined previously.

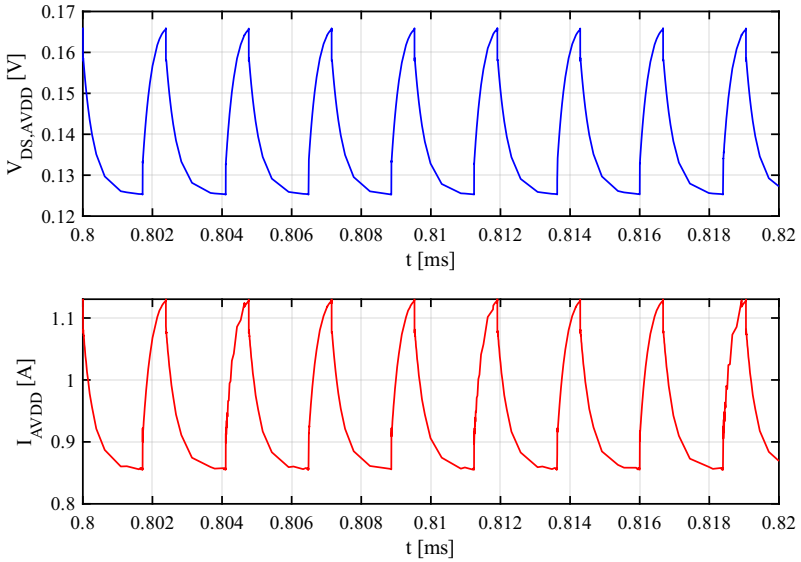


Figure 4.1: Isolation-switch current I_{AVDD} and voltage drop $V_{DS,AVDD}$ in the reference implementation

   Figure 4.1, as expected, shows that the switch conducts the output current delivered to the load. Under worst-case operating conditions, the current flowing through the device reaches an average value of approximately $1A$.

Assuming operation in the triode region, where the transistor behaves approximately as a linear resistor, the effective on-resistance is obtained from the simulated waveforms as the ratio between the drain-to-source voltage drop and the corresponding conduction current,

$$R_{ON} \approx \frac{V_{DS}}{I_D}. \tag{4.1}$$

Applying this procedure to the simulated operating point yields an equivalent on-resistance of approximately 146 mΩ. This implementation is used as the reference for all the subsequent sizing and area comparisons.

2. **Impact of HVINP Pin Removal**

Removing the external capacitor C_1 from the HVINP node significantly modifies the current flowing through the isolation switch. As discussed in the previous chapter (chap. 3.2), in the absence of the external capacitor the switch must directly conduct the pulsating current associated with the high side switch.

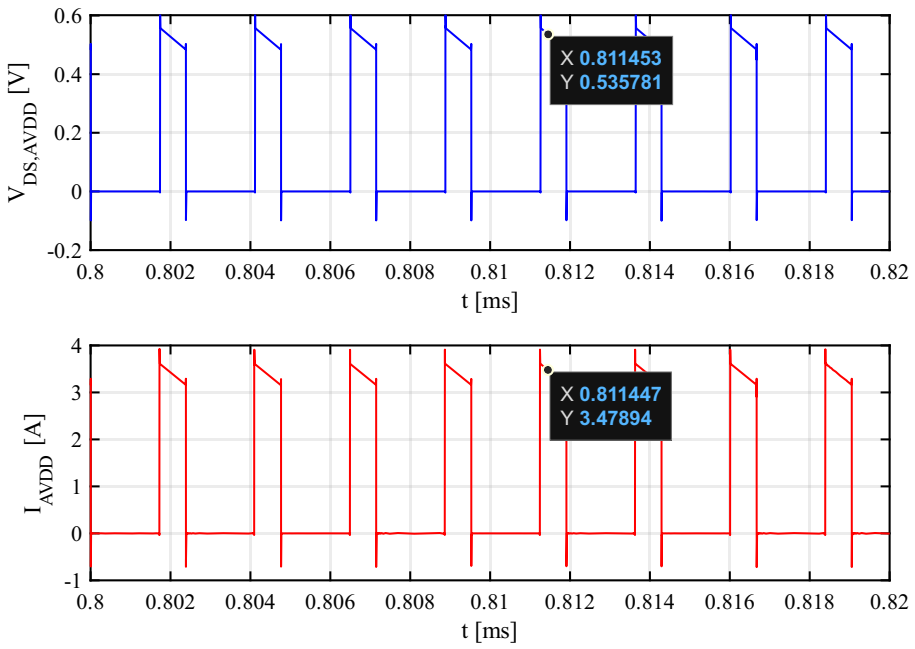


Figure 4.2: Isolation-switch current I_{AVDD} and voltage drop $V_{DS,AVDD}$ after removal of the HVINP pin and capacitor C_1, with no width size variation with respect to step 1

The current waveform obtained from simulations is shown in Fig. 4.2. Compared to the reference implementation, the maximum current flowing through the isolation switch increases significantly.

To avoid degrading the converter performance with respect to the reference implementation, the sizing criterion adopted in this step consists in maintaining approximately the same voltage drop across the isolation switch. Therefore,

the target on-resistance is scaled according to the increase in the current flowing through the device.

Assuming the same voltage drop across the switch,

$$V_{DS,ref} = V_{DS,new}$$

and considering eq 4.1 the target on-resistance can be expressed as

$$R_{ON,new} = R_{ON,ref} \frac{I_{AVDD,ref}}{I_{AVDD,new}}. \tag{4.2}$$

Simulation results show that the ratio between the current flowing through the isolation switch in the proposed architecture and in the reference implementation is approximately

$$\frac{I_{AVDD,new}}{I_{AVDD,ref}} \approx 3.5.$$

Consequently, the target on-resistance must be reduced by the same factor, resulting in a required value of approximately 42 mΩ.

The design parameter modified to achieve the required on-resistance is the equivalent total width. As described by

$$R_{ON} \approx \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} \tag{4.3}$$

Therefore, increasing the total width by a factor of approximately 3.5 allows the target value of 42 mΩ to be achieved.

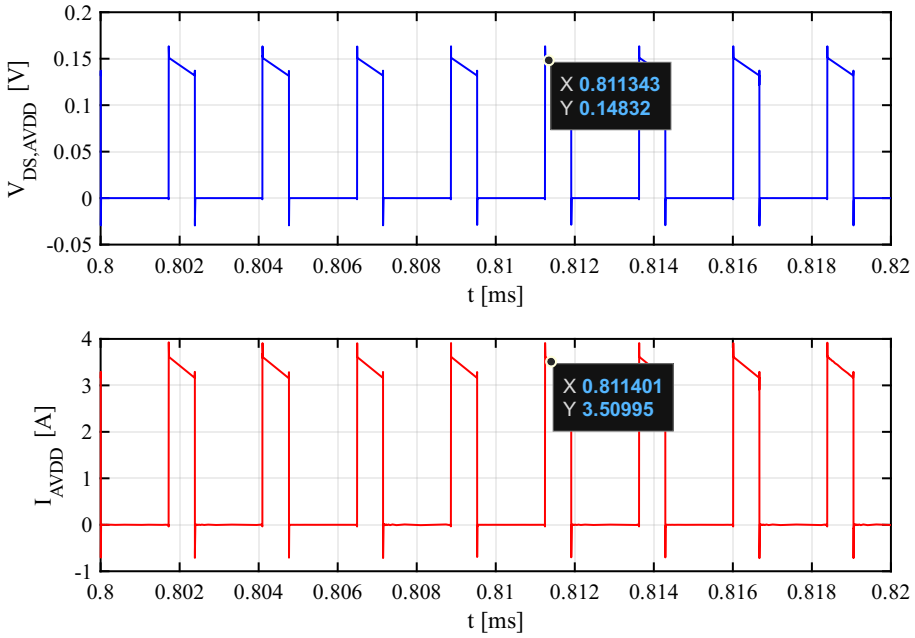


Figure 4.3: Isolation-switch current I_{AVDD} and voltage drop $V_{DS,AVDD}$ with modified total width after HVINP capacitor and pin removal

The obtained sizing is verified through circuit-level simulations (Fig. 4.3) by evaluating the ratio between the drain-to-source voltage and the current flowing through the isolation switch. The extracted on-resistance is found to be consistent with the expected value.

Compared to the reference implementation, the required total width increases by approximately 250%. The impact of this modification on the occupied layout area is discussed in the comparison of the investigated implementations.

3. **Lower-Voltage PMOS Implementation**

   In this step, the architecture introduced in the previous section is maintained, with the external capacitor C_1 removed from the HVINP node.

   As discussed in chapter 3.2, once the HVINP pin is removed, the maximum voltage stress experienced by the isolation switch is no longer determined by the converter output voltage, but instead by the maximum input voltage of the boost converter. Therefore, the isolation switch is implemented using a PMOS device, but its source-to-drain voltage rating can be reduced. Being the $V_{IN,max} = 5.5V$, the voltage rating is consequently reduced from 14 V to 7.5 V, still maintaining some voltage margin.

   Since the architecture remains unchanged, the current flowing through the isolation switch remains identical to that observed in the previous step. However, owing to its lower voltage rating, the adopted PMOS device exhibits a lower on-resistance per unit width. Consequently, for the same device dimensions as the previously used transistor, a smaller on-resistance is obtained.

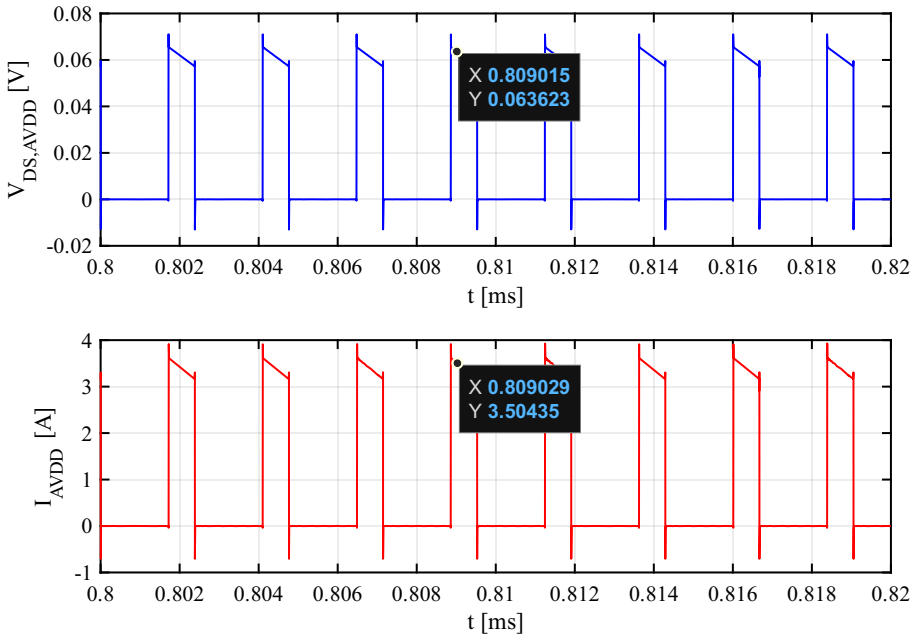


Figure 4.4: Current I_{AVDD} and voltage drop $V_{DS,AVDD}$ of Lower-Voltage PMOS isolation-switch with no size variation with respect to the modified 14V-PMOS in step 2

The effective on-resistance of the 7.5 V PMOS device is extracted from the simulation shown in fig. 4.4 by evaluating the ratio between the drain-to-source voltage and the current flowing through the transistor.

Since the current does not change, the sizing process is now based on maintaining the same on-resistance. The target value is chosen equal to the on-resistance obtained in the previous step, namely 42 mΩ. The ratio between the on-resistance extracted from this implementation and the target value is therefore used to determine the total transistor width required to restore the desired R_{ON}.

As a result, the required total transistor width corresponds to an increase of only 50% with respect to the reference implementation. Although the device remains larger than the original isolation switch, the resulting layout area is only approximately 26% greater than the reference case, representing a significant improvement compared to the high-voltage PMOS implementation of the previous step.

4. **NMOS Implementation**

The final design step consists of replacing the low-voltage PMOS isolation switch with an NMOS device having the same voltage rating of 7.5 V.

To enable a fair comparison with the previous implementation, a preliminary NMOS with the same size is placed to evaluate the effect of using this type of device on the R_{ON}.

As previously discussed (chap. 2.3), NMOS transistors provide a lower on-resistance per unit area and can achieve the same electrical performance with a smaller total transistor width.

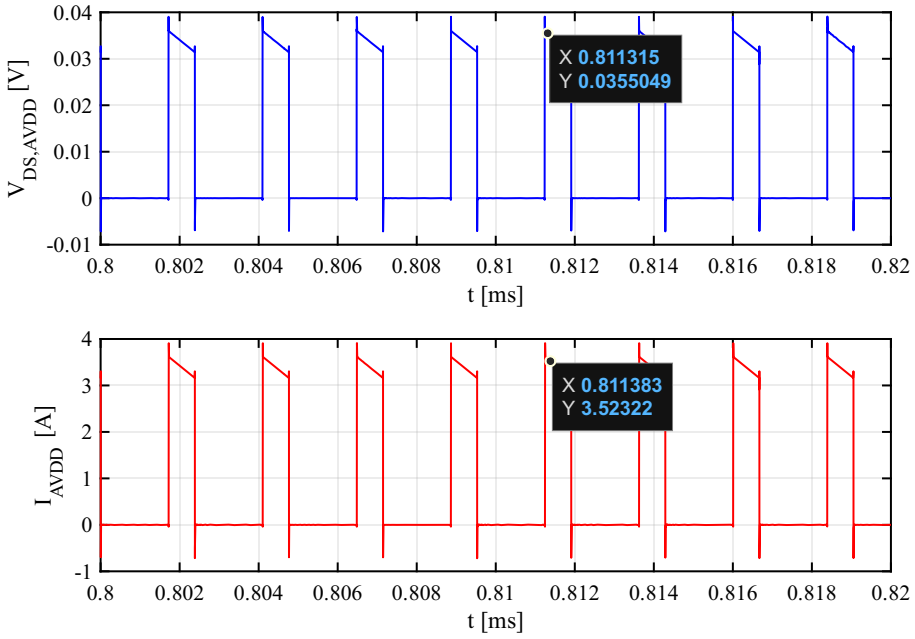


Figure 4.5: Current I_{AVDD} and voltage drop $V_{DS,AVDD}$ of Lower-Voltage NMOS isolation-switch with the same size as the modified 7.5V-PMOS in step 3

Extracting from the simulated drain-to-source voltage and current waveforms (Fig. 4.5), the effective on-resistance of the isolation switch is found to be smaller as the PMOS is replaced with an NMOS of the same width, as expected.

At this step, the required scaling factor for the transistor width is found in order to maintain the same target on-resistance as before (42 mΩ). Therefore, by evaluating the ratio between the extracted R_{ON} value and the target R_{ON} the required device sizing is determined.

The resulting implementation requires a total transistor width approximately 64% smaller than that of the reference high-voltage PMOS solution. In terms of layout occupation, this corresponds to an area reduction of approximately 71%, or equivalently to a 3.4× reduction with respect to the original implementation.

Among the investigated solutions, the lower-voltage NMOS implementation occupies the smallest silicon area while still meeting the same electrical requirements imposed on the isolation switch. For this reason, it represents the preferred implementation for the panel-supply scenario and constitutes the solution proposed in this work.

COMPARISON OF THE INVESTIGATED IMPLEMENTATIONS

The results obtained through the different sizing steps can now be compared in terms of occupied area.

Implementation	Ron [mΩ]	Total Width Variation	Area Variation
14V PMOS with pin	146	Reference	Reference
14V PMOS without pin	42	+250%	+250%
7.5V PMOS without pin	42	+50%	+26%
7.5V NMOS without pin	42	–64%	–71%

Table 4.2: Comparison of the investigated isolation-switch implementations for the panel supply application

Table 4.2 summarizes the variations in total transistor width and layout area obtained for the different implementations. The comparison highlights how the removal of the HVINP pin alone leads to a significant increase in the required device size, while the adoption of a lower-voltage-rated PMOS substantially mitigates this area penalty. Finally, replacing the PMOS isolation switch with an NMOS device provides the most area-efficient solution.

It should be noted that a variation in the total transistor width does not necessarily translate into an equivalent variation in layout area. For the large device dimensions considered in this work, the required total width is typically realized by means of multiple gate fingers replicated with a suitable multiplicity factor. In addition to the active device area, each finger requires diffusion regions and the minimum spacing imposed by the technology design rules.

As a consequence, the occupied area depends not only on the effective transistor width but also on the geometric arrangement of the fingers and on the gate pitch, defined as the center-to-center distance between adjacent gate fingers, which typically scales with voltage rating. For this reason, the relationship between total width and layout area is not strictly linear. In particular, a reduction in the required width may also reduce the number of fingers necessary to implement the device, resulting in area savings that can be larger than the width reduction itself.

To accurately evaluate the actual silicon-area impact of each solution, layout-level implementations have been developed for all investigated cases and are reported in Fig. 4.6.

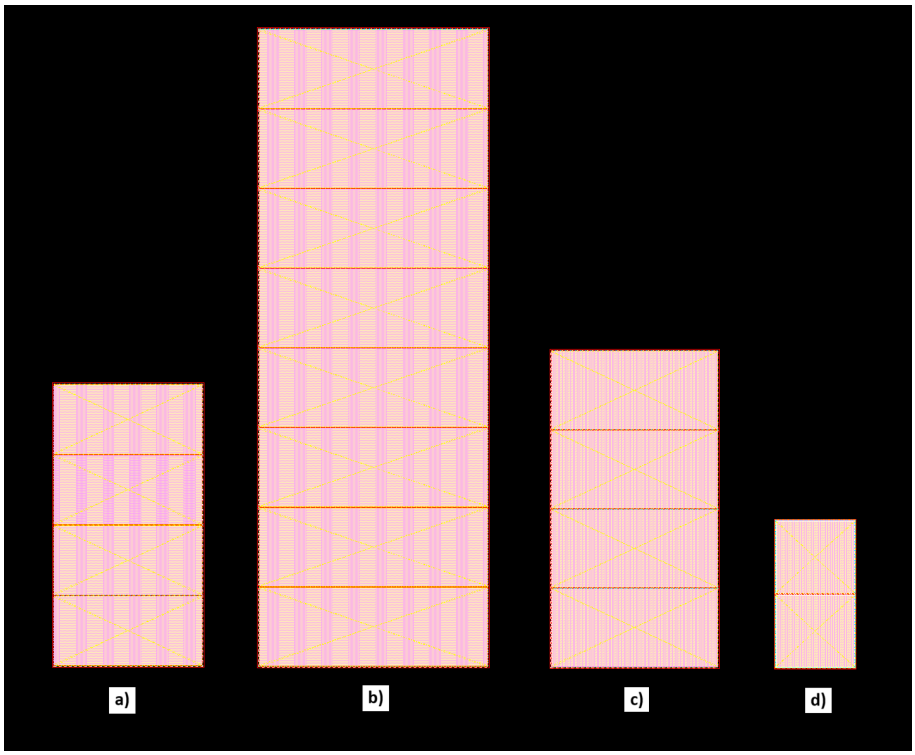


Figure 4.6: Layout comparison of the investigated isolation-switch implementations for the panel supply scenario: (a) 14V PMOS with pin, (b) 14V PMOS without pin, (c) 7.5V PMOS without pin, and (d) 7.5V NMOS without pin

The layout comparison visually confirms the conclusions drawn from Table 4.2. Among the investigated implementations, the low-voltage NMOS solution exhibits the most compact layout and achieves the largest area reduction, thus representing the preferred implementation for the panel-supply scenario.

4.3 Gate Driver Supply Scenario

The design process adopted for the gate-driver supply scenario follows the same methodology described for the panel-supply application. Therefore, the discussion is focused on the main differences introduced by the operating conditions of this scenario and on their impact on the isolation-switch sizing.

All simulations are performed under worst-case operating conditions, namely $V_{IN} = 2.8\,\mathrm{V}$, $V_{OUT} = 21\,\mathrm{V}$, and $I_{LOAD} = 100\,\mathrm{mA}$. Although the input-voltage range is identical to that considered for the AVDD supply, the significantly higher output voltage results in a much higher boost-converter conversion ratio. Consequently, the relationship between the output current and the current flowing through the isolation switch differs substantially from the previous scenario and directly affects the isolation-switch sizing process.

1. **Reference HV PMOS Implementation**

   As a first step, the original architecture is simulated in order to establish a reference for the subsequent comparisons. Due to the higher output-voltage

level required in this application, the isolation switch is implemented using a 28 V PMOS device, providing sufficient voltage margin with respect to the maximum output voltage.

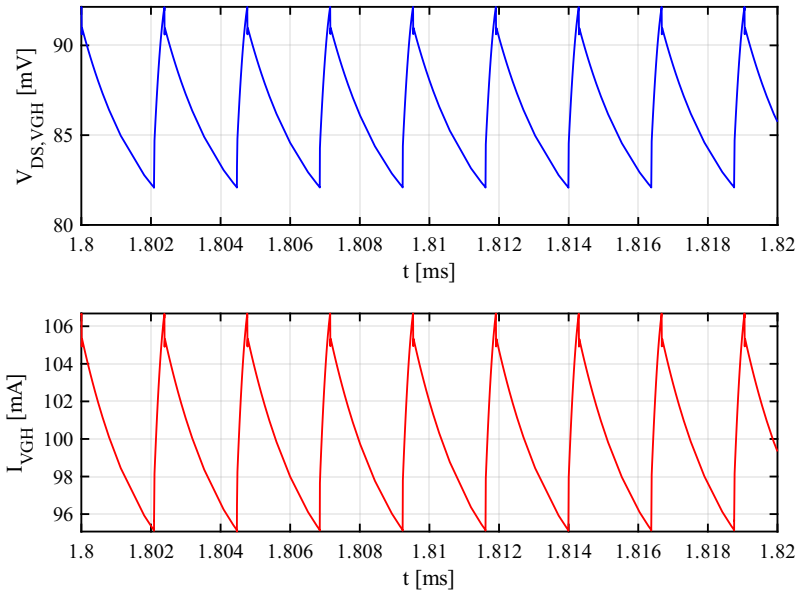


Figure 4.7: Isolation-switch current I_{VGH} and voltage drop $V_{DS,VGH}$ in the reference implementation

Figure 4.7 shows that the isolation switch, as expected, mainly conducts the load current and therefore carries an average current of approximately $\sim 100\,\text{mA}$.

Assuming operation in the triode region, the equivalent on-resistance is extracted from the simulated drain-to-source voltage and current according to

$$R_{ON} \approx \frac{V_{DS}}{I_{VGH}}$$

resulting in an equivalent on-resistance of approximately $860\,\text{m}\Omega$. This implementation is used as the reference for the following sizing steps.

2. **Impact of HVINP Pin Removal**

   As discussed throughout this work, removing the capacitor connected to the HVINP node modifies the current flowing through the isolation switch. In this case, the effect is significantly more pronounced than in the panel-supply scenario due to the much higher conversion ratio required by the boost converter.

   For an ideal boost converter, the input current scales with the conversion ratio, according to power conservation. Therefore, when generating 21 V from a minimum input voltage of 2.8 V, the isolation switch experiences a current increase that is substantially larger than the current variation in the AVDD scenario.

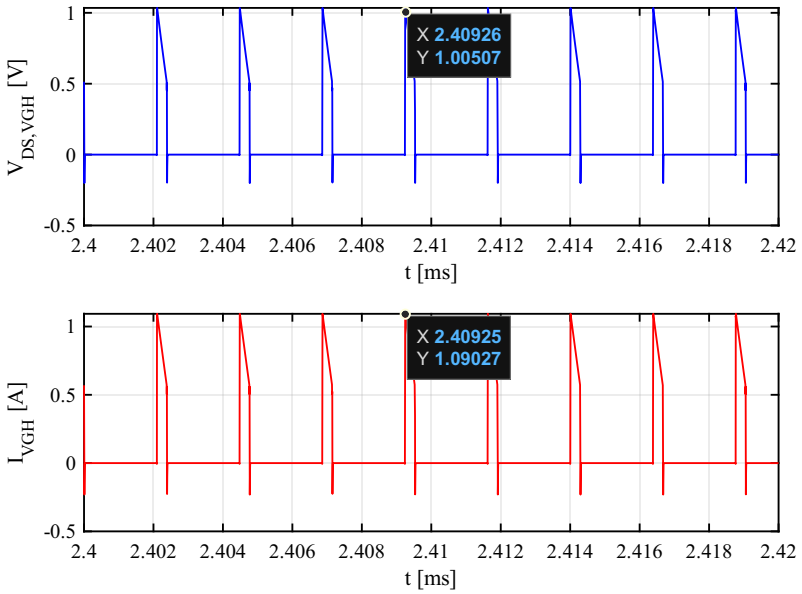


Figure 4.8: Isolation-switch current I_{VGH} and voltage drop $V_{DS,VGH}$ after removal of the HVINP pin and capacitor C1

The simulated current waveform is shown in Fig. 4.8. A peak current of approximately 1.09 A is observed, corresponding to an increase of about 10.9× with respect to the reference implementation. Since the same voltage-drop criterion adopted in the previous scenario is maintained, the target on-resistance must be reduced by the same factor.

Consequently, the total transistor width is increased by approximately 10.9×, resulting in a target on-resistance of approximately 80 mΩ.

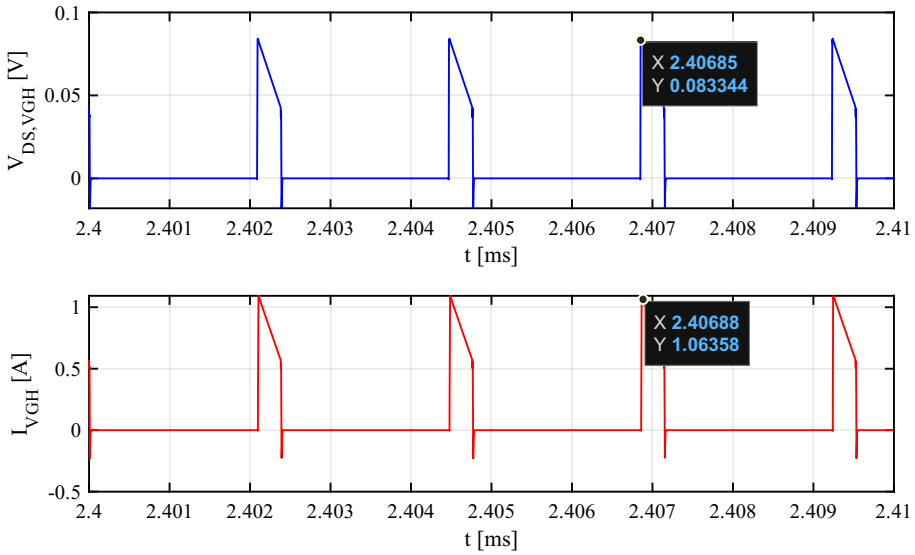


Figure 4.9: Isolation-switch current I_{VGH} and voltage drop $V_{DS,VGH}$ without the HVINP pin after scaling of the total transistor width

The resized implementation is then verified through simulation (Fig. 4.9), confirming the expected value of R_{ON}.

Despite the large layout-area increase of approximately 967% resulting from the higher current stress, this step provides the necessary baseline for evaluating the benefits introduced by the subsequent device optimizations.

3. **Lower-Voltage PMOS Implementation**

   In the next step, the isolation switch is replaced with a lower-voltage PMOS device since the proposed architecture limits the maximum voltage stress experienced by the isolation switch. A 14V PMOS was chosen as it represents the lowest-voltage-rated device available with a breakdown voltage compatible with the maximum output voltage of 21V. This ensures adequate reliability margins while enabling a reduction in device area compared to the 28V PMOS implementation.

   Because the circuit architecture remains unchanged, the current flowing through the isolation switch is identical to that observed in the previous step. As a consequence, the chosen target on-resistance is maintained at 80 mΩ.

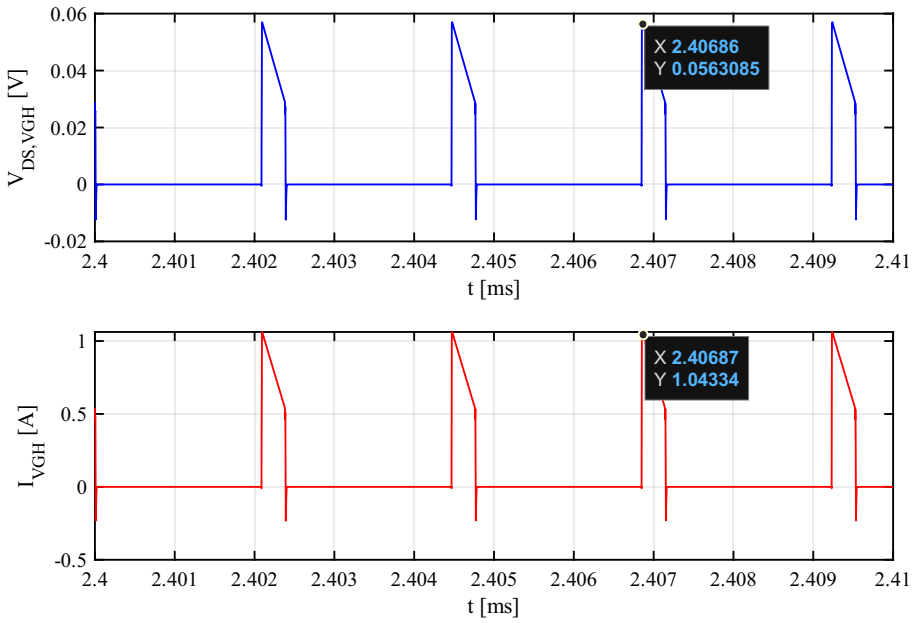


Figure 4.10: Current I_{VGH} and voltage drop $V_{DS,VGH}$ of Lower-Voltage PMOS isolation-switch with no size variation with respect to the modified 28V-PMOS in step 2

   Simulation results show that, given the same total width, the lower-voltage PMOS exhibits a reduced on-resistance per unit width compared to the 28 V device. Therefore, the corresponding sizing factor required to achieve the target R_{ON} leads to a significant reduction in occupied area with respect to the previous step. However, the resulting device still occupies an area approximately 339% larger than the reference solution.

4. **NMOS Implementation**

The final sizing step consists of replacing the 14 V PMOS isolation switch with an NMOS device having the same voltage rating.

As discussed previously, NMOS transistors provide a lower on-resistance per unit area than equivalent PMOS devices.

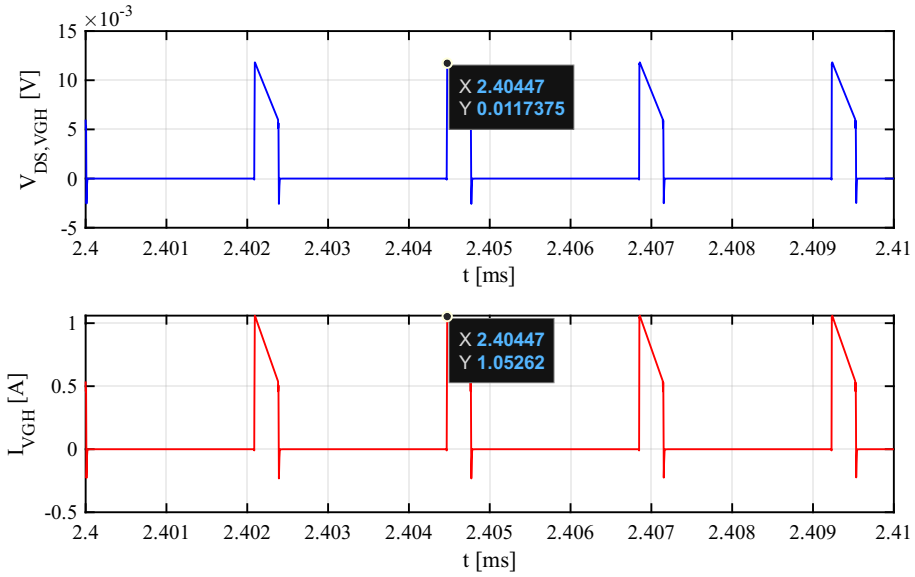


Figure 4.11: Current I_{VGH} and voltage drop $V_{DS,VGH}$ of Lower-Voltage NMOS isolation-switch with the same size as the modified 14V-PMOS in step 3

The R_{ON} extracted from the simulation shown in fig. 4.11 confirms that the NMOS implementation can achieve the target on-resistance of 80 mΩ with considerably smaller dimensions than the corresponding PMOS solution.

The resulting device is obtained with a total width similar to that of the reference implementation. Nevertheless, as discussed in Section 4.2, total width and layout area are not directly proportional. The more efficient finger-gate arrangement available for the NMOS implementation allows a more compact layout realization, leading to an area reduction of approximately 35% with respect to the reference solution.

COMPARISON OF THE INVESTIGATED IMPLEMENTATIONS

The results obtained from the isolation-switch sizing analysis for the VGH generation scenario are summarized in Table 4.3.

Implementation	Ron [mΩ]	Total Width Variation	Area Variation
28V PMOS with pin	860	Reference	Reference
28V PMOS without pin	80	+988%	+967%
14V PMOS without pin	80	+644%	+339%
14V NMOS without pin	80	+2%	-35%

Table 4.3: Comparison of the investigated isolation-switch implementations for the gate-driver supply application

The comparison confirms the trends highlighted throughout the analysis. The removal of the HVINP pin introduces a significantly larger current increase than in the panel-supply scenario, resulting in a more stringent sizing requirement for the isolation switch. Nevertheless, adopting lower-voltage devices and ultimately replacing the PMOS with an NMOS progressively reduces the associated area penalty.

This result highlights a key difference with respect to the AVDD scenario. In the VGH application, the substantial increase in current caused by the removal of the HVINP pin largely offsets the area savings introduced by the adoption of a lower-voltage device and by the NMOS implementation. As a consequence, the area reduction achieved by the NMOS solution is less pronounced than that observed in the panel-supply scenario.

Nevertheless, the proposed implementation still enables the architectural benefits associated with the removal of the external HVINP pin to be retained. Therefore, even though the NMOS device provides a smaller area advantage than in the AVDD case, the overall solution remains beneficial.

This conclusion is further supported by the layout comparison shown in Fig. 4.12, where the relative area occupied by the different isolation-switch implementations can be directly observed.

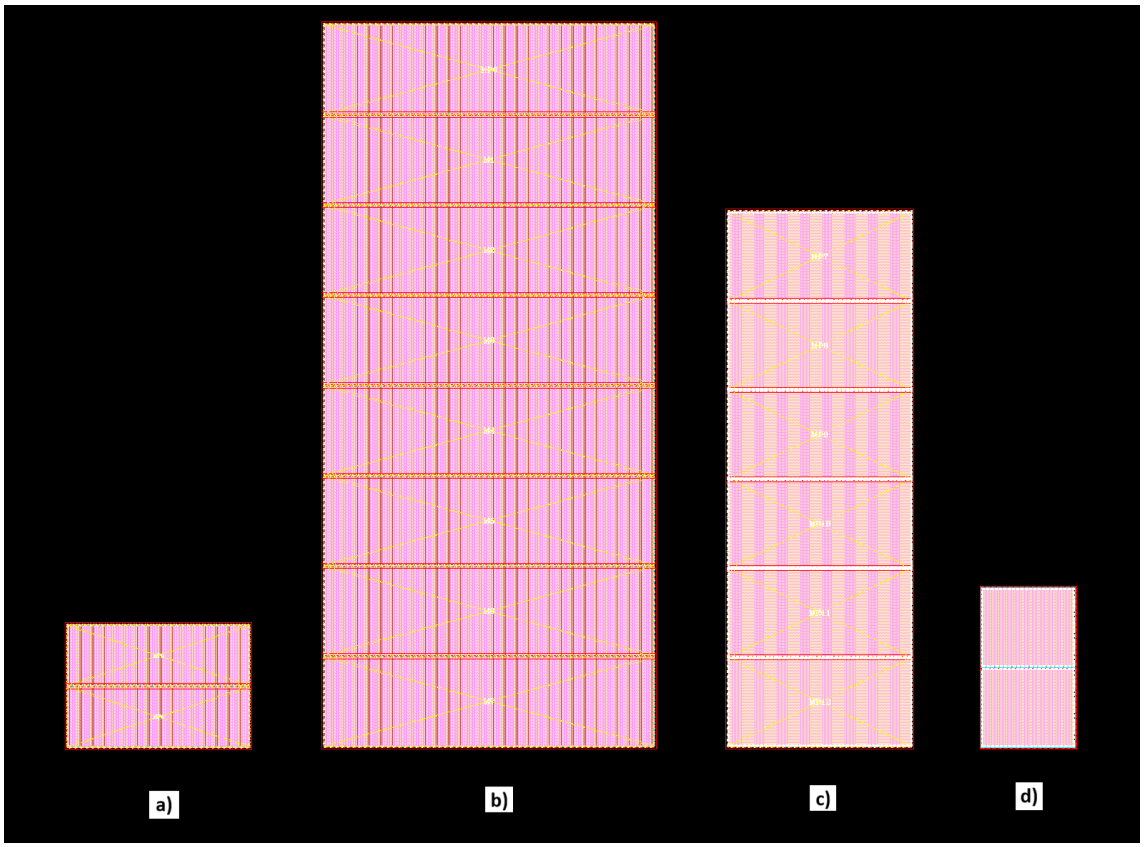


Figure 4.12: Layout comparison of the investigated isolation-switch implementations for the gate-driver supply scenario: (a) 28V PMOS with pin, (b) 28V PMOS without pin, (c) 14V PMOS without pin, and (d) 14V NMOS without pin

In conclusion, the analyses presented in this chapter confirm the initial hypothesis that the proposed architecture, with respect to the original implementation, provides an area advantage based on using a lower-voltage NMOS isolation switch and removing the externally accessible HVINP pin.

Having identified the preferred isolation-switch implementation, the next step is to investigate its practical integration within the converter, with particular focus on the required gate-driving and protection circuitry.

Chapter 5

Isolation Switch Circuitry detailed Functional Analysis and Simulations

In the original implementation, the isolation switch is driven by a dedicated control circuitry that also provides a current-limiting function. Besides generating the gate-to-source voltage required to control the device, the driver regulates the maximum current flowing through the isolation switch. As the switch conducts the load current, this mechanism directly limits the current supplied to the output, providing protection against overload conditions.

In the architecture proposed in this work, the isolation switch is required to conduct a significantly larger current than in the original implementation, as it now carries the boost-converter current. As discussed in Section 3.1, the boost converter inherently includes a current-limiting function. Nevertheless, the increased current level associated with the isolation switch makes the implementation of a dedicated current-limiting mechanism within the driver particularly relevant. In this context, the driver operates not only as a gate-control circuit but also as a protection block to avoid device degradation or failure under abnormal operating conditions.

As a first step toward the design of a new driver suitable for the proposed NMOS-based solution, a detailed functional analysis of the existing PMOS driving circuitry is carried out. Understanding the operating principles of the original implementation provides a valuable reference for the development of the new architecture and helps identify the key parameters that must be reconsidered when transitioning from a PMOS to an NMOS isolation switch.

This chapter therefore describes the operation of the existing driver circuit and validates its functionality through simulation results. Particular attention is devoted to the current-limiting mechanism and to the design parameters that differ from those required by the proposed solution.

5.1 Functional analysis of the reference driver implementation

A driver circuit for the PMOS isolation switch, including the current-limiting functionality, is shown in Fig. 5.1.

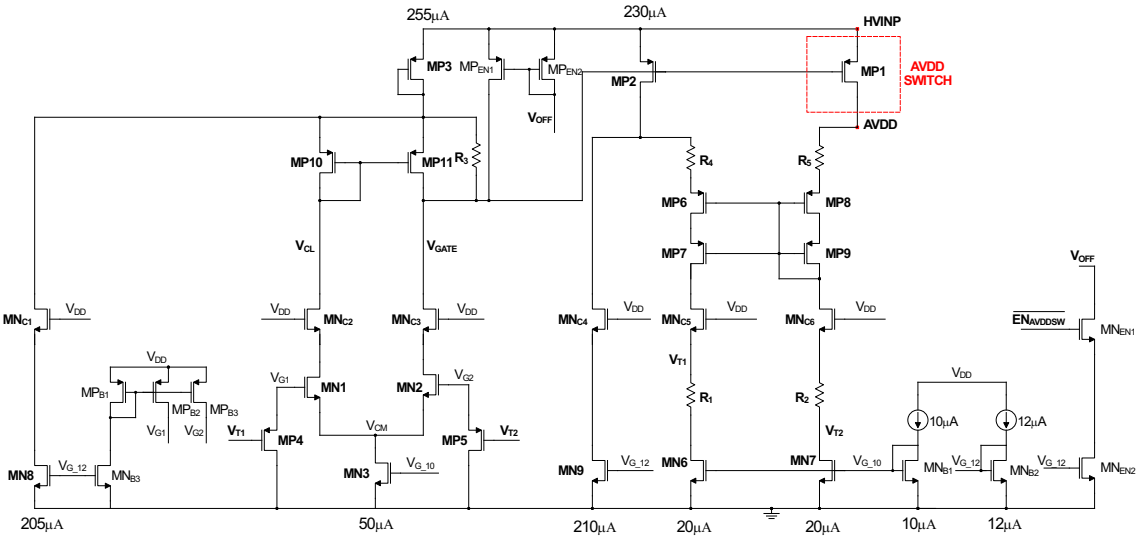


Figure 5.1: Transistor-level schematic of the PMOS isolation-switch driver with integrated current-limiting function

The isolation switch, identified as MP1, is located in the upper-right portion of the schematic. The fundamental principle of the circuit is the regulation of the gate-to-source voltage of MP1. By controlling the value of V_{SG}, the driver determines the conduction state of the isolation switch and regulates the current delivered to the load.

For clarity, the circuit can be divided into four main functional blocks:

- the bias generation circuitry;
- the enable circuitry;
- the current-sensing and comparison stage;
- the gate-control stage.

The operation of each block is described before analyzing the overall circuit behavior.

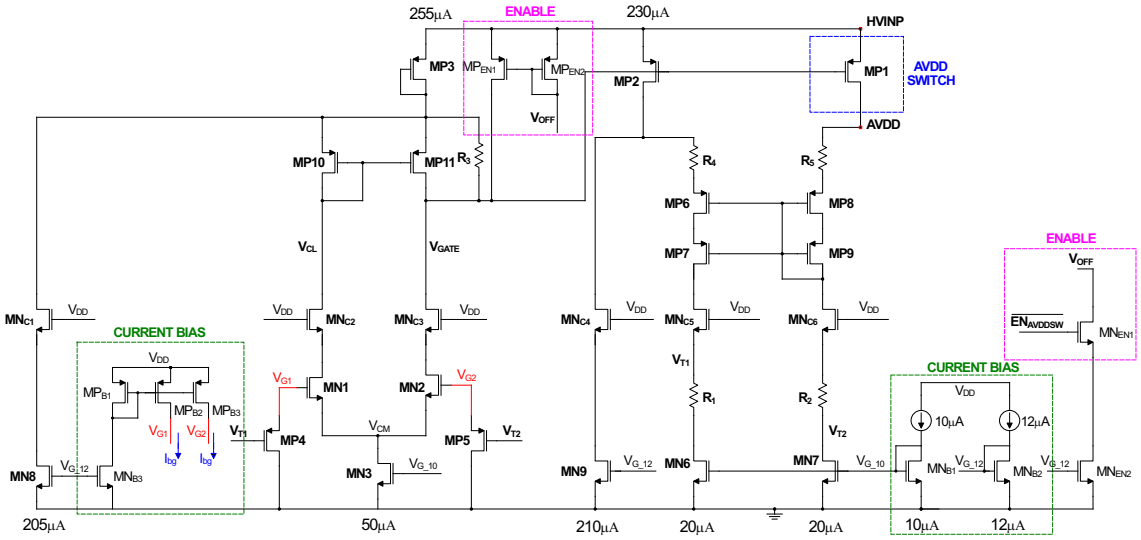


Figure 5.2: Transistor-level schematic of the PMOS isolation-switch driver with the bias generation and enable functional blocks highlighted

As highlighted in Fig. 5.2, transistors MN_{B1} and MN_{B2} generate mirrored bias currents of $10\,\mu A$ and $12\,\mu A$, respectively. In addition, transistors MN_{B3}, MP_{B1}, MP_{B2}, and MP_{B3} provide the current I_{bg} used to bias the branches containing $MP4$ and $MP5$. These currents establish the operating point of the sensing and control circuitry and remain active in both the normal and current-limit operating conditions.

The enable function is implemented by transistors MN_{EN1}, MN_{EN2}, MP_{EN1} and MP_{EN2}. When the signal EN_{AVDDSW} is low, its complementary version $\overline{EN}_{AVDDSW}$ becomes high, turning on MN_{EN1}. The current flowing through MN_{EN1} is mirrored by MP_{EN2} onto the branch containing MP_{EN1}.
As a consequence, the conducting transistor MP_{EN1} pulls the gate node of MP1close to the HVINP potential, resulting in a negligible gate-to-source voltage,

$$V_{SG} = V_{HVINP} - V_{GATE} \approx 0.$$

Under this condition, the isolation switch is turned off.

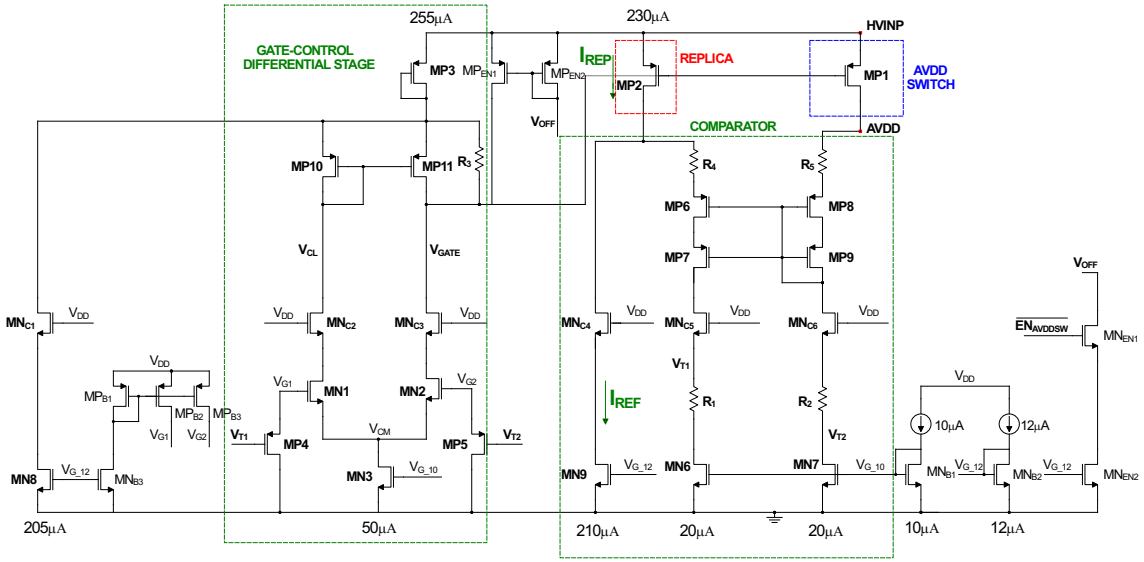


Figure 5.3: Transistor-level schematic of the PMOS isolation-switch driver with the current-sensing and comparator stage and gate-control stage highlighted

The active control circuitry can be divided into two main stages, as shown in Fig. 5.3. The first stage monitors the current flowing through the isolation switch and determines whether it exceeds a predefined threshold. The second stage generates the gate voltage required to establish the appropriate value of V_{SG}, thereby controlling the operating condition of the isolation switch.

Current monitoring is performed by means of a scaled replica of the isolation PMOS transistor. The replica device, denoted as MP2, is scaled down by a factor n with respect to the main switch MP1. The purpose of this replica is to reproduce the operating conditions of the isolation switch, and in particular its drain-to-source voltage. To achieve this, both transistors share the same source voltage, $HVINP$, and are driven by the same gate voltage, V_{GATE}. In addition, a current corresponding to the current-limit value scaled down by the factor n must be imposed in the replica branch.

More specifically, the branch containing $MN9$ carries a reference current I_{REF}, generated by the current mirror based on MN_{B2} with the appropriate mirror ratio. This current is selected to bias the replica transistor MP2 at the operating point corresponding to the desired current-limit condition of the isolation switch. Therefore, I_{REF} establishes the comparator threshold and sets the current level at which the circuit recognizes that the programmed current limit has been reached.

In this architecture, the PMOS conducts the load current. Therefore, its maximum current is approximately equal to the maximum load current, $I_{LOAD,max} \approx 1\,\mathrm{A}$. The current limit is set to a slightly higher value of approximately 1.4A in order to provide some design margin. Accordingly, I_{REF} is selected such that, under current-limit conditions, the current flowing through the replica transistor MP2 is

$$I_{REP,LIM} = \frac{I_{AVDD,max}}{n}.$$

By properly selecting I_{REF}, the comparator stage, formed by the R_4 and R_5

branches, is able to determine whether the isolation switch is operating below the programmed current limit or has entered the current-limit condition. The resulting voltages V_{T1} and V_{T2} are then used to steer the differential gate-control stage, which establishes the appropriate gate-bias conditions for each operating mode.

Having described the function of the different circuit blocks, the operation of the driver can now be analyzed under its two possible operating conditions. In the following sections, the behavior of each functional block is examined in order to understand how the circuit generates the gate voltage of the isolation switch and how it transitions between normal operation and current-limit operation.

- **Typical V_{SG} generation**

  The typical operating condition is analyzed first, starting from the operation of the first stage, shown in Fig. 5.4.

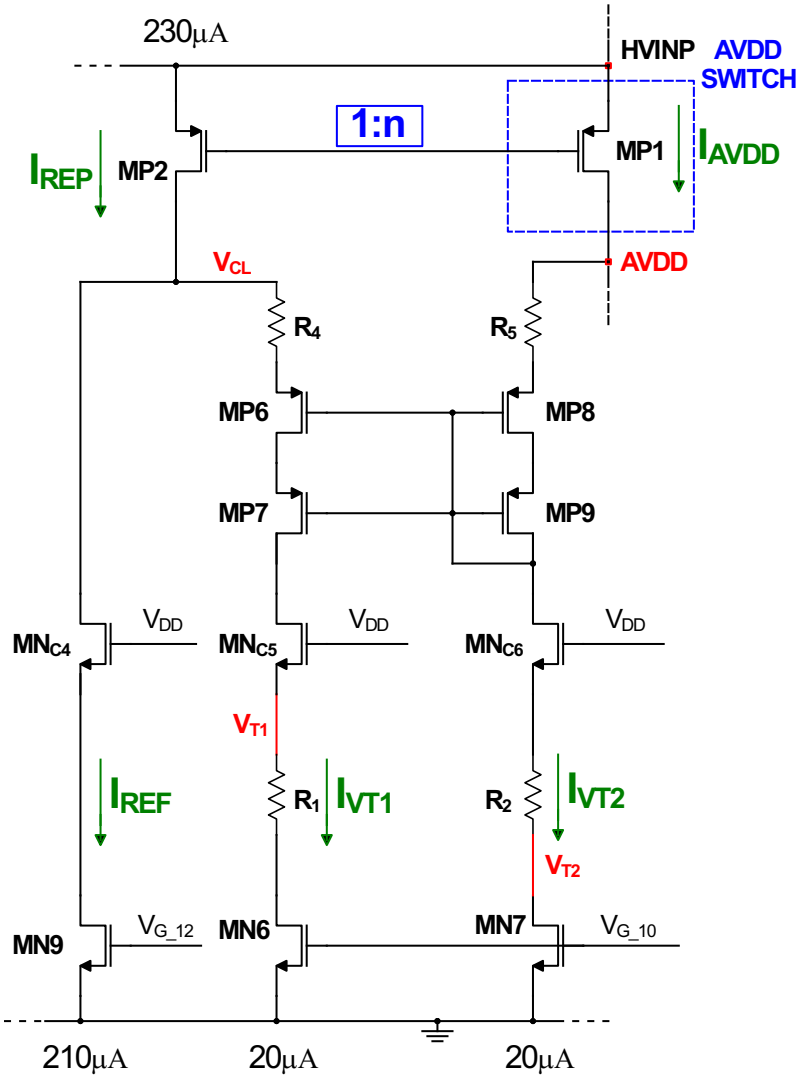


Figure 5.4: Replica and comparator stage of the PMOS isolation-switch driver in typical operation

The operating voltage range of this stage extends from ground up to the

HVINP voltage, which can reach approximately 10 V. Therefore, transistors MN_{C4}, MN_{C5}, and MN_{C6} are used as cascode devices. By absorbing most of the voltage associated with the high-voltage node $HVINP$, these devices reduce the drain-to-source voltage applied to the underlying transistors $MN9$, $MN6$, and $MN7$, ensuring that they remain within their voltage-rating limits while operating correctly over the entire input-voltage range.

The V_{T1} and V_{T2} branches are biased by mirroring a 20 μA current into $MN6$ and $MN7$, respectively, starting from the bias transistor MN_{B1} (Fig. 5.2).

When the isolation transistor MP1 is enabled, it conducts the current I_{AVDD}, resulting in a voltage drop across the device

$$V_{DS,AVDD} = I_{AVDD} \cdot R_{ON,MP1}$$

As the current increases, the voltage drop increases as well. In other words, the voltage at node HVINP increases as the current through the isolation switch increases.

As previously discussed, I_{REF} is selected such that the replica transistor $MP2$ reproduces the drain-to-source voltage that MP1 would exhibit under current-limit conditions

$$V_{DS,REP} = V_{DS,AVDDmax} = HVINP – I_{REF} \cdot R_{ON,MP2}.$$

This allows the drain voltage of MP2, denoted as V_{CL}, to be used as the comparator threshold.

Under normal operating conditions, AVDD remains higher than V_{CL}. As a consequence, the source voltage of PMOS transistors MP8 and MP9 is higher than that of MP6 and MP7.

A key aspect of the circuit operation is that transistor MP7 is driven by the gate voltage of the diode-connected transistor MP9. When AVDD is higher than V_{CL}, and therefore the drain voltage of MP9 is sufficiently high, MP7 is pushed toward its turn-off region. This occurs because the voltage applied to the gate of MP7, equal to $V_{D,MP9}$, becomes high enough to reduce the source-to-gate voltage of MP7 below its threshold voltage.

As a result, the current imposed through the mirror is correctly conducted in the MP9 branch, where all transistors operate in saturation. Conversely, when transistor MP7 is in the off state, transistor MN6 is forced into the triode region, where it no longer mirrors the imposed bias current.

As a direct consequence, the voltage V_{T1} is pulled toward ground. Considering MN6 operating in the linear region, where $V_{DS,MN6} \ll V_{OV,MN6}$, its drain current can be approximated as

$$I_{VT1} \approx \beta_6 \left(V_{GS,MN6} - V_{TH}\right) V_{DS,MN6} \tag{5.1}$$

where $\beta_6 = \mu_n C_{ox}(W/L)_6$, with μ_n denoting the electron mobility, C_{ox} the gate-oxide capacitance per unit area, and $(W/L)_6$ the transistor aspect ratio, while V_{TH} is the threshold voltage.

Therefore,

$$V_{DS,N6} \approx \frac{I_{VT1}}{\beta_6 \left(V_{GS,N6} - V_{TH}\right)},$$

and the voltage V_{T1} can be expressed as

$$V_{T1} \approx \frac{I_{VT1}}{\beta_6 \left(V_{GS,N6} - V_{TH}\right)} + I_{VT1} R_1 \tag{5.2}$$

On the other hand, V_{T2} can be determined starting from the gate voltage of MN_{C6}. Under the assumption of saturation operation, the resulting voltage at node V_{T2} is given by

$$V_{T2} = V_{DD} - V_{TH,MNC6} - V_{OV,MNC6} - I_{20\mu A} R_2. \tag{5.3}$$

Since $I_{VT1} \ll I_{VT2}$ in this operating mode, the resulting voltage V_{T2} settles to a value significantly higher than V_{T1}. These voltages constitute the outputs of the comparator stage and are used as inputs to the differential stage to establish the operating condition of the isolation PMOS switch.

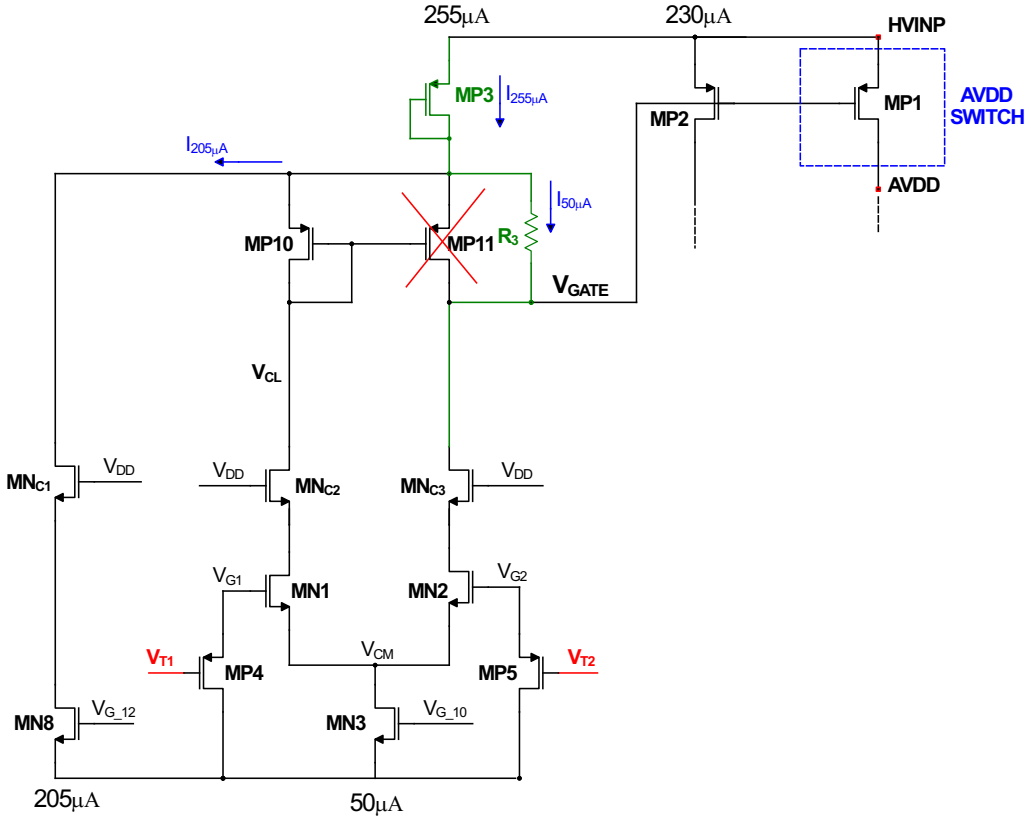


Figure 5.5: Gate-control differential stage of the PMOS isolation-switch driver in typical operation

Figure 5.5 shows the second stage of the circuit. Transistors MN_{C1}, MN_{C2}, and MN_{C3} are cascode and provide the same function as MN_{C4}, MN_{C5}, and MN_{C6} in the previous stage.

Transistor MN3 mirrors a current of $50\,\mu$A, while transistor MN8 mirrors a current of $205\,\mu$A into a branch parallel to the differential stage. At the top of the schematic, a diode-connected PMOS transistor, MP3, has its source connected to $HVINP$. MP3 is sized identically to MP2 and therefore serves as a scaled replica of the main isolation transistor MP1, with the same scaling factor n used for MP2.

Signals V_{T1} and V_{T2} drive PMOS transistors MP4 and MP5, which act as level shifters, translating the voltages V_{T1} and V_{T2}, respectively, toward the higher common-mode level required by the gate-control stage. As a result, the voltages V_{G1} and V_{G2} follow V_{T1} and V_{T2} with an approximately constant offset equal to the source-to-gate voltage of MP4 and MP5:

$$V_{G1,2} = V_{T1,2} + V_{SG,MP4,5}.$$

In the typical operating scenario, where $V_{T2} > V_{T1}$, the differential pair becomes unbalanced and steers essentially all the tail current provided by MN3 into the branch containing MN2.

As a consequence, negligible current flows through MN1. Therefore, MP10 does not mirror current into MP11, causing MP11 to become a high-impedance device. In the parallel network formed by R_3 and MP11, the effect of MP11 becomes negligible, and the entire tail current flows through resistor R_3.

The $50\,\mu$A current flowing through R_3 combines with the $205\,\mu$A current provided by MN8, resulting in a total current of $255\,\mu$A flowing through MP3. Since MP3 is diode-connected ($V_{SD,MP3} = V_{SG,MP3}$), the gate-to-source voltage established on MP1 is therefore given by

$$V_{SG,MP1} = HVINP - V_{GATE} = V_{SG,MP3} + R_3 \cdot I_{50\mu A}.$$

Accordingly, R_3 is dimensioned such that a gate-to-source voltage of approximately 1.5 V is established across MP1, thereby maintaining the isolation switch in the required operation region during normal boost-converter operation.

- **Current-Limit Operation**

  Let us now analyze the circuit behavior when the current flowing through MP1 starts increasing and reaches the maximum value that must be enforced by the current-limiting function.

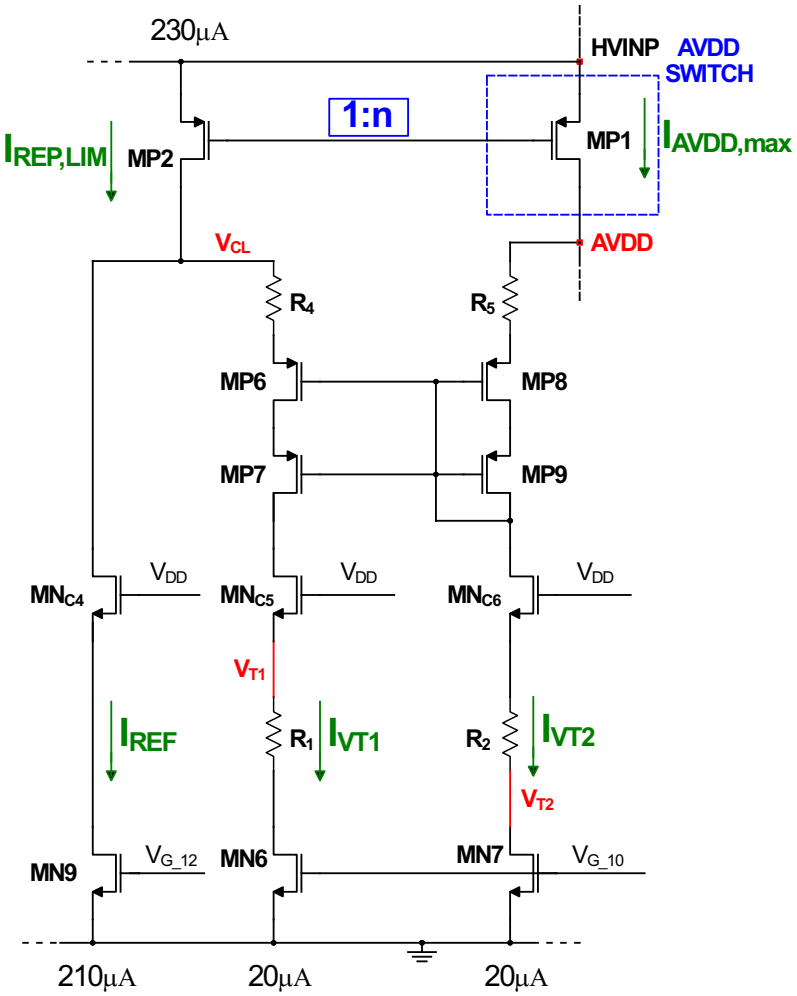


Figure 5.6: Replica and comparator stage of the PMOS isolation-switch driver in current-limit condition

As shown in Fig. 5.6, under current-limit conditions the isolation switch MP1 conducts a current $I_{AVDD,max}$, which generates a drain-to-source voltage drop $V_{DS,AVDD,max}$ across the device.

As discussed previously, the current flowing through MP2 is scaled such that the transistor reproduces the voltage drop $V_{DS,AVDD,max}$ associated with the current-limit condition. As the circuit enters the current-limit condition and the current through MP1 increases, the corresponding increase in $V_{DS,AVDD}$ raises the $HVINP$ potential relative to $AVDD$. Since V_{CL} follows the HVINP potential through MP2, it is pulled upward until the condition $AVDD < V_{CL}$ is reached, indicating that the current-limit threshold has been reached.

The resulting increase in $V_{SG,MP7}$ eventually drives the transistor above threshold, causing MP7 to turn on.

In this operating condition, both MN6 and MN7 operate in saturation and conduct the same current of 20 μA, imposed by the current mirror. Resistors

R_1 and R_2 are intentionally chosen with identical values so that the voltage drops across them $I_{VT1}R_1$ and $I_{VT2}R_2$ are equal when $I_{VT1} = I_{VT2}$.

As a result, the balance between the two branches is reversed with respect to the previous operating condition, leading to $V_{T1} > V_{T2}$. This change in the relative values of V_{T1} and V_{T2} indicates that the current threshold has been exceeded and activates the subsequent current-limiting action.

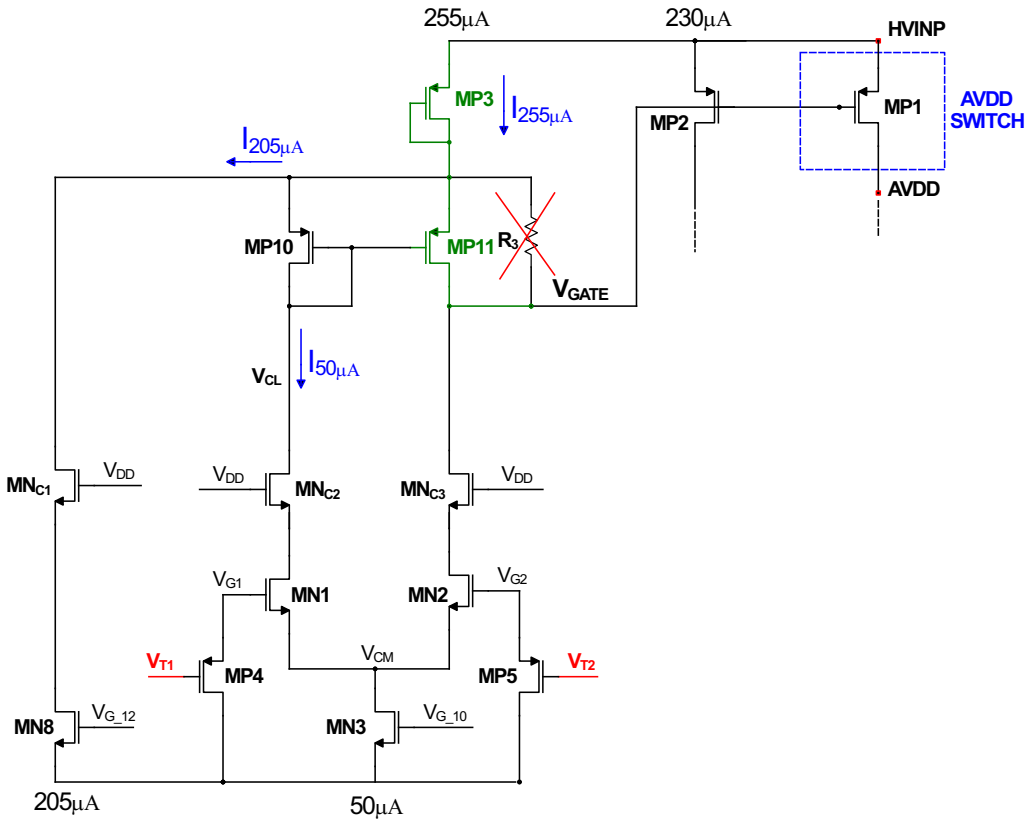


Figure 5.7: Gate-control differential stage of the PMOS isolation-switch driver in current-limit condition

In the second stage, under current-limit conditions, the operation shown in Fig. 5.7 takes place.

The voltages V_{T1} and V_{T2} unbalance the differential pair, steering most of the tail current into the branch containing MN1. As a result, MP10 conducts a current of $50\,\mu$A, which is mirrored to transistor MP11. MP11 is appropriately sized so that, at this current level, the drain-to-source voltage $V_{DS,MP11}$ remains negligible, on the order of a few mV.

Since MP11 therefore behaves as a very low impedance, the voltage drop across resistor R_3 can be neglected and MP11 can be approximated as a pseudo short-circuit. Consequently, the source-to-gate voltage used to drive MP1 is approximately determined only by $V_{SG,MP3}$.

As discussed previously, MP3, similarly to MP2, acts as a replica of MP1. More specifically, MP3 is biased so as to generate the value of V_{SG} that, when applied to the AVDD switch ($V_{SG,MP1} = V_{SG,MP3}$), biases the device to conduct its maximum allowable current, thereby implementing the current-limiting function.

To achieve this condition, MP3 must be biased with a current corresponding to the current-limit threshold scaled by the replica factor n. A current of $205\,\mu$A is generated by MN8 and added to the $50\,\mu$A tail current of the differential pair. As a result, MP3 conducts a total current of $255\,\mu$A, which is greater than the value of $I_{REP,LIM} = I_{AVDD,max}/n$ used by the first stage to detect the onset of the current-limit condition.

This choice is motivated by stability considerations. If MP3 were biased with exactly the same current used to generate the reference voltage across MP2, the detection threshold and the regulation threshold would coincide. In this situation, even a small variation of $V_{SG,MP1}$ could reduce the current through MP1 slightly below the current-limit threshold, causing the circuit to exit the current-limit state. The resulting feedback action would then drive the circuit back into current limit, leading to continuous transitions around the operating point.

By intentionally biasing MP3 with a current larger than that used in MP2, a margin is introduced between current-limit detection and current-limit regulation. As a result, small perturbations around the operating point do not cause unwanted transitions and ensures stable operation once the current-limit condition has been reached.

Therefore, the second stage not only enforces the desired current limit on the isolation switch, but also guarantees a robust and stable current-limiting operation in the presence of process variations and operating-point fluctuations.

In order to validate the operation of the proposed architecture, the complete driving and current-limiting circuitry, together with the isolation switch, was integrated into the boost-converter model. The resulting system was subsequently evaluated through transistor-level simulations. The simulation results presented in the next section confirm the behavior described above and demonstrate the correct operation of the proposed current-limiting scheme under both operating conditions.

5.2 Simulations

The operation of the proposed architecture was first verified under typical boost-converter operating conditions through transistor-level simulations performed on the schematic shown in Fig. 5.1. The simulations were carried out with $V_{IN} = 2.8\,\mathrm{V}$, $AVDD = 10\,\mathrm{V}$, and $I_{LOAD} = 500\,\mathrm{mA}$.

Under these conditions, the behavior of the first stage is analyzed.

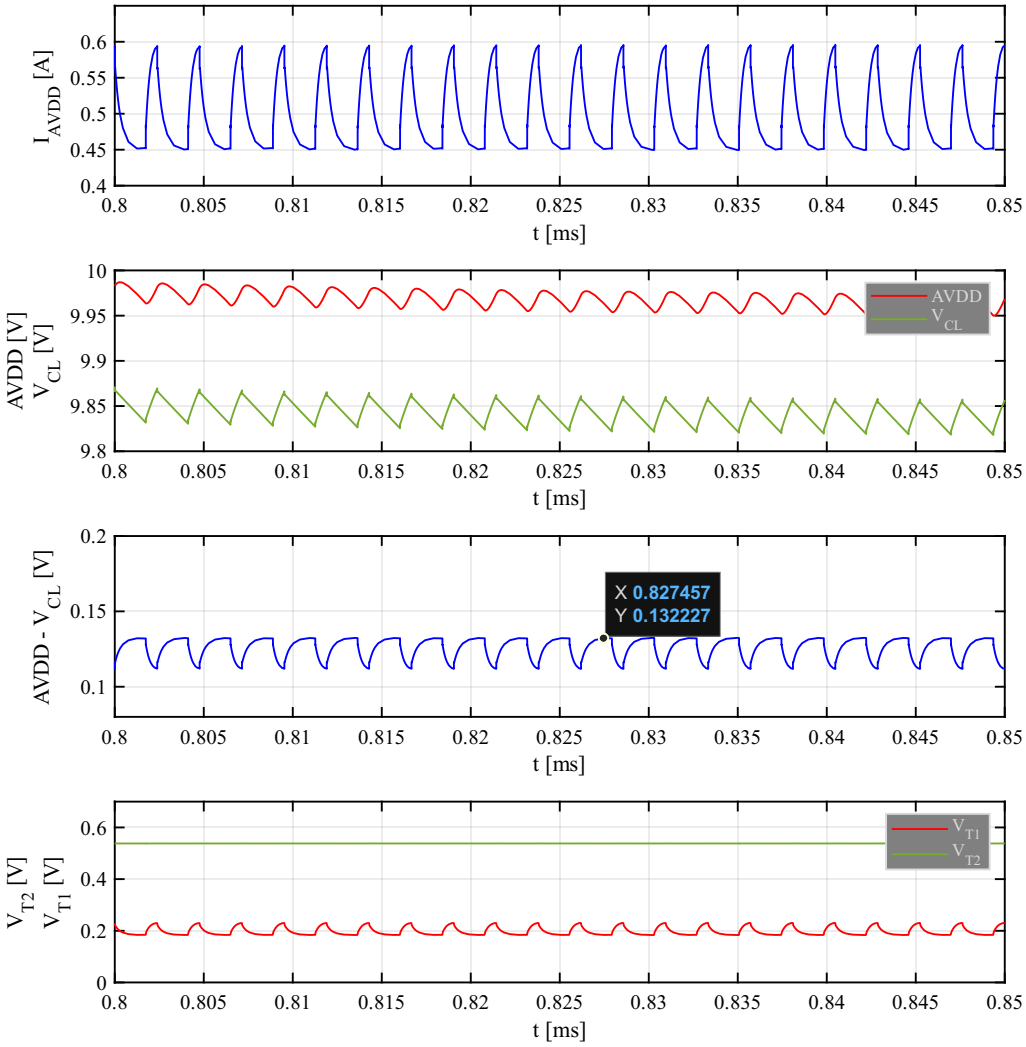


Figure 5.8: Simulation results of the PMOS driver under typical operating conditions, displaying the steady-state waveforms of the AVDD-switch current I_{AVDD}, the output voltage $AVDD$, the MP2 drain voltage V_{CL}, the voltage difference $AVDD - V_{CL}$, and the comparator-stage output voltages V_{T1} and V_{T2}

Fig. 5.8 shows that, when transistor MP1 is not operating in current-limit conditions, the AVDD voltage remains above the threshold voltage V_{CL}. As highlighted by the waveform $AVDD - V_{CL}$, the positive voltage difference results in the operating condition described in Section 5.1, where the comparator generates the signals V_{T1} and V_{T2} such that $V_{T2} > V_{T1}$.

The behavior of the second stage is confirmed by the simulation shown in Fig. 5.9.

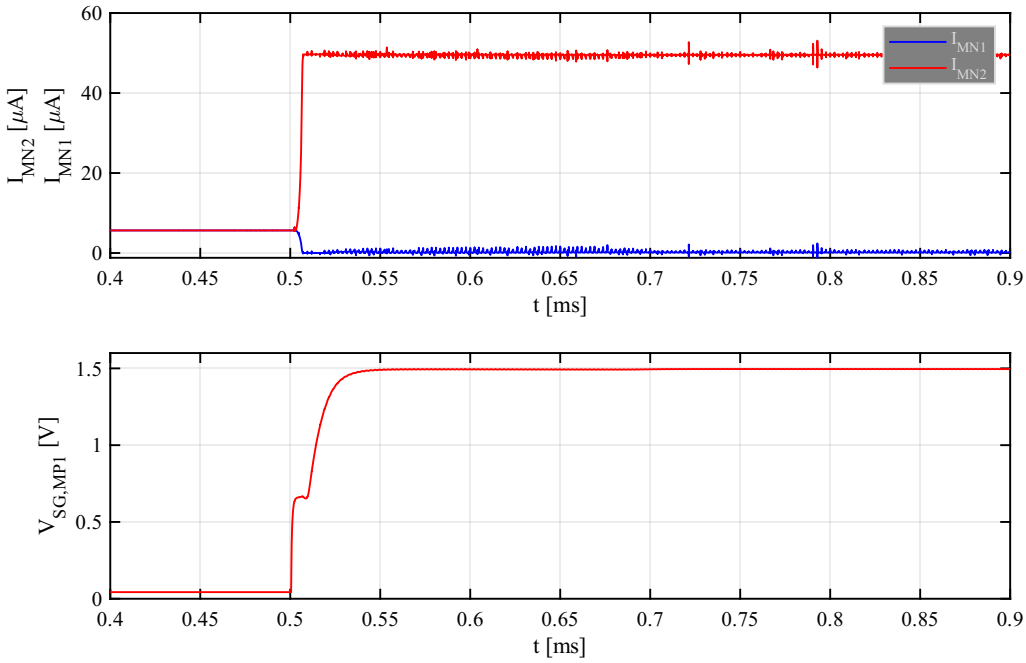


Figure 5.9: Simulation results of the PMOS driver under typical operating conditions, displaying the AVDD-switch source-to-gate driving voltage $V_{SG,MP1}$ and the steady-state waveforms of the current flowing in differential stage branches I_{MN1} and I_{MN2}

The unbalance between V_{T1} and V_{T2} steers the entire tail current ($50\,\mu$A) into transistor MN2, while the current through MN1 is approximately zero. The figure also shows that, with the proper sizing of R_3 (Fig. 5.5), the resulting source-to-gate voltage driving the isolation switch MP1 is approximately 1.5 V during normal operation.

The circuit was subsequently simulated under current-limit conditions by setting $V_{IN} = 2.8\,\text{V}$, $AVDD = 10\,\text{V}$, and $I_{LOAD} = 2\,\text{A}$. Under these operating conditions, the current-limiting function is expected to act so as to reduce the current flowing through the AVDD switch, which would otherwise tend to reach the current requested by the load.

The operation of the first stage under current-limit conditions is shown in Fig. 5.10.

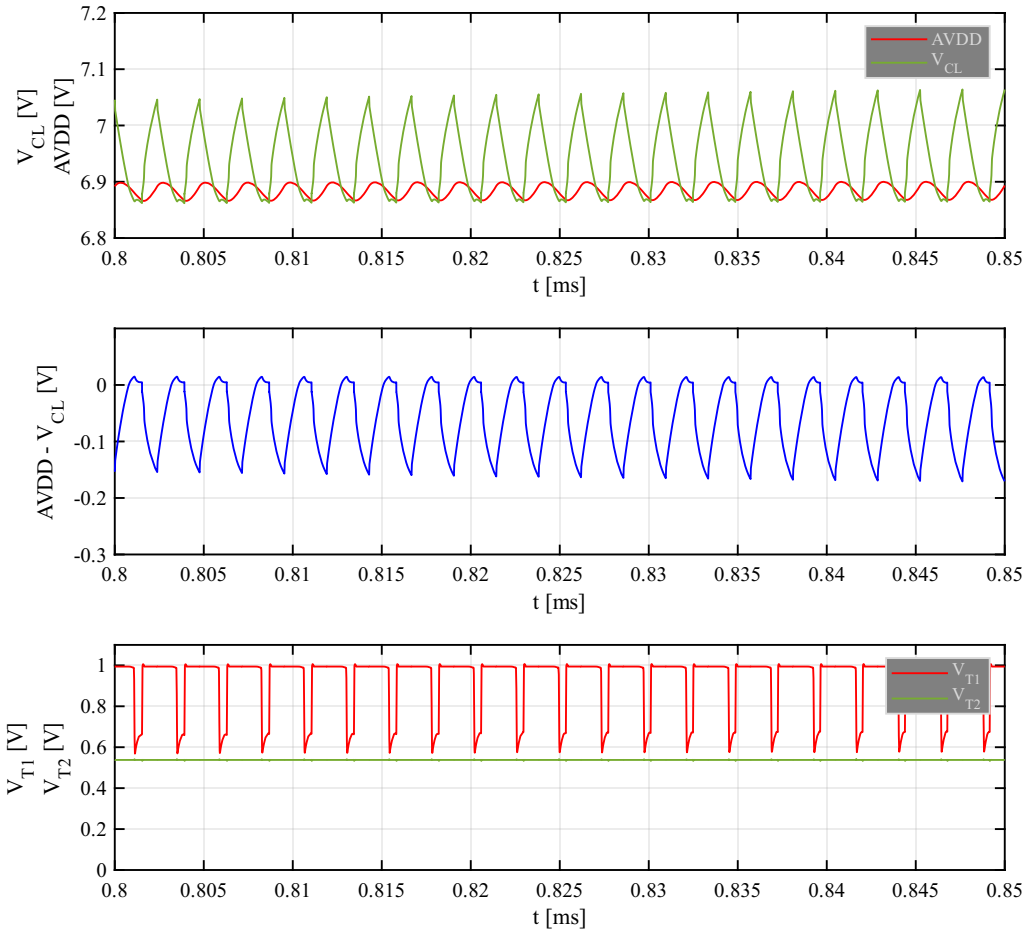


Figure 5.10: Simulation results of the PMOS driver under current-limit conditions, displaying the steady-state waveforms of the output voltage $AVDD$, the MP2 drain voltage V_{CL}, the voltage difference $AVDD - V_{CL}$, and the comparator-stage output voltages V_{T1} and V_{T2}

As the current through the AVDD switch increases, the corresponding voltage drop $V_{DS,AVDD}$ also increases, causing the AVDD voltage to decrease until it reaches the threshold value V_{CL}. When $AVDD - V_{CL}$ becomes negative, that is when AVDD falls below the threshold, the comparator generates V_{T1} and V_{T2} such that $V_{T1} > V_{T2}$.

As a consequence, the differential pair of the second stage becomes unbalanced and steers the tail current into the branch containing MN1.

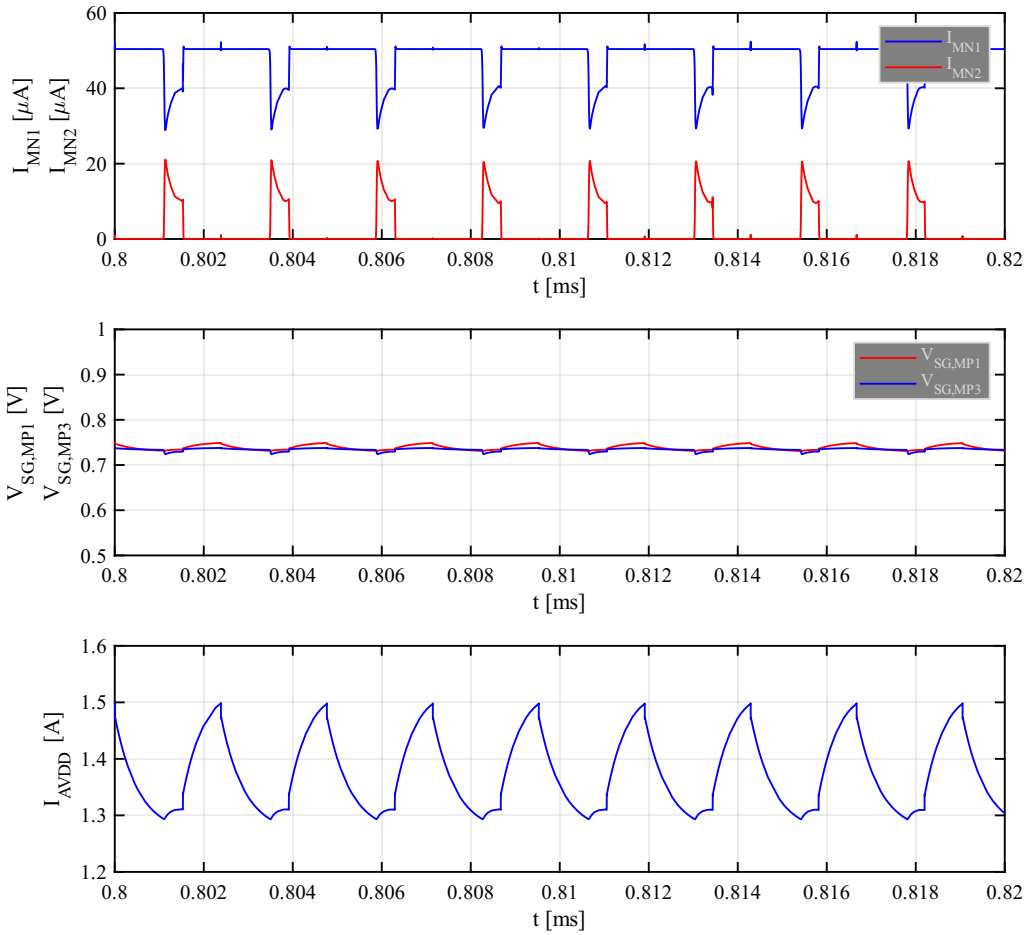


Figure 5.11: Simulation results of the PMOS driver under current-limit conditions, displaying the steady-state waveforms of the current flowing in differential stage branches I_{MN1} and I_{MN2}, the AVDD-switch source-to-gate driving voltage $V_{SG,MP1}$, the replica source-to-gate voltage $V_{SG,MP3}$ and the AVDD-switch current I_{AVDD}

As shown in Fig. 5.11, MN1 conducts the 50 μA tail current, which is subsequently mirrored to MP11.

The figure also shows that the voltage drop across MP11 becomes negligible, resulting in $V_{SG,MP1} \approx V_{SG,MP3}$. This source-to-gate voltage limits the operation of MP1 to a maximum current, independently of the load condition imposed by the simulation. The current-limit value is determined by the current imposed on transistor MP3 in the second stage, multiplied by the scaling factor n.

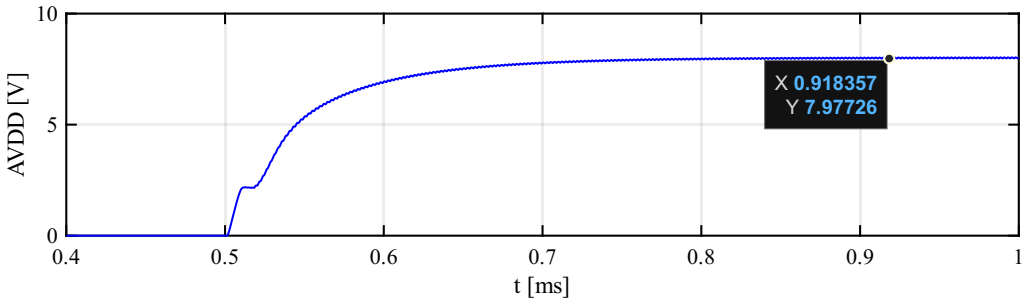


Figure 5.12: Simulation results of the PMOS driver under current-limit conditions displaying the output voltage $AVDD$

Furthermore, it can be observed in fig. 5.12 that the AVDD output voltage does not reach its target value when the isolation switch operates in current-limit conditions. The limitation imposed on the AVDD-switch current prevents the converter from delivering the current required by the load, causing the output voltage to drop below its regulated value.

As already discussed, this analysis provides insight into the operating principles of the proposed PMOS-based driving architecture. The resulting structure is taken as a reference for the implementation of the NMOS isolation-switch driver presented in the following sections. The objective is to preserve the same current-limiting functionality while ensuring proper operation of the isolation switch under both normal and current-limit conditions.

Chapter 6

Gate Driver Architectures for NMOS Isolation Switch

After analyzing the existing gate-driver architecture adopted for the PMOS isolation switch, the next step is to investigate a suitable driving solution for an NMOS-based implementation while preserving the same functional requirements.

Building upon the concepts introduced in Section 3.2, this chapter discusses the main design challenges arising from the adoption of an NMOS isolation switch and highlights the implications associated with its different operating principles.

As a first approach, a complementary implementation derived from the previously presented PMOS architecture is introduced. Its operating principle is analyzed and validated through simulations, which are then used to identify the main limitations of the approach.

Based on the insights gained from this preliminary investigation, a new gate-driver architecture is proposed. The operating principle of the final solution is analyzed in detail and supported by simulation results, highlighting the expected improvements compared to the initial implementation.

6.1 Design challenges

Designing a gate driver for the NMOS isolation switch requires the implementation of both a gate-bias generation function and a current-limiting mechanism compatible with the new architecture. Therefore, several design requirements must be reconsidered with respect to the PMOS-based solution described in the previous chapter.

First, driving a high-side NMOS device requires the generation of a gate voltage exceeding the source voltage by at least the threshold voltage necessary to turn the transistor on. This requires the adoption of a charge pump capable of generating a boosted supply voltage starting from the highest voltage available in the system, namely the AVDD output if the $V_{DS,AVDD}$ is neglected. The generated voltage is used to supply the driver circuitry and to establish a sufficiently large gate-to-source voltage, ensuring that the isolation switch remains fully enhanced and operates in

the triode region when enabled.

One of the main advantages of the architecture proposed in this work is the silicon-area reduction enabled by the removal of the HVINP pin. Consequently, the charge pump must be fully integrable so as not to require additional external components or pins, which would compromise the benefits achieved by the proposed solution. A first design challenge therefore lies in developing a driver whose operation is constrained not only by power consumption but also by the limited output capability of an integrated charge pump, both in terms of deliverable current and achievable output voltage.

Furthermore, unlike the PMOS implementation, where the driver is referenced between HVINP and ground and therefore experiences a dynamic range on the order of $V_{OUT} + V_{DS,AVDD}$, the NMOS driver must be supplied by the boosted voltage generated by the charge pump. As a result, particular attention must be paid to the choice of the circuit operating voltage domain in order to guarantee sufficient voltage headroom for correct operation under all operating conditions.

A second aspect concerns the current-limiting functionality. In the proposed architecture, the NMOS isolation switch is adopted in the configuration where the HVINP capacitor is removed. Consequently, the current flowing through the isolation device follows the same trend as the current through the high-side switch and can reach significantly larger values than in the original implementation. As anticipated in the introduction to Chapter 5, the purpose of the current-limiting function is therefore no longer to limit the load current, but rather to protect the isolation switch from excessive electrical stress.

As a consequence, the current-limit threshold must be set significantly higher than in the PMOS-based implementation. The required value can be derived from the maximum average inductor current together with its ripple component. The current ripple is obtained from eq.2.15 considering $L = 10\mu H$, switching frequency $f_s = 420kHz$,V_{IN}=2.8V and D=0.95, yielding approximately

$$\Delta i_L \approx 300\,\text{mA}.$$

The average inductor current can be estimated through power conservation, assuming a high conversion efficiency:

$$I_{DC} = I_{LOAD}\frac{V_{OUT}}{V_{IN}}.$$

Under the most critical operating conditions, namely $I_{LOAD} = 1\,\text{A}$, $V_{OUT} = 10\,\text{V}$, and $V_{IN} = 2.8\,\text{V}$, the maximum average current is $I_{DC,max} = 3.55\,\text{A}$. The resulting current-limit threshold should therefore be approximately

$$I_{DC,max} + \Delta i_L \approx 3.85\,\text{A}.$$

To provide additional margin for non-ideal conversion efficiency and process variations, a target current-limit value of 4 A is adopted throughout this work. This requirement represents a stringent design constraint, as the considerably higher current

threshold directly impacts the implementation of the sensing and current-limiting circuitry, which must generate appropriate reference quantities while maintaining a limited power budget.

In summary, the NMOS gate-driver architecture must provide the same functionalities previously achieved by the PMOS solution while addressing the additional challenges associated with boosted gate-voltage generation, restricted charge-pump capabilities, and a substantially higher current-limit requirement.

6.2 Initial NMOS Driver Implementation: Complementary Architecture

As a first attempt, the NMOS gate driver was derived directly from the PMOS-based architecture presented in Chapter 5. The proposed implementation is based on a complementary version of the original circuit, obtained by replacing each transistor with its complementary device type and appropriately resizing the resulting network in order to achieve the same functionality and operating behavior.

The complete schematic of the proposed implementation is shown in Fig. 6.1.

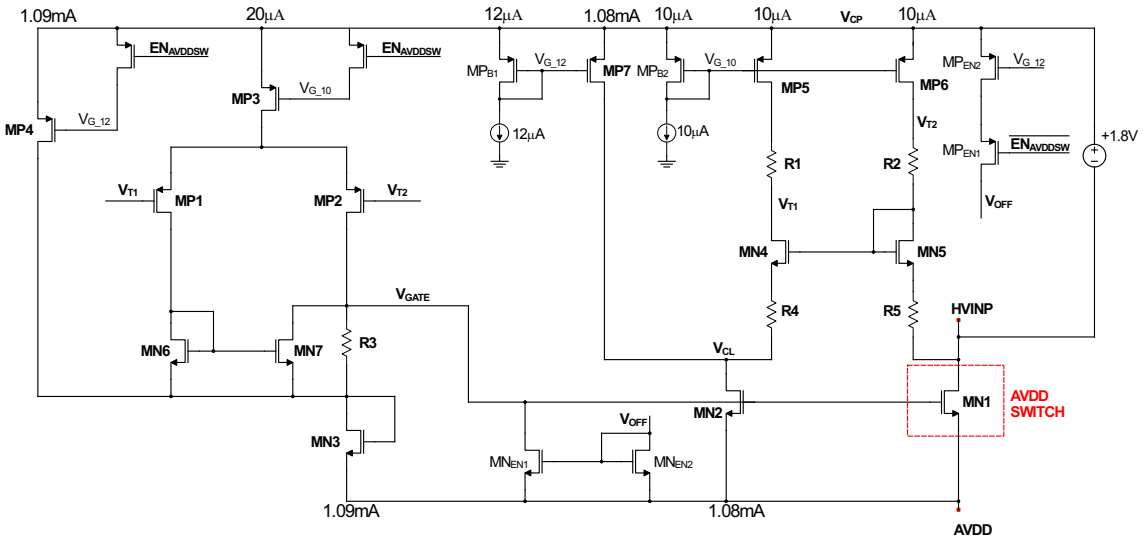


Figure 6.1: Transistor-level schematic of the NMOS isolation-switch driver based on a complementary architecture of the existing PMOS driver

As can be observed, the architecture retains the same functional organization of the PMOS driver, including the bias generation circuitry, the enable function, and the two main operating stages highlighted in Fig. 6.2.

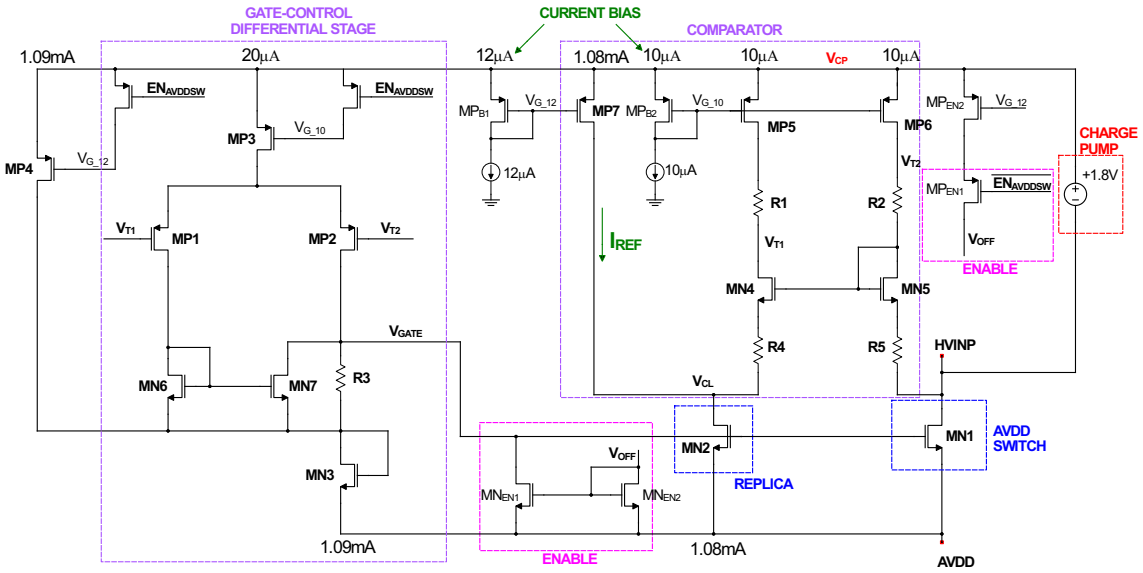


Figure 6.2: Transistor-level schematic of the NMOS isolation-switch driver with the main functional blocks highlighted

Similarly to the PMOS implementation, the enable circuitry controls the state of the isolation switch. When the ENABLE signal is deasserted, its complementary signal turns on the corresponding discharge transistor, forcing the gate-to-source voltage of the isolation switch MN1 to approximately zero and therefore turning the device off. The same bias-generation strategy adopted in the PMOS driver is preserved, with the reference currents being distributed to the various branches through the transistors labeled MN_B, thereby establishing the required operating conditions for the different circuit blocks.

In addition, the schematic includes the charge pump required for NMOS operation. For the purpose of this analysis, the charge pump is modeled as a boosted voltage source characterized by finite output impedance and limited current-driving capability. Its output voltage is assumed to be equal to $HVINP + 1.8\,\mathrm{V}$, providing the supply required by the gate-driver circuitry.

The first stage of the architecture is shown in Fig. 6.3.

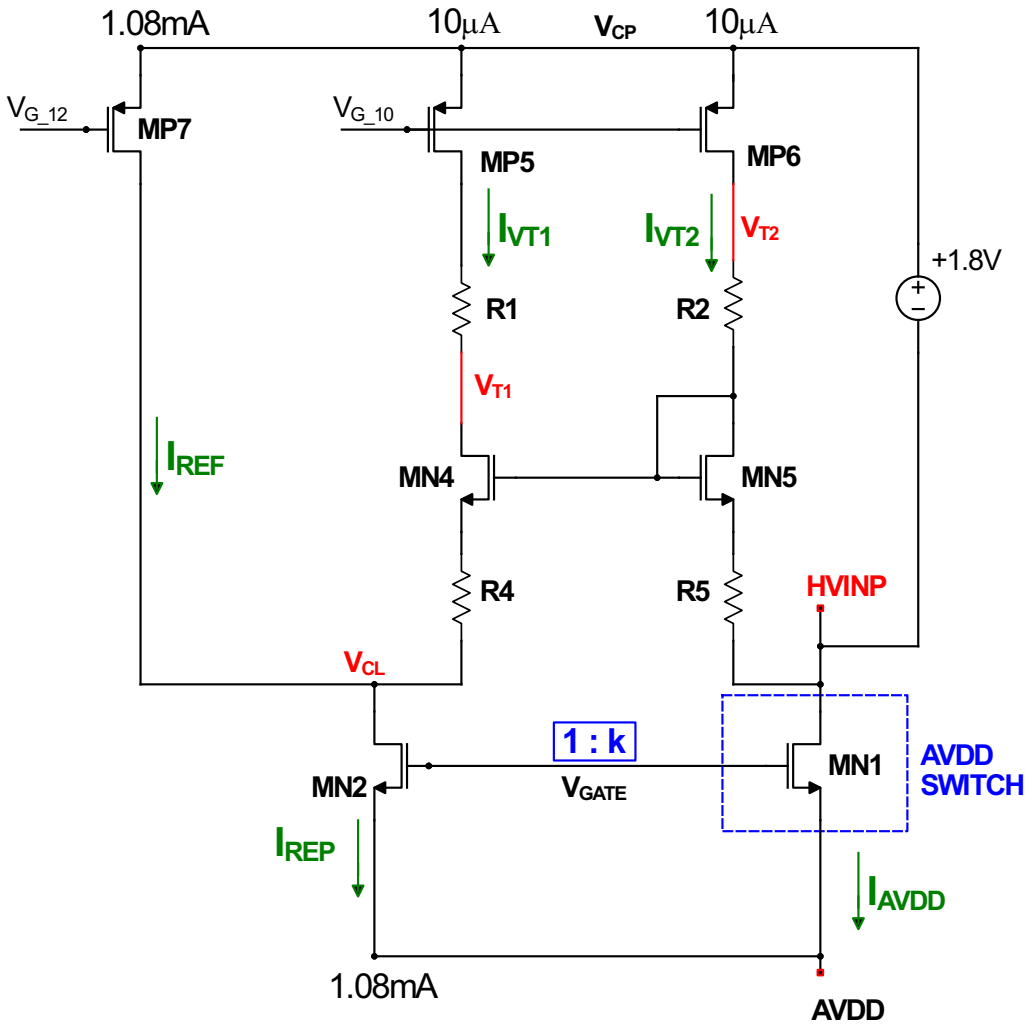


Figure 6.3: Replica and comparator stage of the NMOS isolation-switch complementary driver

The NMOS isolation switch ($MN1$) is sized according to the criteria presented in Chapter 4. The transistor $MN2$ acts as a scaled replica of the isolation switch, with a scaling factor k, and is biased so as to reproduce the maximum drain-to-source voltage experienced by $MN1$ under current-limit conditions.

As in the PMOS driver architecture, the replica branch is biased by a reference current I_{REF} chosen such that, at the onset of current limiting, the replicated current is

$$I_{REP,LIM} = \frac{I_{AVDD,max}}{k}.$$

The drain voltage of $MN2$, denoted by V_{CL}, acts as the comparison threshold against the $HVINP$ voltage, allowing the circuit to determine whether the isolation switch is operating below or above the current-limit condition. The resulting comparison generates the voltages V_{T1} and V_{T2}, which are subsequently used by the gate-control stage.

The second stage of the architecture is shown in Fig. 6.4.

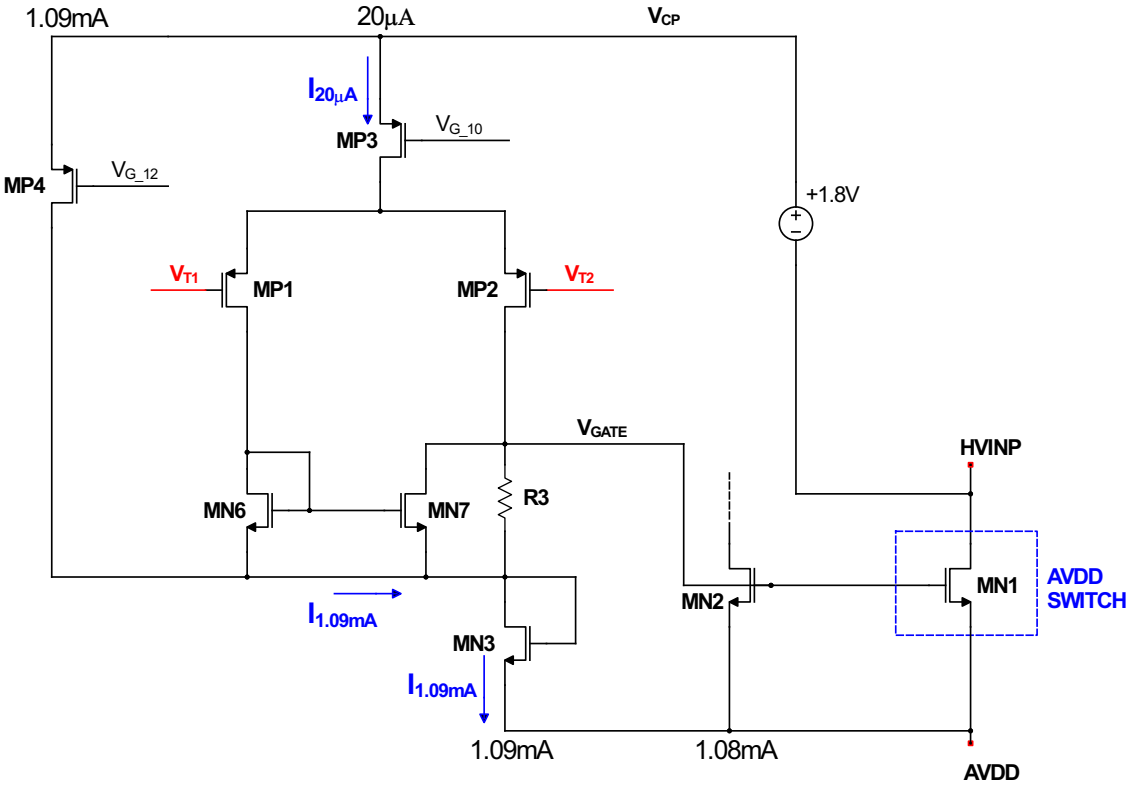


Figure 6.4: Gate-control differential stage of the NMOS isolation-switch complementary driver

As illustrated in Fig. 6.4, the voltages V_{T1} and V_{T2} are applied to a PMOS-input differential gate-control stage. Depending on the outcome of the comparison, the tail current is steered toward one of the two branches, thereby modifying the gate-drive condition of the isolation switch.

As a result, the gate voltage of $MN1$ is adjusted to provide either the nominal gate-to-source voltage required for normal operation, typically around 1.5 V, or the value necessary to constrain the maximum current when the current-limit condition is reached. The transistor $MN3$ performs a function analogous to that of the replica transistor used in the second stage of the PMOS driver (MP3 in Fig. 5.5). More specifically, it reproduces the gate-to-source voltage corresponding to the current-limit operating point of the isolation switch, providing the reference condition required to enforce the desired current limit once the protection mechanism becomes active.

6.2.1 Circuit Operation and Simulation Results

The functionality of the proposed architecture was initially verified independently of the complete boost-converter system. To reproduce the operating conditions experienced by the isolation switch, the voltage at the $HVINP$ node was fixed to $AVDD + \Delta V$, where ΔV is representative of the voltage drop on the power transistor, while a variable resistive load was connected to the source terminal of $MN1$ in order to set the current flowing through the AVDD isolation switch (Fig 6.5).

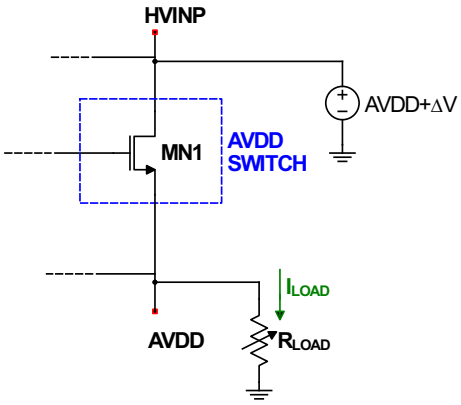


Figure 6.5: Simplified testbench adopted to validate the NMOS gate-driver operation independently of the complete boost-converter system

In this testbench configuration, an increase in load current results in a reduction of the $AVDD$ voltage rather than an increase of the $HVINP$ voltage, as would occur in the actual converter. Nevertheless, both the source terminal of $MN1$ and that of its replica transistor $MN2$ are connected to the $AVDD$ node. Consequently, since $MN2$ is operating in triode region, when $AVDD$ decreases, the threshold voltage V_{CL} corresponding to the drain voltage of $MN2$ decreases by the same amount. Therefore, the variation of the quantity $HVINP - V_{CL}$, which is the parameter used by the comparator to determine the operating condition of the isolation switch, remains equivalent to that occurring in the actual converter.

As a result, the operation of the current-detection stage is accurately reproduced despite the simplified test setup. The simulations were performed under critical operating conditions with $AVDD = 10\,\mathrm{V}$. The enable signal is asserted at 0.3 ms, turning on the isolation switch.

In order to evaluate both operating regimes, the current flowing through the isolation switch, I_{AVDD}, was directly imposed. A value of 1 A was used to verify normal operation, whereas a current of 10 A, well above the programmed current-limit threshold, was applied to force the circuit into current-limit conditions.

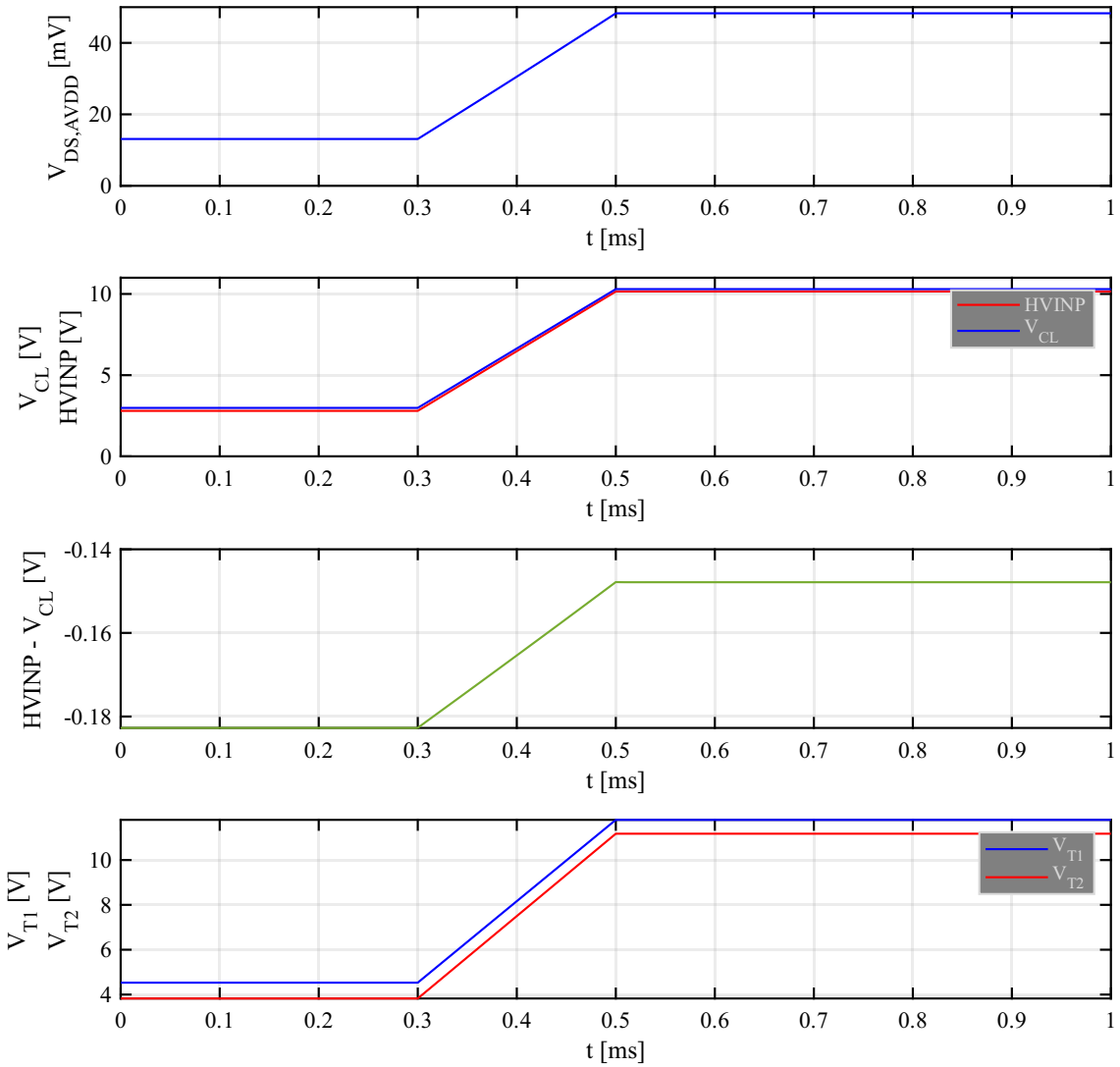


Figure 6.6: Simulation results of the first stage of the NMOS driver under typical operating conditions, displaying the AVDD-switch drain-to-source voltage $V_{DS,AVDD}$, the $HVINP$ voltage, the MN2 drain voltage V_{CL}, the voltage difference $HVINP - V_{CL}$, and the comparator-stage output voltages V_{T1} and V_{T2}

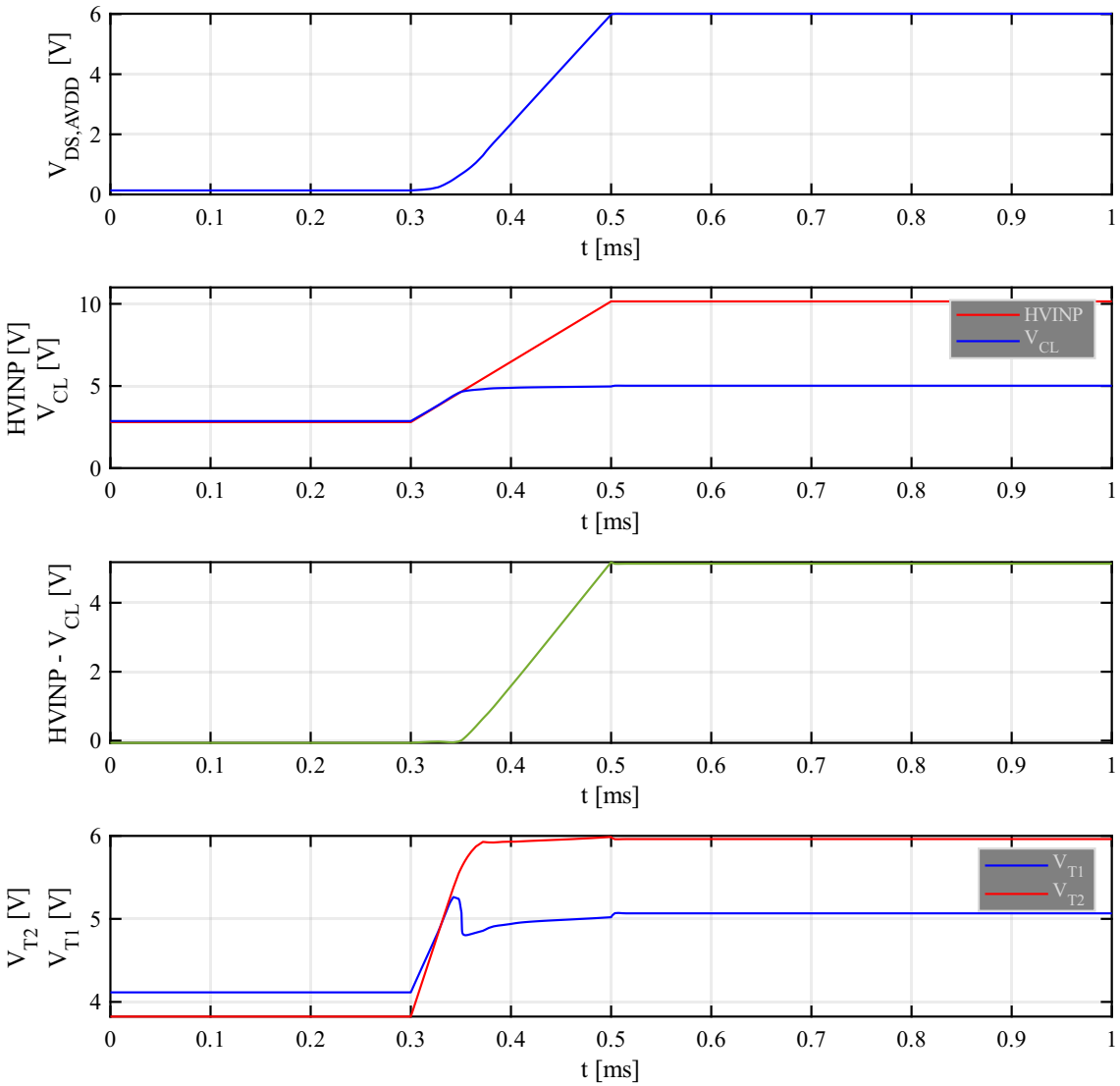


Figure 6.7: Simulation results of the first stage of the NMOS driver in current-limit conditions, displaying the AVDD-switch drain-to-source voltage $V_{DS,AVDD}$, the $HVINP$ voltage, the MN2 drain voltage V_{CL}, the voltage difference $HVINP - V_{CL}$, and the comparator-stage output voltages V_{T1} and V_{T2}

Figures 6.6 and 6.7 show the operation of the first stage. Under nominal operating conditions, the drain-to-source voltage of $MN1$ remains sufficiently small such that $HVINP < V_{CL}$. As a consequence, the comparator generates an output condition characterized by

$$V_{T2} < V_{T1}.$$

When the current through $MN1$ approaches the current-limit threshold, the increased voltage drop across the isolation switch causes $V_{DS,MN1}$ to rise. This condition is reflected by the replica branch, causing the relationship between $HVINP$ and V_{CL} to reverse. Once the current-limit operating point is reached, the comparator switches state and generates

$$V_{T1} < V_{T2}.$$

The resistors R_1 and R_2 are equally sized so that the transition occurs when

the currents flowing through $MP5$ and $MP6$ become equal, thereby defining the switching threshold of the comparator stage.

It should be noted that the voltage difference between $HVINP$ and V_{CL} in Fig. 6.7 is an artifact of the adopted testbench, since $HVINP$ is externally imposed rather than generated by the converter. Nevertheless, its magnitude has no impact on the operation of the circuit, as the comparator only detects whether $HVINP$ is above or below V_{CL}. The crossing between the two voltages is therefore sufficient to reproduce the intended state transition.

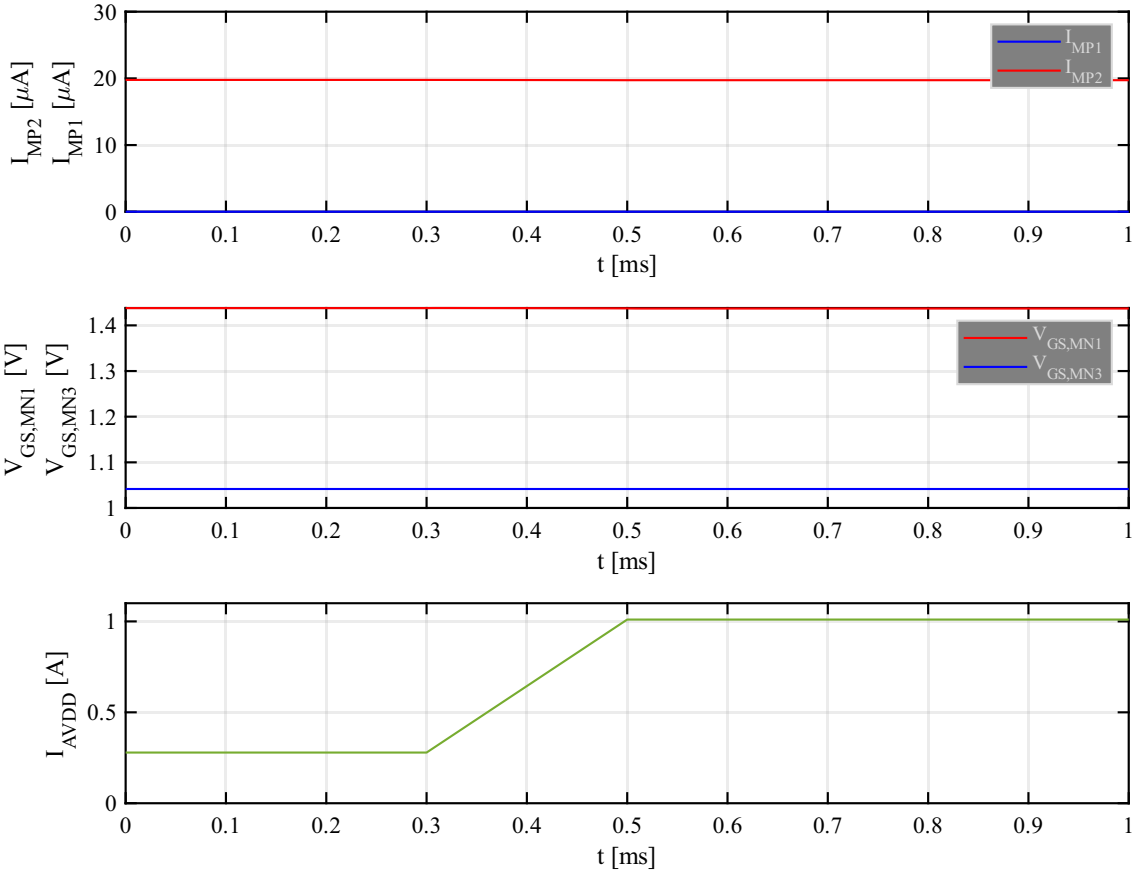


Figure 6.8: Simulation results of the second stage of the NMOS driver under typical operating conditions, displaying the current flowing in differential stage branches I_{MP1} and I_{MP2}, the AVDD-switch gate-to-source driving voltage $V_{GS,MN1}$, the replica gate-to-source voltage $V_{GS,MN3}$ and the AVDD-switch current I_{AVDD}

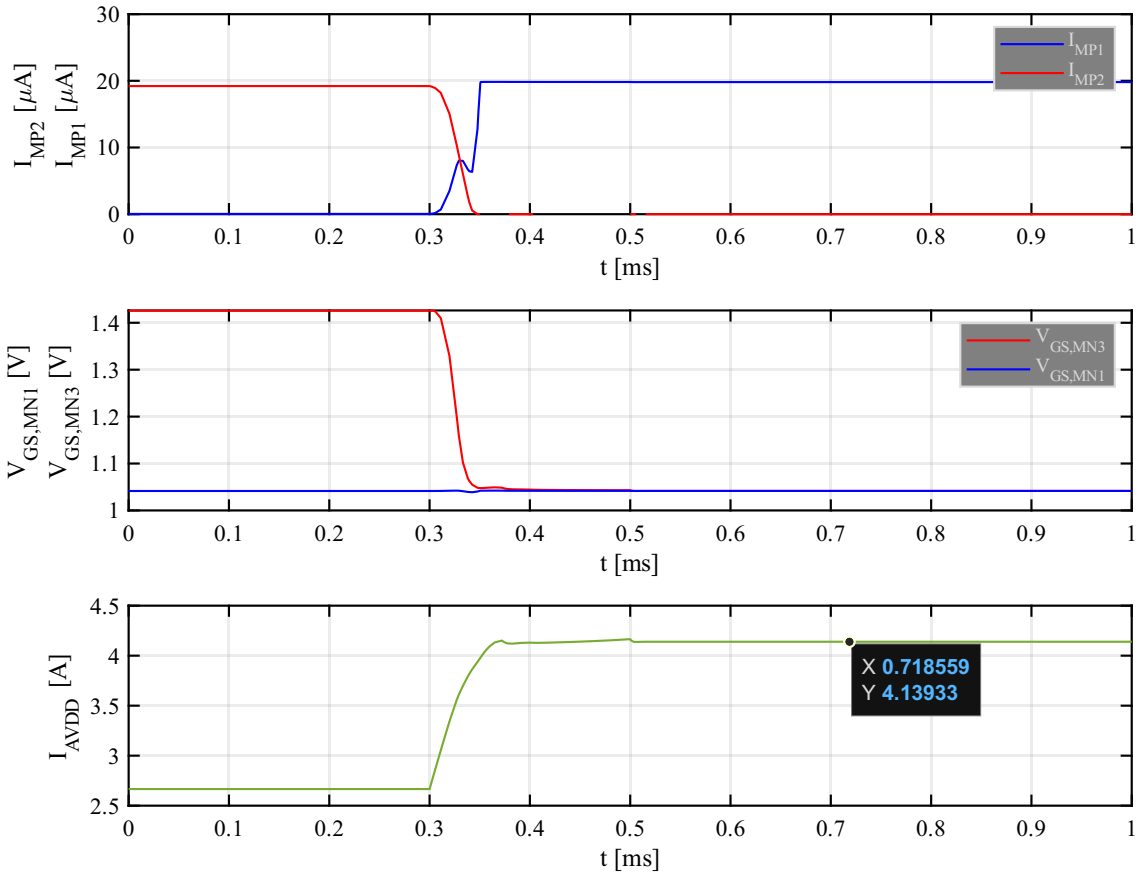


Figure 6.9: Simulation results of the second stage of the NMOS driver in current-limit conditions, displaying the current flowing in differential stage branches I_{MP1} and I_{MP2}, the AVDD-switch gate-to-source driving voltage $V_{GS,MN1}$, the replica gate-to-source voltage $V_{GS,MN3}$ and the AVDD-switch current I_{AVDD}

The second stage exhibits an operating principle analogous to that of the PMOS driver (Fig. 5.5). As shown in Fig. 6.8 and 6.9, the voltages V_{T1} and V_{T2} drive the gates of $MP1$ and $MP2$, respectively, steering the tail current toward one of the two branches depending on the operating condition.

During normal operation, the entire tail current flows through the $MP2$ branch, generating a gate voltage for the isolation switch such that

$$V_{GS,MN1} = V_{GS,MN3} + I_{20\mu A} R_3.$$

The resistor R_3 is sized to produce a gate-to-source voltage of approximately 1.4 V, ensuring that the isolation switch remains fully enhanced.

Conversely, when the current-limit condition is detected, the tail current is redirected to the $MP1$ branch. Through the current mirror formed by $MN6$ and $MN7$, a sufficient current is generated to keep $V_{DS,MN7}$ negligible. Under these conditions, the voltage applied to the gate of $MN1$ becomes approximately equal to that of the replica transistor $MN3$, resulting in

$$V_{GS,MN1} \approx V_{GS,MN3}.$$

Since $MN3$ reproduces the gate-to-source voltage corresponding to the desired current-limit operating point, the isolation switch is forced to conduct approximately its maximum allowable current. As a result, the current through the AVDD switch is constrained to about $I_{AVDD,max} \approx 4\,\mathrm{A}$, which corresponds to the current flowing through the replica transistor $MN3$ multiplied by the replica scaling factor k.

These results demonstrate that the complementary architecture successfully reproduces the intended current-limiting behavior and achieves the same operating principle as the previously analyzed PMOS driver.

6.2.2 Limitations of the Complementary Architecture

Although the complementary architecture presented in the previous section successfully reproduces the functionality of the PMOS gate driver, several limitations make its practical implementation unattractive.

A first issue is related to the available voltage headroom. As shown in Fig. 6.1, the circuit operates between the AVDD node and the charge-pump output voltage V_{CP}. Since the charge pump provides a voltage approximately equal to $AVDD + 1.8\,\mathrm{V}$, the entire architecture must operate within an effective voltage range of only $1.8\,\mathrm{V}$.

This represents a substantial limitation compared to the PMOS driver, where the available dynamic range was approximately equal to the HVINP voltage. In the NMOS implementation, a significant fraction of the available voltage budget is already required to generate the gate-to-source voltage of the isolation switch. More specifically, approximately $1.4\,\mathrm{V}$ are needed to ensure the proper operation of $MN1$, leaving only a small residual voltage available for biasing the remaining circuitry. Referring to Fig. 6.1, the transistors belonging to the $MP5$ and $MP6$ branches must remain in saturation while accommodating the voltage drops across R_1, R_2, R_4, and R_5, as well as guaranteeing the correct operating region for $MN4$ and $MN5$.

Although the circuit can be properly biased through careful device sizing, the resulting operating margins are extremely limited. Consequently, even modest process variations or device mismatch may shift some transistors out of their intended operating region, leading to degradation or failure of the current-detection function.

A second limitation is associated with power consumption. As discussed in Section 6.1, the substantially larger current flowing through the isolation switch requires a correspondingly larger reference current in the replica branch in order to establish the correct current-limit threshold. As a result, the total current consumption of the driver exceeds $2\,\mathrm{mA}$. This increase is not only associated with higher power dissipation, which is expected given the significantly larger current-limit requirement, but also places a considerable load on the charge pump.

Although the proposed architecture correctly reproduces the desired current-limiting functionality, simulation results show that a substantial amount of current

is continuously drawn from the boosted supply. Such a current demand is difficult to reconcile with the implementation of a fully integrated charge pump. Providing several milliamperes from an on-chip charge pump would require a considerably larger circuit and would significantly reduce its efficiency, ultimately making the proposed solution impractical for the intended application.

The analysis of the complementary architecture therefore highlights two fundamental limitations. First, the voltage range available between V_{CP} and $AVDD$ is insufficient to guarantee robust operation with adequate design margin. Second, the reference-current levels required by the current-limiting circuitry are incompatible with the output-current capability of a realistically integrable charge pump.

These observations provide the key guidelines for the development of an improved architecture. The gate-driver circuitry should be referenced to ground in order to exploit a wider effective voltage range, while the current-sensing architecture should be reformulated to reduce the current demand imposed on the charge pump.

6.3 Final NMOS Driver Architecture

The final architecture, shown in Fig. 6.10, implements the functionality identified as necessary from the analysis of the previously presented driver solutions. In particular, transistor MN1 acts as the isolation switch and represents the main power device controlled by the proposed architecture.

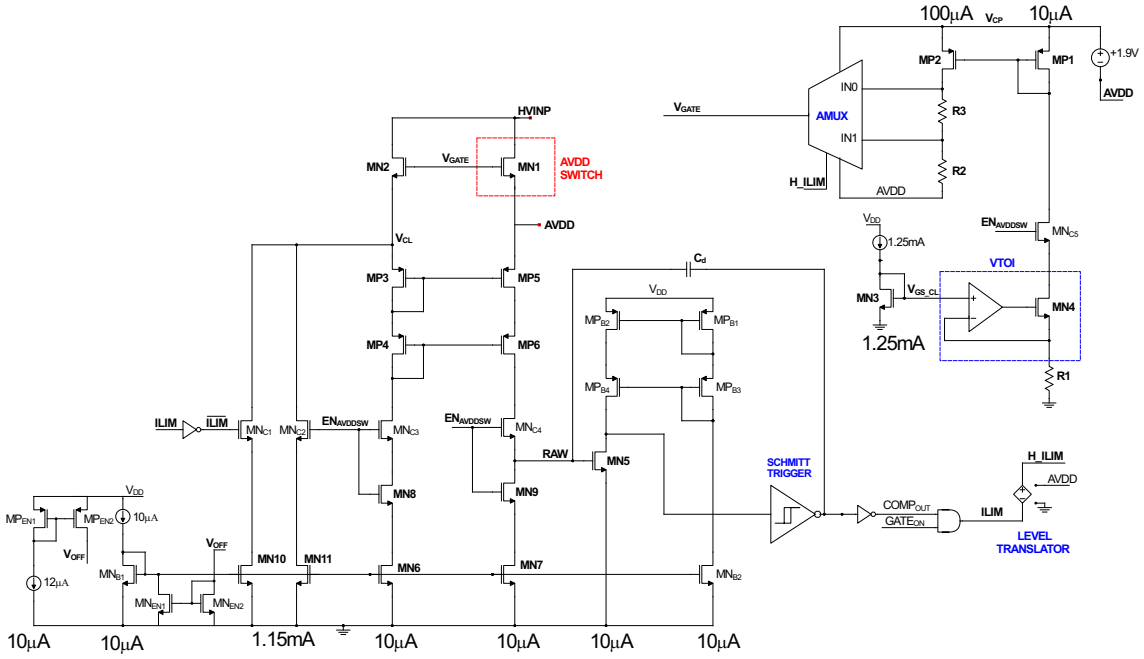


Figure 6.10: Proposed NMOS-based isolation-switch driver architecture

The circuit includes dedicated biasing blocks, highlighted in Fig. 6.11, responsible for generating the bias currents required by the various functional blocks. The enable signal is managed such that the current flowing through the main branches

of the circuit is reduced to zero when the isolation switch is disabled. In particular, when the enable signal is low, transistor MN_{C5} is turned off, interrupting the current required by the mirror composed of MP1 and MP2, which is responsible for generating the gate-drive voltage of MN1. As a consequence, the imposed gate voltage results in $V_{GS,AVDD} \approx 0\,\mathrm{V}$, ensuring that the isolation switch remains turned off.

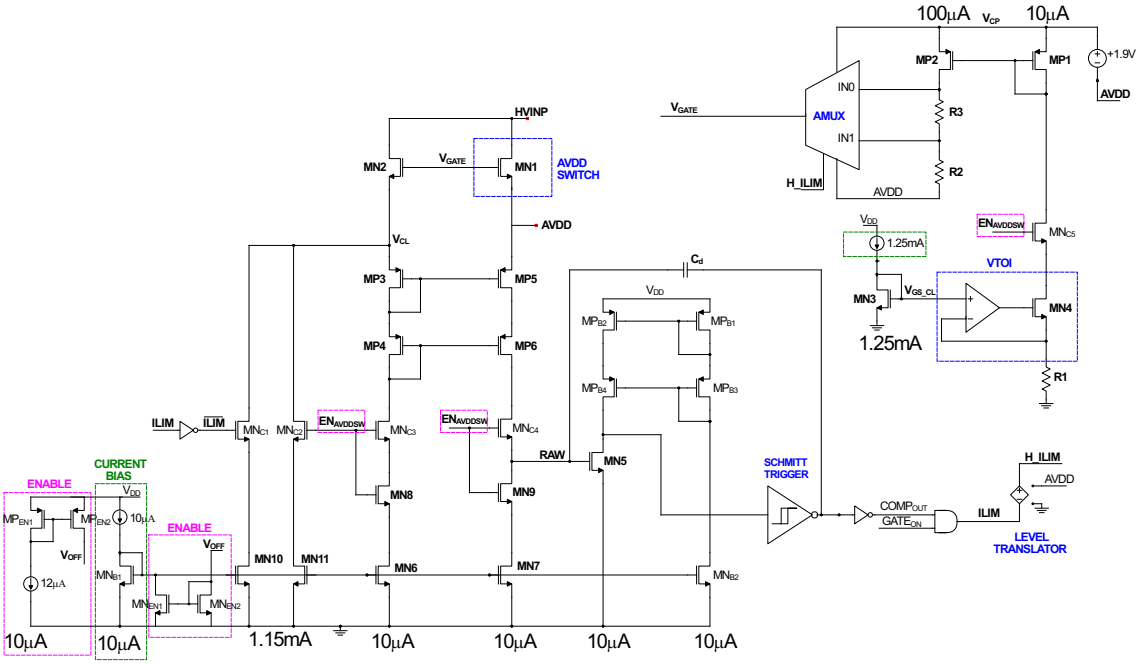


Figure 6.11: Proposed NMOS-based isolation-switch driver with the current bias generation and enable functional blocks highlighted

The operation of the proposed solution relies on several functional blocks that differ from those employed in the complementary PMOS-based architecture.

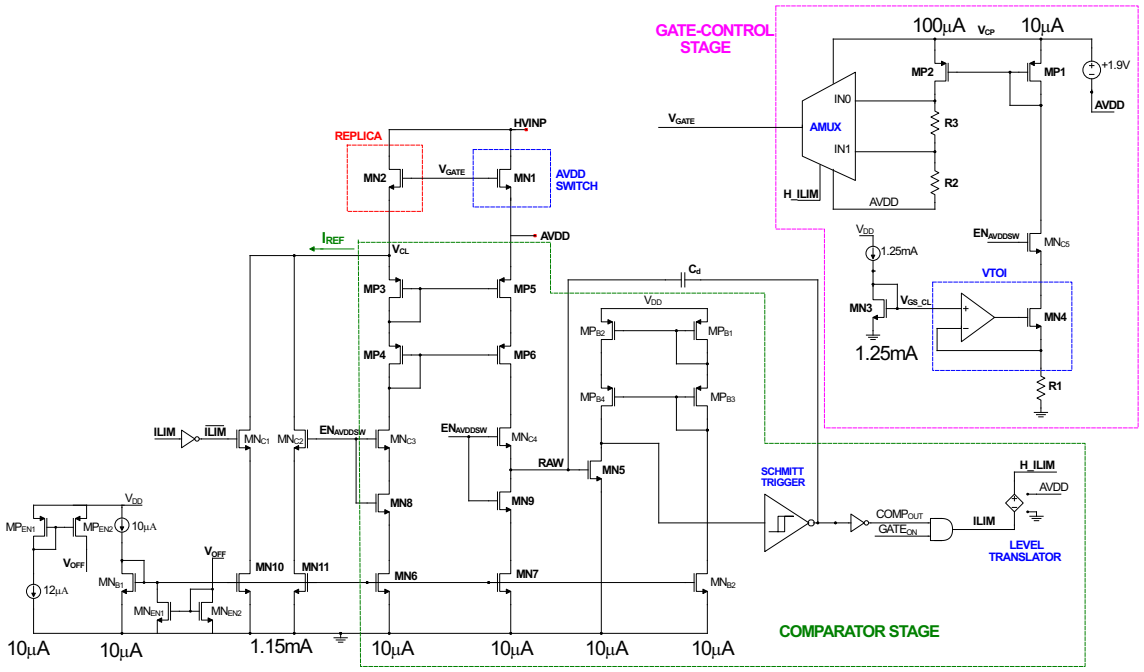


Figure 6.12: Proposed NMOS-based isolation-switch driver with the replica and comparator stage and gate-control stage highlighted

As shown in Fig. 6.12, the circuit includes a replica transistor, denoted as MN2, which represents a scaled-down version of the main isolation switch MN1 by a factor k. Furthermore, a comparator stage is employed to monitor the operating condition of the isolation switch, reproducing a function analogous to that performed by the comparator analyzed in the previous architecture.

Unlike the PMOS implementation, however, the output of the first stage is a digital signal, denoted as $ILIM$, which indicates whether the circuit is operating under current-limit conditions. This signal is subsequently translated to the high-voltage domain defined by AVDD and the charge-pump voltage V_{CP} and is used to control an analog multiplexer (AMUX), identified in Fig. 6.10.

The $ILIM$ signal therefore determines the operating state of the driver according to the truth table reported below:

Operating Condition	ILIM
Current-limit condition	1
Normal operation	0

Table 6.1: Operating conditions associated with the ILIM signal

Depending on the value of $ILIM$, the AMUX selects one of two gate-drive voltages to be applied to the gate of MN1. Under normal operating conditions ($ILIM = 0$), the voltage connected to input IN0 is selected, whereas under current-limit conditions ($ILIM = 1$) the output is switched to input IN1.

The detailed operation of each functional block, together with the corresponding simulation results, is presented in the following sections. Particular attention

is devoted to the current-limiting mechanism and to the architectural advantages introduced by the proposed NMOS-based implementation with respect to the previously analyzed complementary solution.

6.3.1 Circuit Analysis and Simulation Results

The proposed architecture was analyzed using a testbench similar to that adopted for the NMOS implementation described in Section 6.2. As in the previous case, the $HVINP$ voltage is fixed, while the current flowing through the isolation switch is varied by means of a variable resistive load.

Although the circuit introduces a different implementation of the current-detection mechanism, its operating principle retains several concepts already discussed in the previously presented architectures. For this reason, its functionality can again be analyzed by separating the circuit into two main stages.

FIRST STAGE of the NMOS DRIVER

The first stage of the proposed architecture is shown in Fig. 6.13.

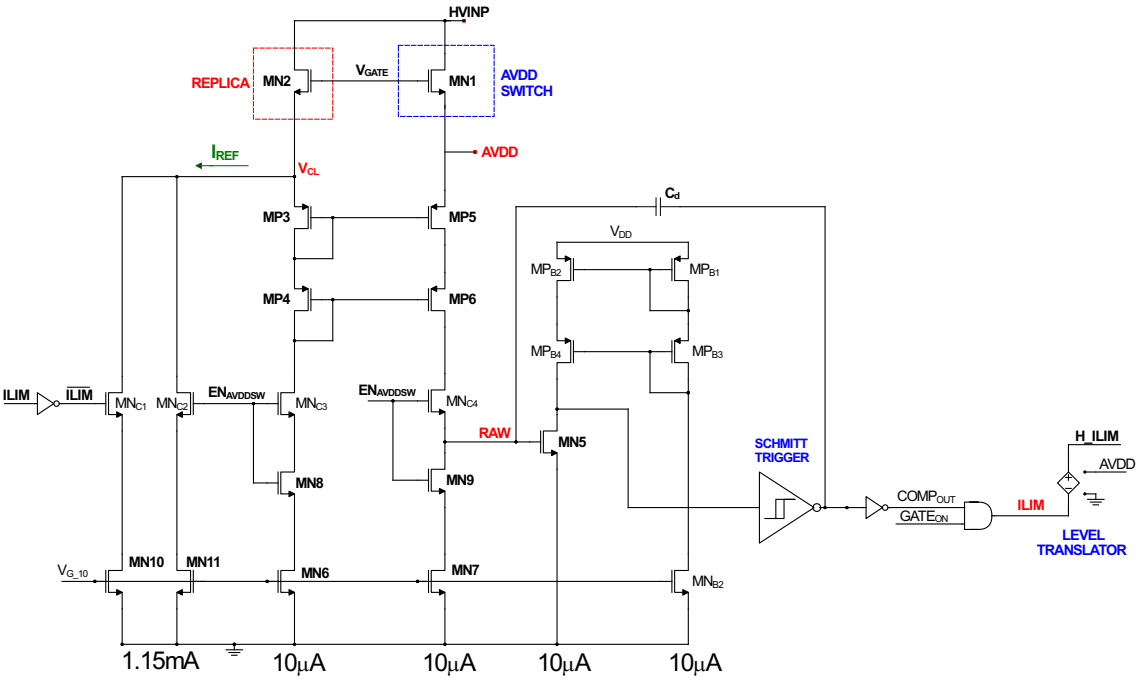


Figure 6.13: First stage of the proposed NMOS driver architecture

The cascode transistors labeled MN_C serve the same purpose as their counterparts in the previously discussed architectures. The replica transistor $MN2$ can also be identified. Its source voltage, denoted as V_{CL}, acts as the reference threshold used to determine whether the isolation switch is operating under nominal conditions or has entered the current-limit region.

The reference current is selected such that the voltage drop reproduced across $MN2$ is equal to the drain-to-source voltage of the isolation switch in current limit conditions, $V_{DS,AVDD,max}$. Therefore, the sizing of the replica branch is based on

a target current-limit value of $I_{AVDD,max} = 4\,\mathrm{A}$, with k denoting the scaling factor between the isolation switch and its replica transistor.

The reference current used in the comparator stage is intentionally chosen slightly lower than the value that would produce

$$I_{REP,LIM} = \frac{I_{AVDD,max}}{k}.$$

As a result, the onset of the current-limit condition is detected before the isolation-switch current reaches its maximum regulated value. This introduces a small margin between the comparator threshold and the effective current limit imposed by the second stage, preventing unintended transitions out of the current-limit condition that could otherwise result from small variations in the generated gate-to-source voltage.

As previously discussed, the adopted testbench differs from the actual converter operation. Since $HVINP$ is fixed, an increase in the current through the AVDD switch produces a reduction in $AVDD$, whereas in the real converter $AVDD$ remains regulated and the increase in $V_{DS,AVDD}$ would instead result in a rise of the $HVINP$ voltage, thereby increasing the source potential of $MN2$. Nevertheless, the comparator is sensitive only to the voltage difference between $AVDD$ and the reference voltage V_{CL}. Therefore, this alternative excitation produces the same effect at the comparator input and accurately reproduces the intended circuit behavior.

In the replica branch, the diode-connected transistors $MP3$ and $MP4$ control the gates of $MP5$ and $MP6$, which belong to the branch monitoring the AVDD isolation switch.

Before current limiting occurs, the drain-to-source voltage of the isolation switch is relatively small, resulting in the condition

$$AVDD > V_{CL}.$$

Under these conditions, the source-to-gate voltage of $MP5$ is sufficiently larger than its threshold voltage to keep the transistor turned on. As a result, the current imposed by the mirror formed with $MN7$, equal to $10\,\mu\mathrm{A}$, flows through the $MP5$ branch.

In this operating condition, the voltage at the node labeled RAW is given by

$$V_{RAW} = EN_{AVDDSW} - V_{TH,MNC4} - V_{OV,MNC4},$$

where EN_{AVDDSW} is equal to VDD (1.9 V) when asserted. Through proper transistor sizing, the circuit is designed to satisfy

$$V_{RAW} > V_{GS,MN5}.$$

Consequently, $MN5$ is turned on and its drain voltage is pulled toward ground.

The drain voltage of $MN5$ is then applied to a Schmitt trigger, which provides a robust state detection function and generates an inverted output. An additional

inverter is therefore placed at its output to produce the signal $COMP_OUT$. This signal is referenced to the VDD-to-ground domain, and it is processed as a conventional digital signal.

The signal $GATE_ON$, which is applied to the second input of the AND gate, is asserted only when the isolation switch is enabled. This prevents false current-limit detections during startup, when the inductor is being charged and the drain-to-source voltage of the isolation switch may temporarily exceed the comparator threshold even though the current-limit condition has not yet been reached.

As a result, the output of the first stage is the digital signal $ILIM$, which follows the state of $COMP_OUT$ only when the isolation switch is effectively turned on.

As the current through the isolation switch increases and approaches the current-limit threshold, $V_{DS,AVDD}$ rises until the condition $AVDD < V_{CL}$ is reached. Beyond this point, the source-to-gate voltage of $MP5$ decreases below its threshold voltage, causing the transistor to turn off. Consequently, the drain voltage of $MN7$ drops until the transistor enters the linear region, effectively suppressing the current that would otherwise be imposed by the mirror.

As a result, the RAW node voltage falls below the turn-on threshold of $MN5$. The transistors labeled MP_B provide the bias current for the branch by mirroring a current of approximately $10\,\mu$A and are sized such that, when $MN5$ is turned off, its drain node is pulled toward VDD.
The comparator output therefore switches state, producing a logic-high $ILIM$ signal that indicates the current-limit condition.

The behavior of the first stage was verified through simulation with $V_{OUT} = 10\,\text{V}$. A variable load resistance was used to transition from a nominal operating condition, corresponding to $I_{AVDD} = 1\,\text{A}$, to a forced overload condition corresponding to $I_{AVDD} = 10\,\text{A}$ at $t = 1.5\,\text{ms}$. The load was then restored at $t = 2.5\,\text{ms}$, bringing the circuit back to the nominal operating condition.

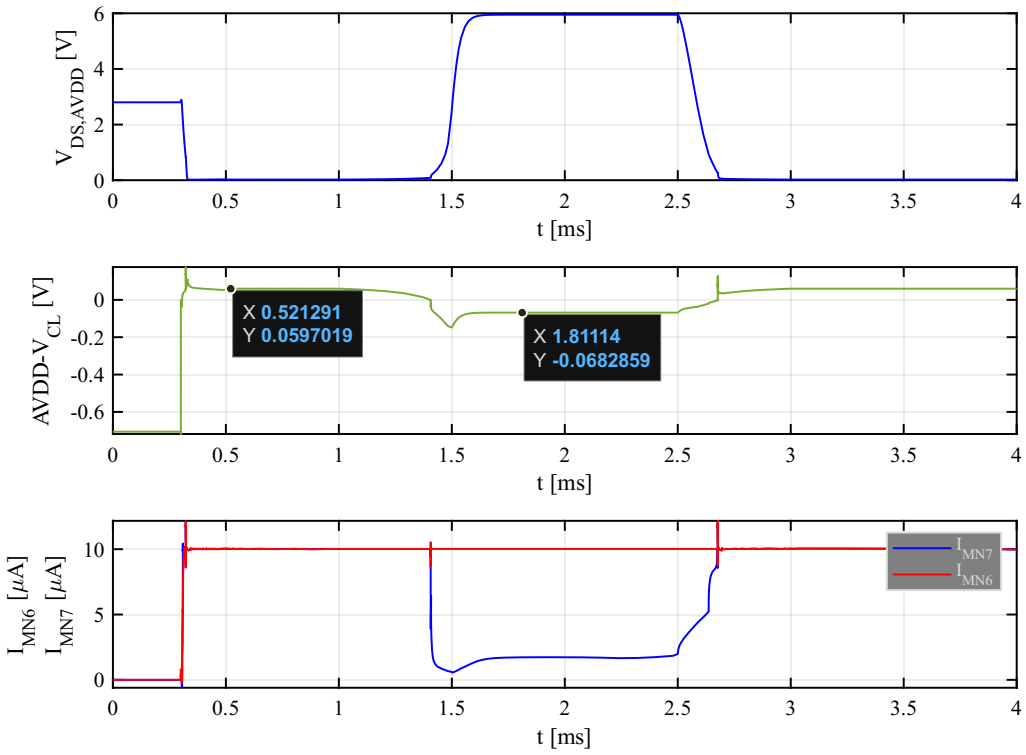


Figure 6.14: Simulation results of the proposed NMOS driver displaying the state transition between normal and current limit condition of waveforms $V_{DS,AVDD}$ the isolation switch voltage drop, the voltage difference $AVDD - V_{CL}$, and the currents of MN6 and MN7 I_{MN6} and I_{MN7}

Figure 6.14 shows the transition from normal operation, characterized by $AVDD - V_{CL} > 0$ to the current-limit condition, where the increase of $V_{DS,AVDD}$ causes $AVDD - V_{CL} < 0$. Accordingly, the currents flowing through $MN6$ and $MN7$, initially equal to $10\,\mu$A, become unbalanced, with the current through $MN7$ decreasing significantly.

It should be noted that the absolute value of $V_{DS,AVDD}$ observed under current-limit conditions is not representative of the actual converter operation, since $HVINP$ is fixed by the testbench. In the complete system, the HVINP voltage would instead decrease as a consequence of the load not receiving the requested current.

Finally, Fig. 6.15 illustrates the evolution of the RAW node voltage together with the conduction state of $MN5$.

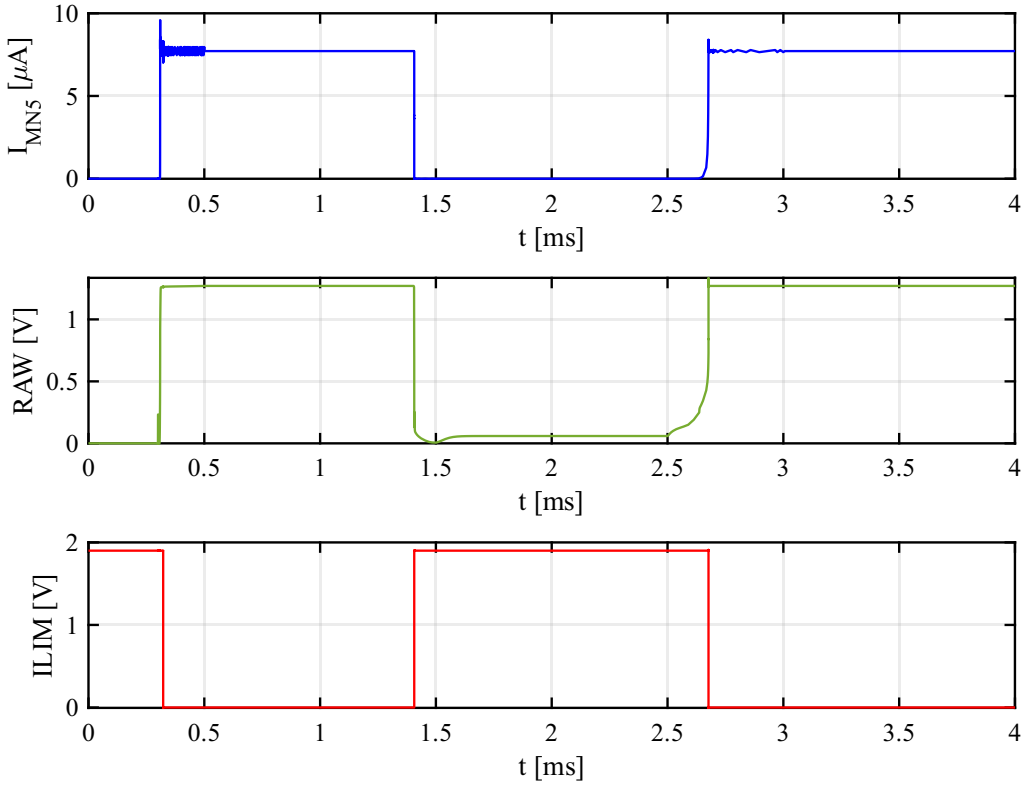


Figure 6.15: Simulation results of the proposed NMOS driver displaying the state transition between normal and current limit condition of waveforms I_{MN5} the current through transistor MN5, the voltage at node RAW, and the ILIM signal

The figure clearly shows how the comparator changes state as the operating condition transitions into current limit, causing the $ILIM$ signal to switch high and thereby correctly indicating the activation of the protection mechanism.

The behavior of the $ILIM$ signal, however, requires further discussion. Reliable operation of the comparator stage relies on the presence of an additional stabilization mechanisms that confirm the detected operating state.

In particular, without such a mechanism, when the circuit transitions from the current-limit condition back to normal operation, the $ILIM$ signal may experience undesired oscillations before settling to its low state. To highlight this effect, Fig. 6.16 reports the simulated behavior of the circuit without the stabilization network.

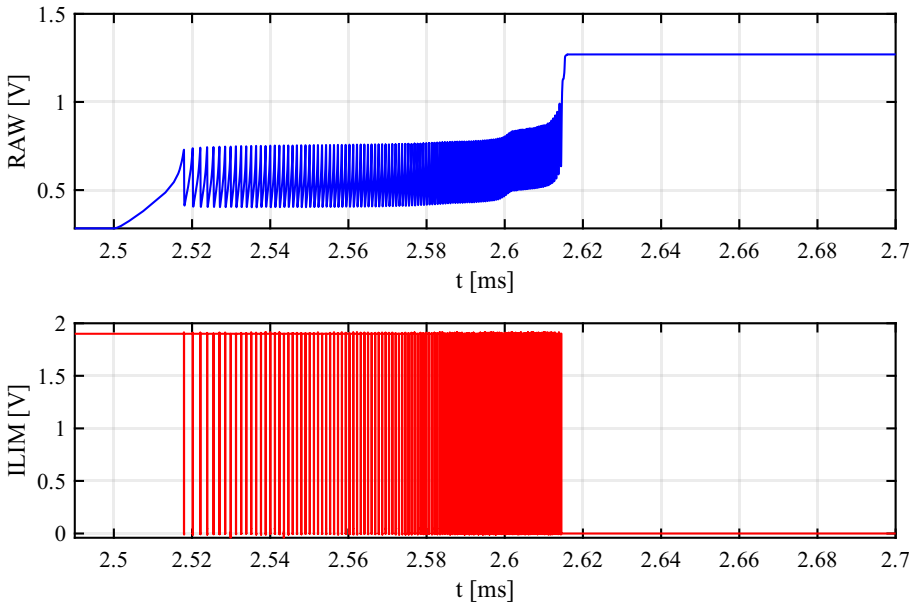


Figure 6.16: Simulation result of the RAW and ILIM signals when the stabilization mechanism is removed, with focus on the transition from the current limit condition to typical operation

The oscillations occur when the current flowing through the AVDD isolation switch decreases and approaches the programmed current-limit threshold. As soon as the comparator detects that the current has fallen below the threshold, the current-limiting action is removed, causing the switch current to increase again. This may immediately drive the circuit back into current-limit conditions, resulting in repeated transitions of the $ILIM$ signal around the switching point.

To prevent this behavior, a static hysteresis mechanism is introduced in the comparator stage. The reference current I_{REF}, which establishes the comparator threshold, is divided into two branches associated with $MN10$ and $MN11$. The current partitioning is chosen such that approximately 30% of the reference current flows through the $MN10$ branch, whose operation is controlled independently of the $MN11$ branch.
Referring to the final implementation shown in Fig. 6.13, when the $ILIM$ signal is asserted, the gate voltage of $MNC1$ is pulled low, turning the transistor off and removing the current contribution provided by the $MN10$ branch.

As a consequence, once the circuit has entered the current-limit condition, the comparator threshold is slightly shifted. The transition back to normal operation therefore occurs only when the current through the isolation switch has decreased sufficiently below the original threshold value.

This hysteretic behavior stabilizes the $ILIM$ signal and prevents spurious transitions around the current-limit boundary.

Additionally, to improve the robustness of the transition from the nominal operating condition to the current-limit state, a capacitor C_D is connected in feedback between the output of the Schmitt trigger and the RAW node, thereby introduc-

ing a dynamic hysteresis mechanism. The capacitor is sized such that, during the switching transient, the feedback action produces a rapid voltage step at the RAW node, reinforcing the state transition and preventing spurious oscillations around the comparator threshold.

SECOND STAGE of the NMOS DRIVER

The second stage of the proposed driver is responsible for generating the gate voltage applied to the isolation switch. A simplified representation of the circuit is shown in Fig. 6.17.

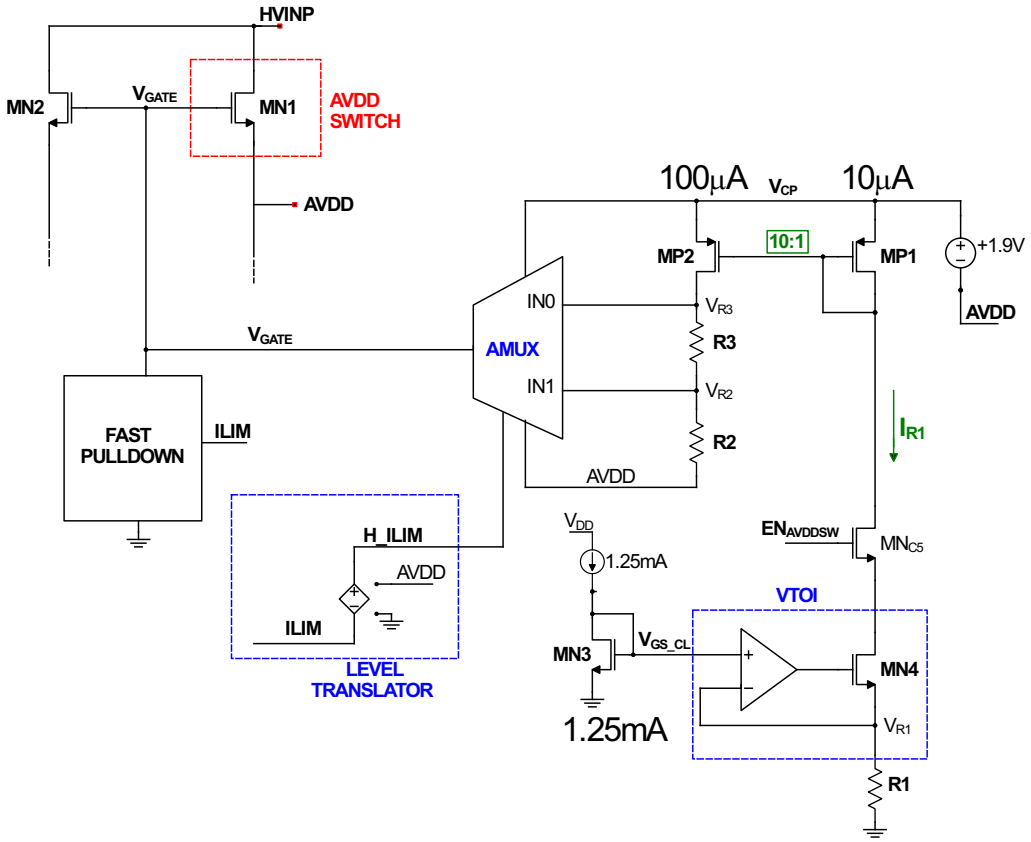


Figure 6.17: Second stage of the proposed NMOS driver architecture

The operating principle of this architecture is based on concepts already introduced in the previously discussed implementations. In particular, transistor $MN3$ is sized as a scaled replica of the isolation switch $MN1$, using the same scaling factor k adopted for $MN2$. The transistor is connected in a diode configuration and biased with a current equal to

$$\frac{I_{AVDD,max}}{k},$$

thus reproducing the gate-to-source voltage that the isolation switch would exhibit when conducting the maximum allowed current.

The voltage generated at the gate of $MN3$, denoted by $V_{GS,CL}$, is applied to the non-inverting input of an operational amplifier. The VTOI block reproduces the voltage $V_{GS,CL}$ at the source terminal of $MN4$. As a result, a current $I_{R1} = \frac{V_{GS,CL}}{R_1}$

is established in the branch containing $MN4$ and R_1. The value of R_1 is then selected such that a current of $10\,\mu$A flows through the branch.

The remaining circuitry is supplied by the charge-pump voltage

$$V_{CP} = AVDD + 1.9\,\mathrm{V},$$

which provides sufficient voltage headroom to generate a gate voltage above the source potential of the isolation switch. Since the branch containing R_1 spans the entire voltage range between V_{CP} and ground, the cascode transistor $MNC5$ performs the same function as the other cascode devices employed throughout the architecture, while also providing the disable functionality when the enable signal is deasserted.

The current mirror formed by $MP1$ and $MP2$ replicates the current flowing through R_1 with a mirror ratio of 10. Consequently, a current equal to $I_{R1} \cdot 10$ is forced through the branch containing resistors R_2 and R_3.

Two different gate-drive voltages are therefore generated and applied to the inputs of the analog multiplexer (AMUX), corresponding to the two operating modes of the isolation switch.

The voltage applied to input $IN1$ is denoted by V_{R2} and can be expressed as

$$V_{R2} = AVDD + \Delta V_{R2}.$$

Since the current mirrored through $MP2$ is equal to $10I_{R1}$, choosing $R_2 = \frac{R_1}{10}$ results in a voltage drop across R_2 (ΔV_{R2}) identical to that across R_1. Therefore,

$$\Delta V_{R2} = V_{GS,CL}.$$

When the AMUX selects input $IN1$, the generated gate voltage forces

$$V_{GS,AVDD} = V_{GS,CL},$$

thereby reproducing the gate-to-source voltage corresponding to the current-limit operating point and constraining the current through the isolation switch to its maximum allowable value.

Conversely, the voltage applied to input $IN0$ is generated at the node V_{R3}, given by

$$V_{R3} = AVDD + \Delta V_{R2} + \Delta V_{R3}.$$

Since ΔV_{R2} is already equal to $V_{GS,CL}$, resistor R_3 is appropriately sized such that the additional voltage drop ΔV_{R3} produces

$$V_{GS,AVDD} = V_{R3} - AVDD = 1.5\,\mathrm{V}.$$

As a result, when input $IN0$ is selected, the isolation switch is driven under nominal operating conditions.

The output signal $ILIM$ generated by the first stage is translated to the voltage domain of the AMUX through a level shifter and is then used as the multiplexer select signal. Consequently, when the current-limit condition is detected and $ILIM$ is asserted, input $IN1$ is selected and the gate voltage is forced to $V_{GS,AVDD} = V_{GS,CL}$. Conversely, when $ILIM$ is deasserted, input $IN0$ is selected and the gate-to-source voltage of the isolation switch is set to approximately 1.5 V, ensuring proper operation under nominal conditions.

The operation of the second stage was verified using the same simulation setup adopted for the analysis of the first stage. The testbench is configured so that the load current is initially set to $1A$. At $t = 1ms$, the load is linearly increased, causing the demanded current to rise from $1A$ to $10A$, which is reached at $t = 1.5ms$. The load is then kept constant until $t = 2.5ms$. Finally, between $t = 2.5ms$ and $t = 3ms$, the load is linearly reduced back to its initial value, restoring I_{AVDD} to $1A$.

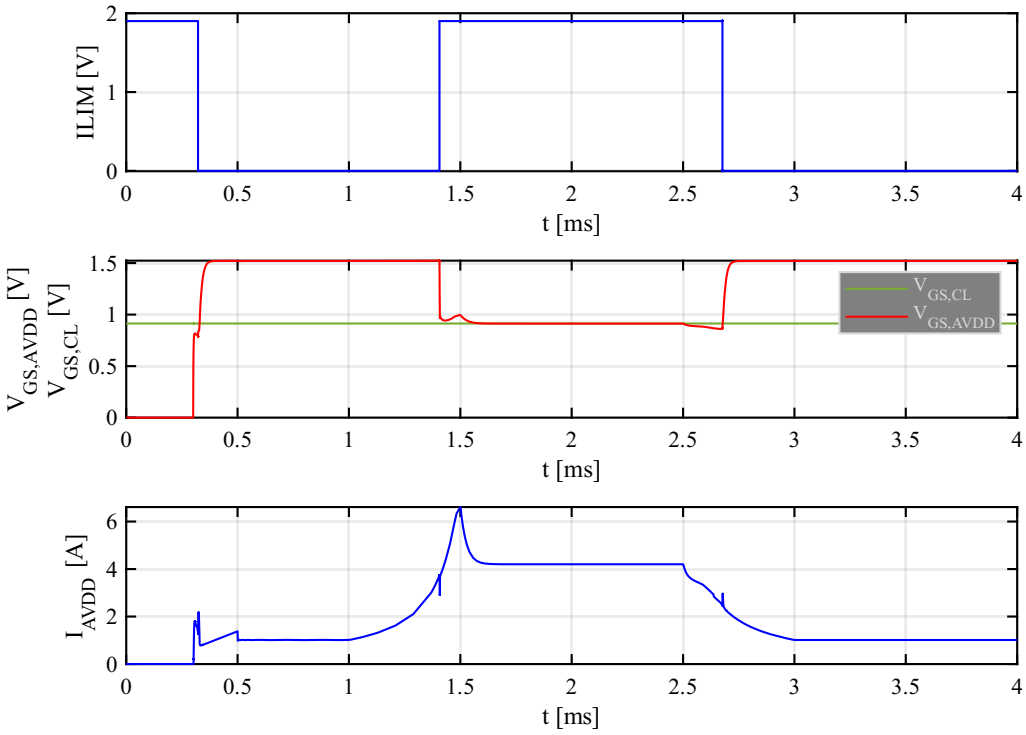


Figure 6.18: Simulation results of the proposed NMOS driver displaying the state transitions between normal and current limit condition of select signal $ILIM$, the gate-to-source voltage $V_{GS,AVDD}$ with respect to $V_{GS,CL}$ and the isolation switch current I_{AVDD}

Figure 6.18 verifies the operation of the second stage. Under nominal conditions, $ILIM$ is low and the AMUX selects the gate voltage required to obtain $V_{GS,AVDD} \approx 1.5\,\text{V}$. When the current-limit condition is detected, $ILIM$ switches high and $V_{GS,AVDD}$ is forced to $V_{GS,CL}$, limiting the current through the isolation switch to approximately 4 A. After the overload is removed, the driver automatically returns to the nominal operating condition.

As shown in Fig. 6.17, the final architecture includes an additional circuit block connected to the gate of the isolation switch, which implements a dedicated fast pull-down function. This block was introduced to address a critical issue associated with the relatively high impedance at the gate node, which results in a slow discharge of the gate-to-source voltage of transistor MN1 during the transition into the current-limit condition.

A slow reduction of the $V_{GS,AVDD}$ implies that the isolation switch continues to operate close to its nominal conduction state while the load current is rapidly increasing. Consequently, the current flowing through the device may significantly exceed the intended current-limit threshold before the gate voltage reaches its current-limit value. The resulting current overshoot depends on the load conditions and can substantially increase the electrical stress experienced by the isolation switch.

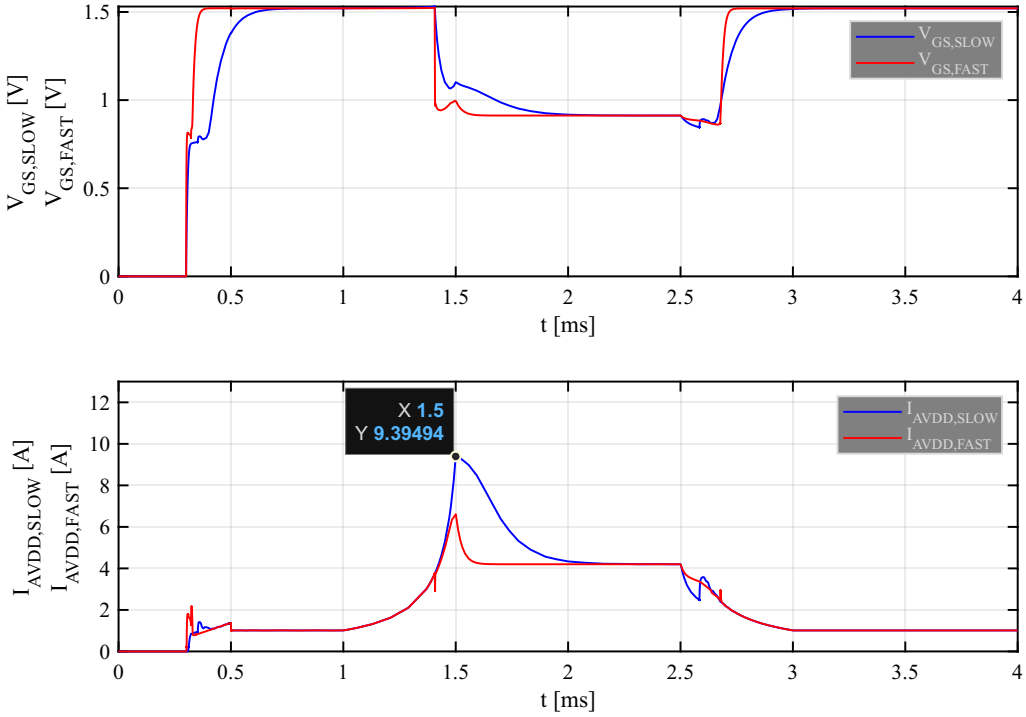


Figure 6.19: Simulated transition into the current-limit condition, comparing the final implementation with an architecture that does not include the fast pull-down mechanism and exhibits a higher gate-node impedance.

To highlight this effect, the simulation results shown in Fig. 6.19 were obtained under the same operating conditions used for Fig. 6.18. The figure illustrates the impact of a slow transition of $V_{GS,AVDD}$ on the current flowing through the isolation switch.

As can be observed, when the transition of $V_{GS,AVDD}$ from its nominal operating value to $V_{GS,CL}$ occurs slowly, the isolation switch remains highly conductive and the device current continues to increase. As a result, I_{AVDD} reaches a peak value of approximately 9.4A before the current-limiting action becomes effective.

To mitigate this overshoot two methods were employed.

First, the impedance seen at the V_{GATE} node was reduced. For this purpose, the mirror ratio of transistors MP1 and MP2 was increased from its original value of 1:1 to 10:1. This modification biases the branch containing R2 and R3 with a current of approximately $100\mu A$, allowing the value of R2 to be reduced by a factor of ten with respect to R1 while maintaining the same voltage drop. Consequently, the value of R3 can also be reduced, lowering the RC time constant associated with the gate node and accelerating the voltage transition.

Second, the above-mentioned fast pull-down circuit was introduced, as shown in Fig. 6.20.

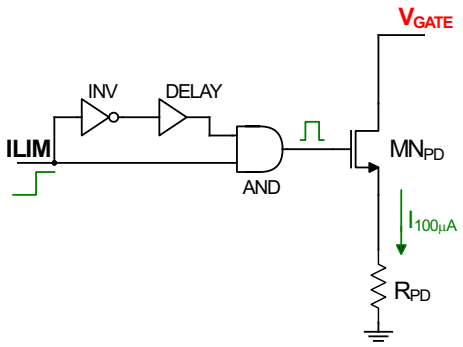


Figure 6.20: Fast pull-down circuit used to accelerate the transition into current-limit operation

When the signal $ILIM$ transitions high, a short pulse generated by the delay network temporarily turns on transistor MN_{PD}. As a consequence, a current of approximately $100\mu A$ is drawn from the V_{GATE} node, accelerating the discharge of the isolation-switch gate capacitance and therefore the transition toward $V_{GS,CL}$.

The effectiveness of these modifications is demonstrated in Fig. 6.19. Thanks to the combined reduction of the gate-node impedance and the action of the fast pull-down circuit, the peak current is reduced to approximately 6.5A, significantly lower than the 9.4A obtained in the absence of these measures.

The simulation results presented in this section demonstrate the correct functionality of the proposed NMOS driver and validate the effectiveness of the techniques introduced to improve its transient response and current-limiting behavior.

Beyond its functional correctness, the proposed architecture also addresses the major limitations identified in the complementary implementation discussed in Section 6.2. Therefore, the following section highlights the key advantages of the proposed solution.

6.3.2 Advantages of the Proposed Architecture

The proposed architecture successfully overcomes the two main limitations identified in the complementary implementation.

The first improvement concerns the available voltage headroom. In the com-

plementary architecture, the entire driver was supplied between the charge pump voltage V_{CP} and the output voltage $AVDD$, resulting in an effective operating range of only approximately 1.8 V. Since about 1.5 V were already required to generate the nominal gate-to-source voltage of the isolation switch, very little voltage remained available to properly bias the remaining circuitry, making the overall operation sensitive to process variations and mismatch.

In the proposed solution, the comparison stage is instead referenced between $HVINP$ and ground, providing a substantially larger voltage range and therefore considerably improving the robustness of the biasing conditions. The charge-pump voltage V_{CP} is only required by the gate-driving stage, where it is used exclusively to generate the gate voltage needed to drive the isolation switch.

A second advantage is related to the current required from the charge pump. In the complementary implementation, the large reference current needed to establish the current-limit threshold was directly supplied by the charge pump, resulting in a current demand incompatible with a practical fully integrated implementation.

In the proposed architecture, the current required by the sensing stage is instead drawn from the converter itself through the $HVINP$ node. Although the reference current reaches approximately 1.15 mA, this current is no longer provided by the charge pump. Similarly, the current used to bias the replica transistor $MN3$ is supplied by the VDD rail. As a result, the current required by the charge-pump is reduced to approximately 110 μA, nearly a twentyfold reduction with respect to the complementary NMOS implementation, making the circuit fully compatible with integrated implementation.

In summary, the proposed architecture demonstrates that both the driving and current-protection functions required by an NMOS isolation switch can be implemented in a manner compatible with the pinless boost-converter architecture proposed in this work. By addressing the limitations of the complementary implementation, the presented solution enables the practical adoption of an NMOS isolation device, thereby completing the transition from the original PMOS-based approach to the proposed NMOS-based converter architecture.

The results presented so far demonstrate the nominal operation of the proposed driver architecture. To further validate the solution, the next chapter investigates its ability to maintain its performance under process variations, device mismatch, and temperature extremes. The analysis aims to evaluate the impact of fabrication non-idealities on the circuit performance and to verify the reliability of the proposed implementation.

Chapter 7

Stability and Accuracy Analysis of the NMOS Driver Architecture

The analyses presented in the previous chapter demonstrated the nominal operation of the proposed NMOS gate-driver architecture. However, the practical implementation of the circuit also requires adequate tolerance to process variations, device mismatch, and temperature-dependent effects.

The reliability assessment is carried out by investigating the main functional blocks of the architecture individually. This approach allows the dominant sources of error and sensitivity to be identified and quantified. In particular, Monte Carlo, corner, and stability analyses are performed to verify the correct operation of the VTOI block and the gate-voltage generation stage in the presence of process variations, device mismatch, and temperature-dependent effects.

Finally, particular attention is devoted to the accuracy of the current-limit threshold generated by the comparator stage, since this parameter directly determines the protection capability of the proposed NMOS isolation-switch driver.

7.1 VTOI Stability and Mismatch Analysis

The VTOI block, shown in Fig. 7.1, consists of an operational amplifier whose non-inverting input is connected to the voltage $V_{GS,CL}$, while the inverting input senses the source voltage of transistor $MN4$. The amplifier output drives the gate of $MN4$, forming a feedback loop whose purpose is to reproduce the voltage $V_{GS,CL}$ at the node denoted as V_{R1}.

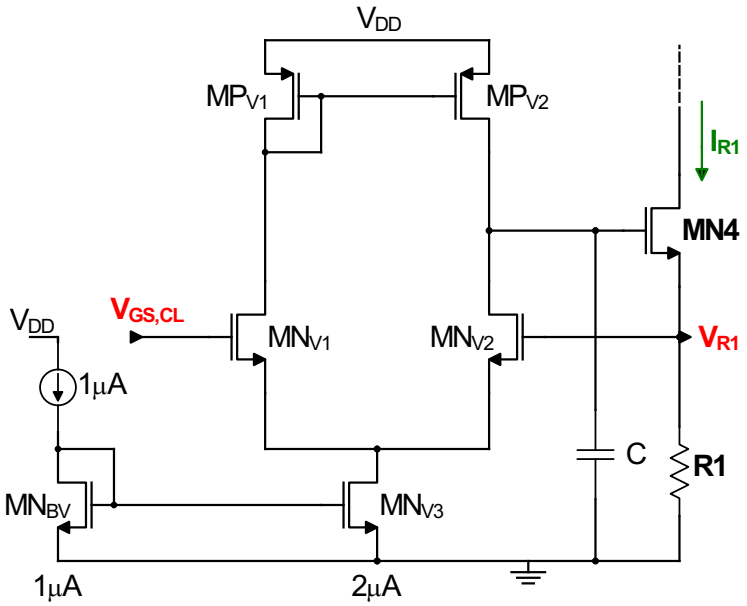


Figure 7.1: Schematic of the VTOI block used to reproduce the reference voltage $V_{GS,CL}$ at the output node V_{R1}

The accuracy of the VTOI block was evaluated through Monte Carlo, corner, and stability analyses performed at three different temperatures: room temperature (27°C), low temperature (−40°C), and high temperature (125°C).

Monte Carlo simulations including both process variations and device mismatch were performed to evaluate the accuracy of the generated voltage $V_{GS,CL}$, the voltage difference $V_{R1} - V_{GS,CL}$, and the current I_{R1}. The results obtained at the three operating temperatures are summarized in Table 7.1.

Test	Temperature [°C]	Min	Max	Mean	Std Dev
V_GS,CL	27	837 mV	987.7 mV	912.7 mV	47.42 mV
V_GS,CL	-40	853.6 mV	999.6 mV	926.9 mV	46.05 mV
V_GS,CL	125	815 mV	972.5 mV	894 mV	49.5 mV
V_R1-V_GS,CL	27	-2.037 mV	1.473 mV	-191.8 µV	873.2 µV
V_R1-V_GS,CL	-40	-1.908 mV	1.646 mV	-39.76 µV	907.1 µV
V_R1-V_GS,CL	125	-2.251 mV	1.14 mV	-442 µV	840.6 µV
I_R1	27	8.169 µA	12.23 µA	10.12 µA	1.095 µA
I_R1	-40	8.207 µA	12.28 µA	10.12 µA	1.108 µA
I_R1	125	8.051 µA	12.12 µA	10.04 µA	1.09 µA

Table 7.1: Summary of Monte Carlo simulation results for the VTOI block, reporting the statistical variation of $V_{GS,CL}$, $V_{R1} - V_{GS,CL}$, and I_{R1} across process, mismatch, and temperature variations

Particular attention is devoted to the standard deviation of $V_{GS,CL}$, since this voltage ultimately determines the current-limit threshold imposed by the second stage of the driver. The obtained variation remains sufficiently small not to produce a significant deviation of the programmed current limit. Similarly, the variation of the current I_{R1} remains within acceptable bounds.

Most importantly, the Monte Carlo results demonstrate that the translation of the voltage $V_{GS,CL}$ to the node V_{R1} is highly reliable. The standard deviation of the voltage difference $V_{R1} - V_{GS,CL}$ remains below 1 mV across all considered temperatures, indicating excellent tracking accuracy. Referring to Fig. 6.17, this result confirms that the voltage drop across resistor R_1 accurately reproduces $V_{GS,CL}$, as required by the operating principle of the gate-voltage generation stage.

Finally, the stability of the VTOI loop was verified through AC analysis performed across different process corners. This analysis is used to evaluate the stability of the feedback loop by determining the phase and gain margins under process-induced variations of transistor parameters. The considered corners include the nominal case (TNTN), where both NMOS and PMOS devices exhibit typical characteristics, as well as worst-case combinations such as WNWP, corresponding to weak NMOS transistors and weak PMOS transistors.

The most critical condition was found to be the WNWP corner. Nevertheless, the simulation shown in Fig. 7.2 displays that the loop exhibits a phase margin of 75.82° and a gain margin of 33.65 dB, indicating stable operation with a comfortable stability margin.

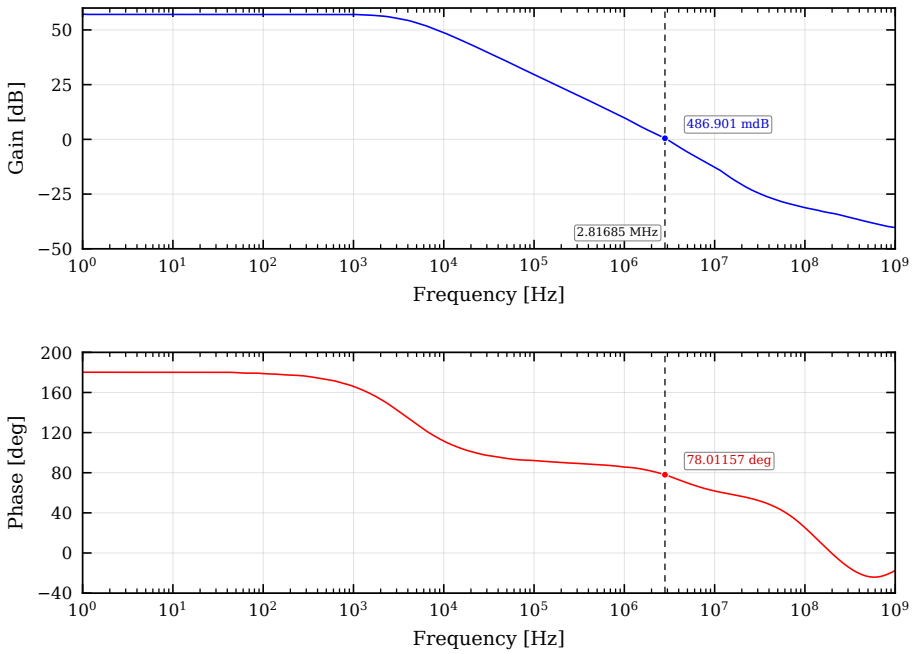


Figure 7.2: Bode plot of the VTOI feedback loop used to extract the phase margin and gain margin of the proposed implementation

The VTOI block can therefore be considered reliable against both process variations and mismatch effects.

7.2 Gate driver Monte Carlo and mismatch analysis

Having analyzed the individual contribution of the VTOI block, the accuracy assessment is extended to the remaining functional blocks of the second stage responsible for generating the gate voltage of the isolation switch (Fig. 6.17).

Particular attention is devoted to the matching between resistors R_1 and R_2, as well as to the accuracy of the current mirror formed by transistors $MP1$ and $MP2$. Finally, Monte Carlo simulations of the complete gate-voltage generation stage are presented to verify that the voltage generated at the output accurately reproduces the reference voltage established by the replica transistor $MN3$.

The first analysis focuses on the matching between resistors R_1 and R_2. Their accuracy is critical because the voltage drop generated across R_1, which corresponds to the gate-to-source voltage imposed on the isolation switch under current-limit conditions, must be faithfully reproduced across R_2 and subsequently transferred to the output of the stage.

To evaluate the matching accuracy, Monte Carlo simulations including both process variations and device mismatch were performed at the three temperatures previously considered (27°C, −40°C, and 125°C). A simple testbench was used in which a voltage of 1 V was applied across each resistor while their corresponding currents were monitored.

Test	Temperature [°C]	Min	Max	Mean	Std Dev
RATIO	27	9.947	10.05	10	24.1 m
RATIO	-40	9.947	10.05	10	24.1 m
RATIO	125	9.947	10.05	10	24.1 m
I_R2	27	95.8 µA	131.2 µA	110.0 µA	10.54 µA
I_R2	-40	94.27 µA	128.6 µA	109.2 µA	10.57 µA
I_R2	125	97.06 µA	133.2 µA	112.3 µA	10.57 µA
I_R1	27	9.575 µA	13.1 µA	11.09 µA	1.054 µA
I_R1	-40	9.421 µA	12.85 µA	10.92 µA	1.058 µA
I_R1	125	9.7 µA	13.3 µA	11.24 µA	1.058 µA

Table 7.2: Monte Carlo analysis of the resistor matching network showing the statistical variation of I_{R1}, I_{R2}, and their ratio

The results reported in Table 7.2 show that the ratio between the currents flowing through R_2 and R_1 exhibits a very small standard deviation of $< 0.3\%$ over all operating conditions. Consequently, the resistor pair demonstrates excellent matching properties and does not represent a significant source of error for the gate-voltage generation stage.

As a second step, the accuracy of the current mirror formed by $MP1$ and $MP2$ was investigated. For this purpose, Monte Carlo simulations were performed on an isolated testbench containing only the two transistors configured as a current mirror. The currents flowing through $MP1$ and $MP2$, together with the resulting mirror ratio, were monitored.

Test	Temperature [°C]	Min	Max	Mean	Std Dev
I_MP2	27	81.94 µA	121.3 µA	101 µA	10.77 µA
I_MP2	-40	82.24 µA	121.6 µA	101 µA	10.86 µA
I_MP2	125	80.89 µA	120.4 µA	100.3 µA	10.76 µA
I_MP1	27	8.205 µA	12.24 µA	10.12 µA	1.093 µA
I_MP1	-40	8.24 µA	12.29 µA	10.12 µA	1.103 µA
I_MP1	125	8.092 µA	12.13 µA	10.04 µA	1.091 µA
MIRR_RATIO	27	9.911	10.03	9.981	24.88 m
MIRR_RATIO	-40	9.897	10.03	9.975	27.63 m
MIRR_RATIO	125	9.927	10.03	9.989	22.43 m

Table 7.3: Monte Carlo analysis of the current mirror formed by $MP1$ and $MP2$, reporting the statistical variation of the mirrored currents and mirror ratio

The corresponding results are summarized in Table 7.3. In particular, the parameter $MIRR_RATIO$ shows a very limited variation across process, mismatch, and temperature conditions (std. dev. $< 0.3\%$). The low standard deviation confirms the good matching properties of the mirror transistors and validates the current-scaling mechanism adopted in the proposed architecture.

Referring to Fig. 6.17, the final step of the analysis evaluates the accuracy of the complete gate-voltage generation stage. Monte Carlo simulations were performed to monitor the voltages $V_{R3} - AVDD$, denoted as $V_{GS,\mathrm{NOCL}}$, and $V_{R2} - AVDD$, denoted as $V_{GS,\mathrm{CL}}$. These quantities correspond to the gate-to-source voltages applied to the isolation switch during normal operation and under current-limit conditions, respectively. In addition, the mismatch between the voltage drop generated across R_2 and the reference voltage $V_{GS,\mathrm{CL}}$ was evaluated through the parameter $\Delta V_{GS,\mathrm{CL}}$. Likewise, the quantity $\Delta V_{GS,\mathrm{NOCL}}$ was used to measure the difference between $V_{GS,\mathrm{NOCL}}$ and $V_{GS,\mathrm{CL}}$.

Test	Temperature [°C]	Min	Max	Mean	Std Dev
ΔV_GS,CL	27	-9.206 mV	3.653 mV	-1.654 mV	2.906 mV
ΔV_GS,CL	-40	-10.37 mV	3.501 mV	-2.38 mV	3.134 mV
ΔV_GS,CL	125	-7.7 mV	4.083 mV	-627.5 µV	2.709 mV
ΔV_GS,NOCL	27	558 mV	651.4 mV	605.5 mV	30.25 mV
ΔV_GS,NOCL	-40	567.6 mV	658.8 mV	613.8 mV	29.18 mV
ΔV_GS,NOCL	125	545.2 mV	643.3 mV	594.7 mV	31.81 mV
V_GS,NOCL	27	1.398 V	1.645 V	1.518 V	79.37 mV
V_GS,NOCL	-40	1.425 V	1.663 V	1.541 V	76.83 mV
V_GS,NOCL	125	1.362 V	1.622 V	1.489 V	83.13 mV
V_GS,CL	27	837.2 mV	993.6 mV	912.6 mV	49.27 mV
V_GS,CL	-40	853.7 mV	1.005 V	926.9 mV	47.84 mV
V_GS,CL	125	815.2 mV	978.7 mV	894 mV	51.45 mV

Table 7.4: Monte Carlo results of the complete gate-voltage generation stage, including $V_{GS,\mathrm{CL}}$, $V_{GS,\mathrm{NOCL}}$, $\Delta V_{GS,\mathrm{CL}}$, and $\Delta V_{GS,\mathrm{NOCL}}$

The Monte Carlo results reported in Table 7.4 show that the standard deviation of $\Delta V_{GS,\mathrm{CL}}$ remains limited to only a few millivolts across all considered temperatures. This confirms that the voltage generated by the replica transistor $MN3$ is accurately reproduced at the output of the gate-voltage generation stage when the circuit operates in current-limit mode.

As expected, the average value of $\Delta V_{GS,\mathrm{NOCL}}$ is approximately 0.6 V. This corresponds to the intentional voltage offset introduced by resistor R_3, which increases the gate-to-source voltage from the current-limit value to approximately 1.5 V, thereby ensuring the correct operating condition of the isolation switch during normal operation.

Overall, the obtained results demonstrate that the gate-voltage generation stage is reliable against process variations, device mismatch, and temperature changes. Both the resistor network and the current mirror accurately reproduce the intended voltage relationships, ensuring reliable generation of the gate voltage in both nominal and current-limit operating conditions.

7.3 Current limit comparator accuracy analysis

The final analysis concerns the first stage of the driver architecture, and in particular the comparator threshold used to detect the current-limit condition.

As discussed in Section 6.3.1, the reference current I_{REF} used to establish the comparator threshold is intentionally selected slightly below the target current limit imposed on the isolation switch. In the proposed implementation, the threshold is designed to detect the onset of current limiting when the current through the isolation switch reaches approximately 3.7 A.

Similarly to the analyses performed for the second stage, Monte Carlo simulations including both process variations and device mismatch were carried out at three operating temperatures (27°C, −40°C, and 125°C) in order to evaluate the robustness of the threshold detection mechanism. The testbench was configured such that the load transitions from a condition corresponding to $I_{AVDD} = 1\,\mathrm{A}$ to $I_{AVDD} = 10\,\mathrm{A}$ between 1 ms and 1.5 ms. The results are summarized in Table 7.5.

Test	Temperature [°C]	Min	Max	Mean	Std Dev
IAVDDSW_TH	27	3.648 A	3.856 A	3.738 A	45.25 mA
IAVDDSW_TH	-40	3.609 A	3.874 A	3.727 A	56.63 mA
IAVDDSW_TH	125	3.685 A	3.83 A	3.75 A	35.74 mA

Table 7.5: Monte Carlo analysis of the current-limit detection stage showing the variation of the trigger current $IAVDDSW_TH$

The parameter $IAVDDSW_TH$ corresponds to the value of the isolation-switch current at which the current-limit condition is detected. As expected, the average value of $IAVDDSW_TH$ remains close to the target threshold of approximately 3.75 A across all temperatures, while exhibiting a relatively small standard deviation.

For protection circuits, a typical accuracy target is on the order of $6\sigma = \pm 10\%$. From the obtained results, a standard deviation of approximately $1\sigma = 1.76\%$ can be extracted, corresponding to a 6σ spread of about 10.6%. Therefore, the detected current-limit threshold falls within an acceptable accuracy range for the intended protection function.

The analyses presented in this chapter demonstrate that the proposed NMOS gate-driver architecture is robust against process variations, device mismatch, and temperature changes. The VTOI block accurately reproduces the reference voltage, while the gate-voltage generation stage preserves the intended voltage relationships with limited statistical variation. Furthermore, the current-limit detection stage maintains an accurate threshold, ensuring reliable activation of the protection mechanism. Overall, the obtained results validate the robustness of the proposed implementation and confirm the correct operation of both the gate-drive and current-limiting functions under realistic fabrication and operating conditions.

Chapter 8

Conclusion and Future Perspectives

This thesis addressed the problem of silicon-area optimization of the isolation-switch architecture adopted in OLED boost converters. Starting from the analysis of the existing PMOS-based implementation, the main mechanisms governing the operation of the isolation switch and its driving circuitry were investigated in order to identify the limitations and opportunities for improvement.

The study of the original architecture highlighted the characteristics that differentiate it from a solution based on an NMOS isolation switch and the removal of the HVINP pin together with its external capacitor. These modifications represent the key enablers of the proposed area-reduction strategy, making it possible to achieve a more area-efficient converter implementation while preserving the required functionality.

As a first step, the selection and sizing of the NMOS isolation switch were carried out in order to identify a suitable replacement for the original PMOS device. Particular attention was devoted to the current-handling capability and operating conditions of the selected transistor, which ultimately established the requirements for the gate-driver architecture.

Subsequently, the design of a dedicated NMOS gate driver was investigated. The analysis of the existing PMOS driver and of its complementary NMOS implementation provided valuable insight into the challenges introduced by the new converter architecture. In particular, the removal of the HVINP pin and the resulting increase in the current flowing through the isolation switch imposed new constraints on the current-limiting function and on the overall driver implementation. Furthermore, the adoption of an NMOS isolation switch required the generation of a boosted gate-drive voltage through an integrated charge pump, whose limited current-delivery capability became a critical design constraint for the proposed driver architecture.

Based on these observations, a new gate-driver implementation for the NMOS isolation switch was proposed. The operating principle of the solution was analyzed in detail and validated through extensive simulations. The proposed architecture was shown to overcome the limitations of the complementary implementation while

maintaining compatibility with an integrated charge-pump solution.

Furthermore, dedicated accuracy analyses demonstrated the correct operation of both the gate-voltage generation stage and the current-limit detection circuitry in the presence of process variations, mismatch, and temperature changes.

Overall, the results presented in this work demonstrate the feasibility of replacing the conventional PMOS isolation-switch solution with an NMOS-based implementation while removing the external HVINP pin. The proposed modifications enable a significant reduction of the silicon area required by the converter and contribute to the development of a more area-efficient solution for OLED applications.

Future work may focus on the integration of the proposed driver architecture within the complete boost-converter system. While the operation of the driver has been extensively validated as a standalone block, further investigations could evaluate its interaction with the converter dynamics and the resulting closed-loop behavior. In addition, several building blocks that were modeled ideally throughout this work, such as the charge pump and the level translators, could be replaced by fully implemented circuit solutions and analyzed within the complete system. These developments would provide further validation of the proposed architecture and support its practical integration into future products.

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