UNIVERSITÀ
DI PAVIA

UNIVERSITY OF PAVIA

FACULTY OF ENGINEERING

Department of Electrical, Computer and Biomedical Engineering

Master Thesis in Industrial Automation Engineering

Design and Implementation of a High-Precision Hardware Characterization Platform for the LEMX-DC 32-Channel A/D Converter

Supervisor:

Prof. Marco Grassi

Co-Supervisor:

Ali Marzdar

Jacopo Giani

Prof. Piero Malcovati

Master thesis of:

Masoud Zargari
Matr. 491354

Academic Year 2024/2025

Abstract

This thesis presents the design, implementation, and verification of a dedicated hardware characterization platform for the **LEMX-DC**, a 32-channel incremental Delta-Sigma Analog-to-Digital Converter (ADC). Following the strategic guidelines provided by the design team, this work establishes a robust experimental infrastructure required for the physical validation of the ASIC, bridging the gap between theoretical simulation and silicon reality.

The core of this research is the development of a test bench PCB designed for high-fidelity testing. The analog interface incorporates high-impedance buffers to ensure signal integrity during characterization. This platform provides the necessary tools for measuring key parameters such as SINAD and linearity, ensuring the hardware meets its design specifications under real laboratory conditions.

Contents

Introduction

The design of integrated electronic systems for scientific space instrumentation is subject to unique constraints in terms of power consumption, area, configurability, and robustness. In particular, analog signal processing chains must be capable of operating reliably in harsh environments, while maintaining high precision and flexibility in the acquisition and digitization of sensor data, as illustrated in Figure 1. This thesis is developed within the framework of the *Lunar Electromagnetic Monitor in X-rays* (LEM-X) project, which includes the design of a dedicated analog-to-digital converter, named, LEMX-DC for X-ray spectroscopy. This *Application Specific Integrated Circuit* (ASIC) is intended to interface with *Silicon Drift Detectors* (SDDs) through a front-end signal conditioning chain and to perform event-driven conversion of the analog outputs. The converter must be compact and reconfigurable, supporting multi-channel operation with strict constraints on timing and accuracy. The work presented in this thesis focuses on the development and verification of two analog subsystems involved in the LEM-X readout chain. The first is the incremental ADC core integrated in the LEMX-DC chip, managed by dedicated digital control logic responsible for sequencing and synchronization. The second is a fully differential output buffer, redesigned as part of the analog front-end (VEGA2 chip), with the aim of improving the dynamic range and ensuring stability under *Process-Voltage-Temperature* (PVT) variations. Particular attention was paid to the implementation of a continuous-time *Common-Mode FeedBack* (CMFB) loop, essential for proper bias control in fully differential configurations. The methodology adopted includes analytical modeling, schematic-level design, and simulation-based validation of the circuits under nominal and non-typical conditions. The implementation choices were guided by considerations of modularity, energy efficiency, and integration within the broader front-end system. The thesis is organized as follows. Chapter 1 introduces the context of the EMM project and presents the architecture of the LEM-X system. Chapter 2 describes the analog front-end (VEGA2) and the structure of the LEMX-DC. Chapter 3 focuses on the design of the incremental ADC and the associated control logic. Chapter 4 presents the design of the analog buffer and the CMFB circuit. Chapter 5 concludes the work with a summary of the simulation results and a discussion of possible future developments.

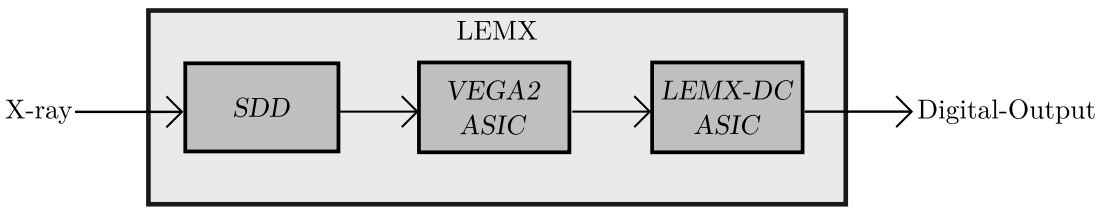

Figure 1: Overview of the LEM-X signal acquisition chain.

Chapter 1

Introduction to LEMX-DC

The *Earth-Moon-Mars* (EMM) project is an initiative funded under the framework of the *Piano Nazionale di Ripresa e Resilienza* (PNRR) (*National Recovery and Resilience Plan*), with the objective of promoting the scientific exploitation of the Moon as an observation platform and as a research base for planet Mars study activities. The proposal falls under *Mission 4 "Education and Research"*, *Component 2 "From Research to Business"*, *Investment Line 3.1 "Strengthening and Creation of Research Infrastructures"* [1]. The project is coordinated by the *National Institute for Astrophysics* (INAF), with the participation of the *Italian Space Agency* (ASI) and the *National Research Council* (CNR). The initiative is based on the concept of using the Moon as a strategic site for observing the Earth and the Universe, while simultaneously supporting research and development activities dedicated to the study of the planet Mars. The main objectives of the EMM project include:

- The creation of a communication infrastructure between Earth, Moon, and Mars;
- The study of the Moon as a scientific laboratory for observing the Earth and the Universe;
- The development of innovative instruments for scientific missions to be installed on lunar infrastructures;
- The implementation of a hardware and software infrastructure dedicated to the study of planetary atmospheres, comprising advanced computing, storage, and processing systems;
- The training of a new generation of scientists and engineers;
- The construction of a national network connecting research institutions and industry, aimed at strengthening synergies and optimizing resource utilization [1].

1.1 Scientific Objectives and System Role of LEM-X

The *Lunar Electromagnetic Monitor in X-rays* (LEM-X) is an instrument designed for sky observation in the energy range between 2 and 50 keV. Its primary goal is the continuous monitoring of the celestial sphere (*All Sky Monitor*), with particular focus on the detection of transient X-ray events such as *Gamma-Ray Bursts* (GRBs), which represent one of the electromagnetic counterparts of gravitational wave sources. LEM-X is part of the so-called multi-messenger astronomy, an observational paradigm that combines electromagnetic signals, gravitational waves, and particles for the study of extreme astrophysical phenomena. The scientific relevance of LEM-X lies in its ability to contribute directly to this observational synergy, thanks to its wide sky coverage and high sensitivity in the X-ray band [2]. From a technological perspective, the instrument is based on *Silicon Drift Detectors* (SDDs), a technology developed in Italy that has

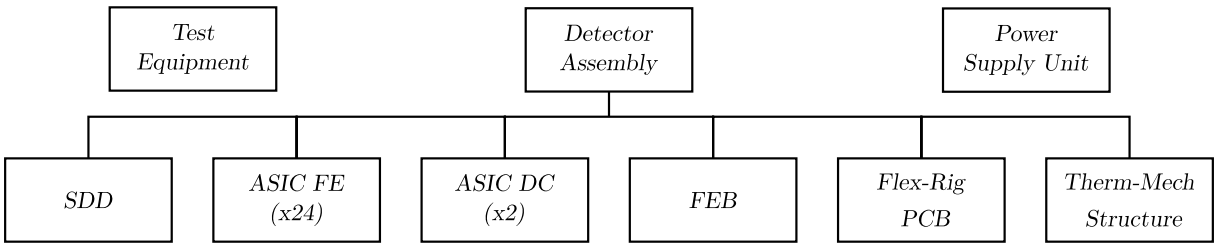

Figure 1.1: Functional architecture of the LEM-X system.

reached a high level of maturity, also thanks to the experience gained in space projects such as HERMES and eXTP [2]. The system has been designed to operate under the extreme environmental conditions typical of the lunar surface, where it must withstand challenges such as large thermal excursions, radiation from high-energy particles, micrometeoroid impacts, and lunar dust. For this reason, the instrumentation was developed with specific criteria for robustness and reliability, and its technical requirements were tailored to ensure environmental compatibility throughout the entire mission duration [2].

1.2 LEM-X System Architecture and Role of the ASIC DC

The architecture of the LEM-X system is organized into four modules called *Detector Assemblies* (DAs), each of which integrates a complete chain for the detection and digitization of X-ray signals. Each DA includes a *Front-End Board* (FEB) that hosts:

- a Silicon Drift Detector (SDD);
- 24 analog *Front-End Application Specific integrated circuits* (ASIC FEs);
- a digital *Application Specific Integrated Circuit for analog-to-digital conversion* (ASIC DC).

The functional composition of the system is illustrated Figure. 1.1. The SDD detects the incident photon and produces a charge signal proportional to the deposited energy. The ASIC FEs perform analog signal processing (amplification, shaping, discrimination), while the ASIC DC is responsible for digitizing the information to enable subsequent processing and transmission. This distributed architecture allows for in situ analog-to-digital conversion, minimizing susceptibility to disturbances and reducing the losses that would occur when transmitting analog signals over long distances. The ASIC DC, also referred to as LEMX-DC, is positioned immediately downstream of the analog front-end chain. Its role is to perform the sequential conversion of signals from 32 channels per ASIC FE, interfacing with the multiplexed outputs through pseudo-differential connections. It also integrates the digital logic required to manage the conversion sequence and synchronize with the higher-level data acquisition subsystems. The DA modules constitute the fundamental functional blocks of the LEM-X system. Their configuration complies with environmental compatibility, mechanical robustness, and thermal optimization constraints imposed by lunar operating conditions [2]. Functionally, the ASIC DC acts as the bridge between the analog signals generated by the detector chain and the digital domain where data are processed and transmitted.

1.3 Technological Choice for Space Qualification

The choice of the ASIC fabrication technology represents a crucial step in the early phase of the project, as it directly affects key aspects such as electrical compatibility with other system

blocks, frequency performance, power consumption, and robustness in space environments. In the case of the LEM-X system, the signals to be digitized originate from the VEGA2 front-end ASICs, whose output buffers operate with a voltage swing compatible with a 3.3 V supply. The analog-to-digital converter (ASIC DC) must therefore be capable of directly interfacing with these signals while maintaining low power consumption and ensuring proper operation in the presence of ionizing radiation. An additional fundamental constraint is the maximum conversion time: each ADC array must convert 32 channels per front-end ASIC within a maximum time of 80 µs. Considering an architecture distributed across two ASIC DCs, this translates into a required per-channel conversion speed of at least 400 kS/s [2]. For the preliminary evaluation, three different CMOS technologies were considered: 0.35 µm, 65 nm, and 28 nm [3]. The first option, based on 0.35 µm CMOS with a 3.3 V supply, offers the advantage of full compatibility with the output swing of the analog front-end, thus avoiding the need for attenuation or adaptation circuits. It is also a well-known technology for the design team, already employed in previous projects involving complex analog blocks, particularly with the AMS c35b4 platform. Its relatively low cost, combined with good radiation hardness, makes it especially suitable for space applications [4]. However, the use of a 3.3 V supply results in higher power consumption compared to more advanced solutions, and the achievable operating frequencies may be insufficient in scenarios where parallelism is minimized. The second alternative analyzed is the 65 nm CMOS technology, which offers a good compromise between speed and power consumption. Thanks to the availability of I/O libraries compatible with 3.3 V, signal compatibility can be maintained while powering the digital core at 1.2 V. This configuration would allow for a significant reduction in power dissipation, provided that the scaled voltage is supplied by an external DC-DC converter. This technology is also widely used in high-energy environments, particularly in CERN projects, where it has been validated for resistance to total ionizing dose and single-event effects. On the other hand, the introduction of a dual supply adds complexity at both the circuit and system level, and requires careful power budget verification to meet the project specifications. Finally, the 28 nm technology represents the most advanced solution in terms of integration and operating frequency. The smaller device dimensions would allow for a significant reduction in circuit area and eliminate the need for time-interleaving techniques. Power consumption would also be drastically lower compared to previous technologies. Nevertheless, there are critical issues that make this option less feasible: development costs are significantly higher, direct compatibility with 3.3 V signals is not guaranteed, and the technology is more sensitive to instability phenomena such as charge accumulation at the oxide edges in high-radiation environments. Moreover, a suitable peripheral library for interfacing with high-dynamic-range analog systems is not always available. In light of these considerations, the 0.35 µm CMOS technology supplied at 3.3 V was selected as the final solution for the implementation of the ASIC DC, as it represents the best trade-off between electrical compatibility, environmental robustness, design simplicity, and consistency with the team's existing expertise [4].

1.4 Thesis Structure and Concluding Remarks

The EMM project, and in particular the LEM-X instrument, defines a highly interdisciplinary application context, where scientific objectives, environmental constraints, and advanced technological requirements converge. Within this architecture, the integrated circuits developed for signal detection, processing, and conversion play a central role in ensuring the overall performance of the system. This thesis fits within this design framework, focusing on the development of two fundamental blocks: on one hand, the design and characterization of a fully differential two-stage analog buffer to be integrated into the VEGA2 front-end; on the other hand, the analysis and description of the digital control logic of the ASIC DC, which is responsible for

managing the conversion phase. These activities aim to improve the reliability, configurability, and overall efficiency of the acquisition chain, contributing to the optimization of key subsystems in the LEM-X system. The remainder of this chapter presents and analyzes the two ASIC circuits involved in the project and then discusses the incremental ADC design together with the architectural and logic choices underlying its development.

1.5 Architectural Overview of the VEGA2 and LEMX-DC ASICs

This chapter presents an architectural overview of the two integrated circuits that compose the analog front-end chain of the LEM-X system. The first is the VEGA2 front-end ASIC, responsible for the analog signal acquisition and processing performed immediately after detection. The second is the LEMX-DC chip, designed to carry out the analog-to-digital conversion and manage the digital interface and synchronization. Although the main focus of this thesis is the LEMX-DC design, the VEGA2 architecture is briefly introduced to clarify the signal flow and to provide context for the redesign of its output buffer, which was part of the development work. The description of the LEMX-DC architecture is then presented in detail, highlighting the design choices, functional blocks, and interface logic that enable reliable and reconfigurable conversion of multi-channel analog signals.

1.5.1 The VEGA2 Front-End ASIC

The VEGA2 integrated circuit, also referred to as the ASIC FE, is the analog front-end block responsible for reading the charge signals generated by a multi-anode silicon drift detector. It represents an optimized layout version specifically designed to minimize cross-talk between adjacent channels and to incorporate a serial communication interface for the configuration and readout of multiple ASICs in multi-chip instruments. Specifically designed for spaceborne spectroscopy applications within the LEM-X project, the circuit was implemented using a 0.35 µm CMOS technology (AMS C35B3C3), which provides radiation tolerance and operational robustness, as previously discussed in Chapter 1. The ASIC integrates a linear array of 32 independent *Anode Readout Channels* (ARCs), each connected to a detector anode via wire bonding. Each channel autonomously acquires the incoming signal from the detector, implementing a complete internal analog processing chain that includes: charge-to-voltage conversion, amplification, signal shaping, peak detection, and storage. This architecture provides high flexibility while improving the signal-to-noise ratio, thanks to design techniques such as functional partitioning, internal shielding, and power supply isolation between analog, mixed-signal, and digital domains. The *Peak-Detector and Hold* (PDH) block used in each channel is based on a recently published low-power, wide-dynamic-range architecture designed to hold the peak value of the shaped signal until reception of an *End-Of-Conversion* (EOC) signal [5]. Additionally, the circuit is capable of autonomously notifying the channel logic of peak detection, thereby improving timing accuracy and system efficiency. To reduce power consumption, each channel includes selective power-down functionality. This strategy allows non-essential blocks to be deactivated in the absence of events, significantly lowering overall power dissipation and ensuring a total current draw below 10 mW in the 8-channel active configuration. At the top level, the chip also integrates shared analog and digital blocks, including a *Proportional-To-Absolute-Temperature* (PTAT) reference, *Digital-to-Analog Converters* (DACs), global threshold generators, and analog output drivers. Output signals are converted into pseudo-differential format using a pair of single-ended buffers, ensuring compatibility with the external digitization stage, as already introduced in Chapter 1. From the digital standpoint, the ASIC is configurable through an *Serial*

Peripheral Interface (SPI), which enables programming of internal registers related to thresholds, operating modes, and trigger states. This synchronous serial protocol, widely adopted in space applications for its simplicity and robustness, allows communication with external control logic, whether a laboratory test system or an in-flight FPGA. The ASIC performance has also been validated under extreme environmental conditions. In particular, the VEGA2 architecture ensures nominal operation over a wide temperature range from −60 °C to 80 °C, with minimal variation in signal amplitude compared to the reference condition at 0 °C. These features complement the requirements and are essential for ensuring reliability in space environments characterized by large thermal excursions. Although the output analog signal is converted into pseudo-differential form, this configuration has shown significant limitations in terms of common-mode rejection and compatibility with fully differential downstream architectures. These considerations motivated the development of a new fully differential two-stage buffer block, discussed later in this thesis, with the aim of improving linearity, output swing, and disturbance immunity.

1.5.2 The LEMX-DC System

The LEMX-DC system functions as the digital interface between the analog signals generated by the SDD detectors acquired through the VEGA2 front-end and the payload onboard electronics. Its primary function is the conversion of the multiplexed analog signal into a compact digital stream, synchronized with the trigger system. The event-driven operation and modular architecture enable high energy efficiency, making the system suitable for satellite-based scenarios with strict constraints in terms of power, area, and reliability. A distinctive trait of LEMX-DC is its direct management of the serialized analog input received from the readout ASIC, also referred to as the front-end chip. The LEMX-DC converts the charge signals generated by an SDD detector into a compact digital stream through its interface with the analog front-end. The architecture is organized as a linear array of at least six identical complete channels, expandable up to a maximum of twelve. Each channel independently processes the serialized analog stream from one of the readout ASICs, converting it into digital words. The initial version of the system, called RA1, represents the first implementation of the LEMX-DC project. It was developed to explore and field-test preliminary architectural solutions, particularly the use of multi-channel incremental ADCs and the logic management of timing. However, during the characterization and validation phases, it was observed that some performance metrics did not fully align with the expected specifications, particularly in terms of energy efficiency and scalability. These considerations led to the development of the next version, RA2, which incorporates improvements at both analog and digital levels. Table 1.1 summarizes the main differences between the two versions. The information reported is based on the internal technical documentation of the RA1

Property	**RA1**	**RA2**
Clock frequency	12.5 MHz	15 MHz
OSR	64	96
Number of paths (with S/H)	2	3
Core On-Duty Power Dissipation	2 × 9 mW = 18 mW	3 × 9 mW = 27 mW
Nominal average power (per channel)	1.4 mW @ 500 events/s	1.5 mW @ 720 events/s
ENOB	11 bits @ full scale	11 bits @ ADR

Table 1.1: Comparison between RA1 and RA2 versions of the LEMX-DC system.

and RA2 versions of the LEMX-DC system, respectively described in [6] and [7].

Chapter 2

LEMX-DC Architecture

2.0.1 Internal Architecture of the LEMX-DC Channel

Each complete channel of the LEMX-DC system is designed to acquire and digitize a stream of 32 multiplexed analog signals originating from the front-end VEGA2 channels (also known as NOVA) [8]. To achieve this, each channel consists of three identical *Analog-to-Digital Converters* (ADCs) operating in parallel. These ADCs share the task of converting the serialized input stream and distribute the workload in a balanced manner. Figure 2.1 reports the block diagram of one full channel. The incoming analog signal is a sequence of 32 DC values transmitted in serial form. A centralized control logic handles the deserialization of the stream, distributes it to the three ADCs, and reassembles the converted digital data into a compact serial output. Each ADC, referred to as a module core, includes a *Sample and Hold* (S/H) circuit, which holds the signal value constant during the conversion, and a 13-bit analog-to-digital converter. Within the usable amplitude range, at least 11 bits are effectively significant, with an average *Effective Number Of Bits* (ENOB) of approximately 11 bits [7]. The conversion process is distributed in a round-robin fashion: the first analog value is assigned to the first ADC, the second to the second ADC, the third to the third, and the fourth again to the first ADC, continuing until all 32 values are processed. Once each sample has been converted, the global logic serializes the digital results into a single output stream compatible with the system onboard electronics [8]. The main specifications of the LEMX-DC ASIC, defined to meet the system-level requirements for timing, resolution, and integration, are summarized in Table 2.1.

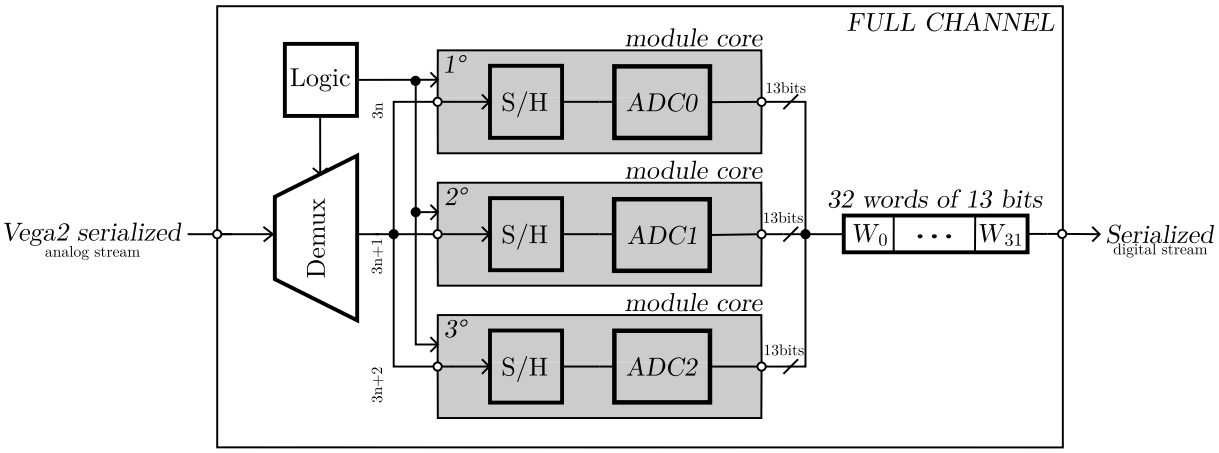

Figure 2.1: Block diagram of one full channel of the LEMX-DC.

Parameter	Value
Number of Channels	6÷12 (x32)
Input Signal	Differential (compliant with Single Ended)
Conversion Time	80 µs (for full 32-pixel scan)
Integral Non-Linearity (INL)	LSB/2 (for 11 bits)
Supply Voltage	3.3 V
Power Consumption	1.5 mW per full channel
Technology	CMOS 0.35 µm (ams c35b4)

Table 2.1: Main specifications of the LEMX-DC ASIC.

To better understand the rationale behind the adopted channel structure, it is useful to examine the timing constraints, signal buffering, and parallelization strategy implemented in the system. The architecture of the LEMX-DC system was designed to complete the acquisition and conversion of the entire multiplexed set within 80 µs (for each full scan sequence). The organization, shown in Fig. 2.1, allows the 32 signals to be distributed among three parallel incremental ADCs resulting in 11 conversions performed by each of the firsts two converters and 10 conversions carried out by the third[7]. The input signal of each channel, as specified, has a maximum duration of 20 µs. This value is not arbitrary; it represents the maximum "dead time" allowed for the SDD detector, i.e. the maximum time interval during which the detector can remain idle without recording new events. The channel reading follows a fixed sequential order (from channel 1 to 32), simplifying temporal control and ensuring proper synchronization of the conversion windows between the logic and the front-end. To ensure the integrity of the analog signal before digitization, a buffer stage must be introduced between the sample and hold circuit and the converter. This precaution is essential for electrically isolating the analog bus from potential parasitic or reflection effects caused by resistive, capacitive, or inductive mismatches along the PCB interconnections. The acquisition path is therefore structured as follows:

$$\text{Analog MUX} \rightarrow \text{Sample and Hold (S/H)} \rightarrow \text{Buffer} \rightarrow \text{ADC}$$

The signal coming from the front-end has a shape resembling a Gaussian bell curve, with an amplitude ranging from approximately 0.7 V to 2.2 V. Furthermore, the system logic is event-driven: the sampling and conversion process is triggered only when a valid input event is detected. As a result, the system can enter a sleep mode during inactivity periods, significantly reducing power consumption and enhancing efficiency in space applications, where the event load is highly variable [7, 8].

2.0.2 Sample and Hold (S/H) Module

The input stage of the ASIC consists of a two-step sample and hold circuit, which intrinsically includes demultiplexing functionality. Its role is to acquire the signals coming from the analog input bus and maintain them stable over time, thus providing a reliable and well-defined value to the subsequent A/D converter. As shown in Fig. 2.2, the circuit is conceptually divided into three parts:

- The first phase is a switch-capacitor structure used to acquire the input signal in a quasi-steady state, meaning the voltage across the sampling capacitor C_{S1} is allowed to settle close enough to its final value within a defined error margin [7]. The `ENMUX` signal, generated by the control logic, enables or disables the charge transfer to C_{S1}. In this phase, the S/H block also serves as an intrinsic demultiplexer, as the three S/H circuits of the respective core modules are alternately selected by the logic through `ENMUX`.

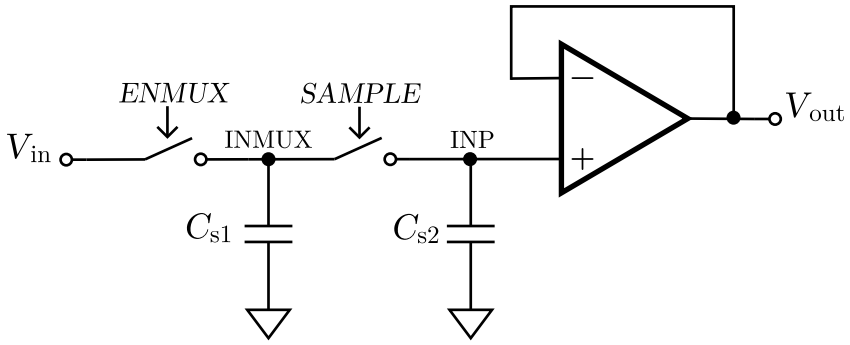

Figure 2.2: Schematic of the two-steps sample and hold circuit.

- Once the S/H circuit is selected (with `ENMUX` active), and after a programmable delay that ensures the signal has sufficiently settled on C_{S1}, the second phase begins: a second switch-cap stage stores the charge on capacitor C_{S2}.
- The third phase consists of a buffer amplifier that ensures proper signal transfer to the ADC, maintaining its stability throughout the conversion process.

This two-stage structure is necessary to effectively decouple the input signal from the subsequent load. The analog bus from which the signal originates is connected to a different ASIC through a PCB. This connection, along with bonding, introduces non-negligible parasitic effects that can degrade the signal. Any bouncing resulting from these parasitics is not seen by the buffer and, consequently, not by the ADC either, significantly improving sampling quality. For both charge transfer phases (first and second), a programmable delay can be configured to guarantee proper settling behavior: the first phase allows quasi-settling on capacitor C_{S1}, while the second phase ensures full settling on C_{S2} [7]. During the second phase, part of the charge previously stored on C_{S1} is shared: capacitors C_{S1} and C_{S2} are therefore connected in parallel, and both need to be recharged for the node to reach a new stable state. Finally, in the third phase, the activation of the `SAMPLE` control signal allows the value stored on capacitor C_{S2} to remain constant for the entire duration of the A/D conversion.

2.0.3 Interconnection Parasitics and Mitigation Strategies

A particularly critical aspect in the design of the LEMX-DC system concerns the interface between the analog and digital domains, specifically between the front-end output and the ADC input. Due to the system structure, in which the signal passes through a PCB and bonding connections between separate ASICs, non-negligible parasitic capacitances are introduced. These effects typically in the range of 5 pF to 10 pF can compromise the proper settling of the signal at the ADC input, especially during the sampling phase [7]. Several mitigation strategies were considered to ensure correct signal acquisition in the presence of unknown or variable parasitic capacitance:

- **Solution 1 — Clock Slowing:** One possible approach is to reduce the clock frequency, thereby giving the signal more time to settle before conversion. However, this solution was discarded because it risks violating the system time constraints (80 µs for 32 channels) and introduces a generalized slowdown even in circuit parts that do not require it.
- **Solution 2 — Programmable Delays:** The preferred approach involves introducing configurable programmability of the delay times for the settling and sampling phases, allowing the system to dynamically adapt to the actual capacitive load. A key advantage of this strategy is that the additional waiting time is not wasted: instead of passively waiting for the signal to settle, the system can exploit this interval to increase the *Oversampling*

Ratio (OSR), thereby enhancing resolution. Four possible implementation strategies were analyzed:

- **(a) 10-bit configuration:** two 5-bit registers allow fine-tuning of the *settling* and *sampling* times, with a resolution of one clock tick per *Least Significant Bit* (LSB). This solution is flexible but introduces significant logical complexity and risks interference between configuration pointers.
- **(b) Selection among 4 scenarios:** two bits select one of four predefined timing profiles. This approach offers a balanced trade-off between area and implementability, but it entails a notable increase in logic, as if the same structure were replicated four times.
- **(c) External FPGA management:** the FPGA controlling the two ASICs provides an authorization signal to start the sampling phase only when the analog signal is deemed stable. In this case, the local logic synchronizes with the FPGA through a simplified protocol: the system asserts the MUX selection signal, and the FPGA responds when it is ready to perform the sampling.
- **(d) Three programmable serial registers:** the final solution makes use of three dedicated configuration registers named `INIT_MARGIN`, `SETTLING_MARGIN`, and `SAMPLING_MARGIN`, which allow the introduction of a configurable delay, divided between total settling time and dedicated sampling time. This choice represents a good compromise between flexibility, robustness, and logical complexity, and it proved to be compatible with the architectural specifications of the project [7]. This is the solution that was ultimately implemented in the final design.

2.0.4 Introduction to the ADC Architecture

In addition to the S/H circuit, the second fundamental component of the LEMX-DC architecture is the *Analog-to-Digital Converter* (ADC). To meet the application's requirements in terms of accuracy, energy efficiency, and compatibility with event-driven acquisition, a second-order *Incremental Sigma-Delta* (IADC) topology was adopted. This architecture is particularly well-suited for high-precision conversion in systems where signal acquisition is sparse or triggered, as it provides excellent static linearity, low offset, and low power consumption. Unlike conventional oversampled modulators, incremental ADCs support sample-by-sample conversion with finite response time and improved immunity to low-frequency noise sources. The chosen implementation features a discrete time architecture with two switched-capacitor integrators and a single bit comparator. The modulator is activated only upon a valid trigger event, operating over a closed acquisition window that enables oversampling and digital noise shaping. This structure enables high resolution and low noise without requiring external components, making it highly compatible with the integration and area constraints of the system. A detailed description of the IADC architecture, including the circuit-level implementation and attenuation strategies adopted to ensure robust performance, is presented later in Section 2.1.

2.1 Incremental ADC Design and Global Control Logic Implementation

In high-precision measurement systems, the accuracy of analog-to-digital conversion plays a crucial role. In these contexts, systematic errors such as offset, high gain error, or significant deviations in linearity are not tolerated. Traditional $\Sigma\Delta$ (Sigma-Delta) modulators, while excelling in resolution, are not optimized for high-precision sample-by-sample conversion. They

tend to introduce structural delays and dependence on the dynamic behavior of the input signal. *Incremental* ΣΔ *ADCs* (IADCs), on the other hand, are specifically designed to provide high accuracy in on-demand conversion of individual samples, ensuring excellent static linearity and low values of *Differential NonLinearity* (DNL), *Integral NonLinearity* (INL), offset, and power consumption [9]. Their architecture is particularly suitable for systems in which acquisition occurs at low frequency or on an event-driven basis, as in scientific, biomedical, or environmental sensing applications [10]. Unlike dual-slope or Nyquist ADCs, IADCs can offer superior performance without requiring external components such as discrete capacitors, making them especially advantageous in integrated circuits. Furthermore, they exhibit higher tolerance to analog component mismatch. In battery-powered applications, the energy efficiency of the ADC becomes a fundamental metric. IADCs are well-suited to adapt to system-imposed power constraints while maintaining strong immunity to error sources such as flicker noise and offset, which are critical in low-amplitude sensor signals. These systems often include a multiplexer for managing multiple channels, making area-efficient and energy-scalable design crucial. An additional architectural advantage lies in the system response structure. The modulator of an IADC exhibits a *Finite Impulse Response* (FIR), allowing the subsequent decimation filter to be implemented as a simple *Cascaded Integrator Comb* (CIC) filter. This design simplicity contrasts with conventional ΔΣ systems, which require more complex and less stable *Infinite Impulse Response* (IIR) decimation filters [11]. For these reasons, the incremental ADC currently represents one of the most competitive solutions for high-precision conversion in environments constrained by power, area, and accuracy.

2.1.1 IADC Architecture and Operating Principle

This section provides a brief description of the operation of a first-order IADC, schematically illustrated in Figure 2.3, while the waveform associated with the conversion process is shown in Figure 2.4. The basic principle of the IADC is that the integration of the input voltage V_{in} and the reference voltage V_{ref} occurs alternately within the same conversion window. This approach differs from that adopted in conventional ΔΣ converters, in which the two integrations are handled separately [10]. Each conversion starts with the reset of both the integrator and the counter, and consists of $n = 2^B$ integration steps, where B is the desired number of output bits. When the output of the integrator exceeds the zero threshold, the decision bit d_i takes the value 1, and the system applies a $-V_{\text{ref}}$ contribution to the input of the integrator. After n cycles, the output of the integrator will be:

$$V = nV_{\text{in}} - NV_{\text{ref}} \tag{2.1}$$

where N represents the number of cycles in which the feedback was active ($d_i = 1$). In order for the conversion to be valid, the output must remain within the range between $-V_{\text{ref}}$ and V_{in}, hence:

$$N = n \cdot \left(\frac{V_{\text{in}}}{V_{\text{ref}}}\right) + \varepsilon \quad \text{with} \quad \varepsilon \in [-1, 1]. \tag{2.2}$$

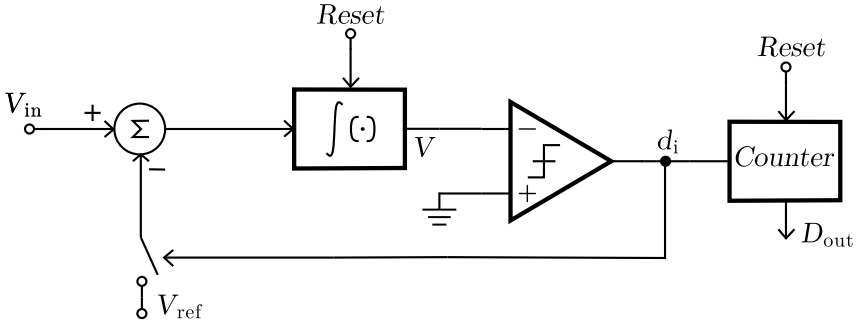

Figure 2.3: Block diagram of a first-order IADC.

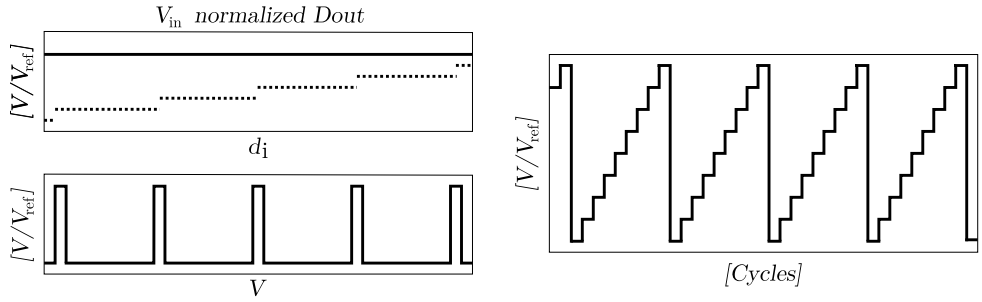

Figure 2.4: First-order IADC waveforms.

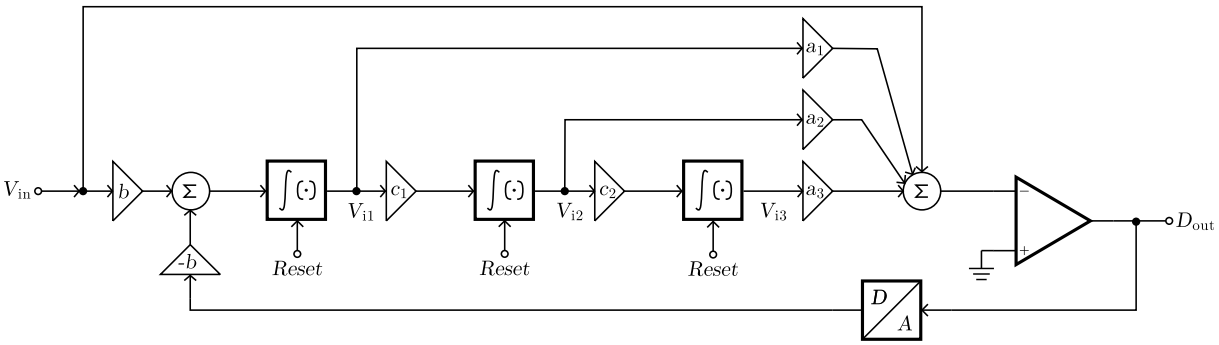

Figure 2.5: Block diagram of a third-order CIFF IADC.

The residual error at the output of the integrator is expressed as:

$$V = -2e_q V_{ref} \qquad \text{with} \qquad e_q \in \left[-\frac{1}{2}, \frac{1}{2}\right]. \tag{2.3}$$

This architecture offers good accuracy but suffers from limited conversion speed: to achieve B bits of resolution, 2^B clock cycles are required for each conversion. This makes first-order IADCs less suitable for high-frequency applications, while still being ideal for low-speed, event-driven, or battery-powered systems [10].

2.1.2 Higher-Order Modulator Architecture

To overcome limitations in terms of speed and noise, the order of the modulator can be increased. One of the most widely used architectures is the *Cascaded-Integrator Feed-Forward* (CIFF) structure, illustrated in Figure 2.5, which allows greater suppression of quantization noise for a given number of cycles n. It is assumed that a *Sample and Hold* (S/H) stage is used at the input to ensure signal stability throughout the entire conversion. At each clock cycle, the input V_{in} is converted and quantized, and the output bit is reused as negative feedback. The output of the three integrators, assuming a constant input and decision bits $d_i \in [-1, +1]$, is described by:

These expressions are derived from the theoretical modeling reported in [10]. For the system to remain stable, the output of the last integrator must stay within the bounds of $\pm V_{ref}$. This can be ensured by appropriately designing the loop and limiting the maximum gain of the *Noise Transfer Function* (NTF).

2.1.3 Quantization Error and Digital Output Resolution

Under the assumption of stability, after n clock cycles, it is possible to estimate as follows the average value of the input normalized with respect to the reference [10]:

$$\frac{\hat{V}_{in}}{V_{ref}} = \frac{3!}{(n-2)(n-1)n} \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k. \tag{2.4}$$

1st integrator:

$$V_{i_1}[0] = 0$$
$$V_{i_1}[1] = b \cdot (V_{\text{in}}[0] - d_0 V_{\text{ref}})$$
$$V_{i_1}[2] = V_{i_1}[1] + b \cdot (V_{\text{in}}[1] - d_1 V_{\text{ref}})$$
$$\vdots$$
$$V_{i_1}[n] = b \cdot \sum_{k=0}^{n-1} (V_{\text{in}}[k] - d_k V_{\text{ref}})$$

2nd integrator:

$$V_{i_2}[0] = 0$$
$$V_{i_2}[1] = c_1 V_{i_1}[0] + V_{i_2}[0] = 0$$
$$V_{i_2}[2] = c_1 V_{i_1}[1] + V_{i_2}[1]$$
$$\vdots$$
$$V_{i_2}[n] = c_1 b \sum_{l=0}^{n-1} \sum_{k=0}^{l-1} (V_{\text{in}}[k] - d_k V_{\text{ref}})$$

3rd integrator:

$$V_{i_3}[0] = 0$$
$$V_{i_3}[1] = c_2 V_{i_2}[0] + V_{i_3}[0] = 0$$
$$V_{i_3}[2] = c_2 V_{i_2}[1] + V_{i_3}[1] = 0$$
$$\vdots$$
$$V_{i_3}[n] = c_1 c_2 b \sum_{m=0}^{n-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} (V_{\text{in}}[k] - d_k V_{\text{ref}})$$

Figure 2.6: Recursive evolution of the three integrator stages in a CIFF IADC.

From the bounds on the estimation error of V_{in}, and considering that in an ideal ADC the maximum quantization error is $\pm\frac{V_{\text{LSB}}}{2}$, the value of the LSB can be derived. Starting from the relation

$$e_q = \frac{\hat{V}_{\text{in}} - V_{\text{in}}}{V_{\text{LSB}}} \quad \Rightarrow \quad V_{i_3}[n] = -2V_{\text{ref}}\, e_q$$

this yields to [9]:

$$V_{\text{LSB}} = \frac{2 \cdot 3!}{(n-2)(n-1)\,n} \cdot \frac{1}{c_1 c_2 b} \cdot V_{\text{ref}}. \tag{2.5}$$

This expression links the minimum distinguishable output value (LSB) to the number of cycles n, the scaling coefficients c_1, c_3, and b, and the reference voltage. Defining

$$G = \frac{2 \cdot 3!}{(n-2)(n-1)\,n} \approx \frac{6}{n^3} \tag{2.6}$$

eq. 2.5 can be rewritten as:

$$V_{\text{LSB}} = \frac{G}{c_1 c_2 b} \cdot V_{\text{ref}}. \tag{2.7}$$

Starting from the LSB, it is possible to compute the effective resolution of the converter, expressed in ENOB [11]:

$$\text{ENOB} = \log_2\left(\frac{2V_{\text{ref}}}{V_{\text{LSB}}}\right) \simeq 3\log_2(n) + \log_2(c_1 c_2 b) - 2.6\,. \tag{2.8}$$

This approximation highlights how the ENOB increases linearly with $\log_2(n)$, with an additional dependence on the scaling factors and a constant term related to the FIR nature of the architecture.

2.1.4 Digital Output Reconstruction and Design Principles

Conceptually, the simplest filter to produce the digital output of the converter is a *Cascade-Of-Integrators* (COI) structure designed specifically to implement the transfer function $\hat{V}_{\text{in}}/V_{\text{ref}}$. This

implementation generates a filter of the same order as the modulator. However, due to the on-demand nature of the incremental modulator, the circuit operates over closed time windows: it is activated only during a conversion and then it is reset. In the case of a first-order modulator, the filter can be implemented very simply through an up/down counter that accumulates the outputs of the quantizer, considering the bits $d_i \in [-1, +1]$. For higher-order modulators, this solution can only be applied to the first stage of the filter: the subsequent stages must be implemented as true digital integrators, repeatedly accumulating the output sequence of the modulator. In first-order modulators, the filter output represents an approximation of the average value of the input signal V_{in} over the entire conversion window. This implies that, in the presence of periodic noise with period T_p, if the conversion duration nT (where T is the clock period and n is the number of cycles) is an integer multiple of T_p, the noise is averaged and substantially eliminated in the conversion process. The situation differs for higher-order modulators. In this case, the output is not a simple average, but a weighted sum obtained through digital filtering of the sequence produced by the loop. This *accumulate-and-dump* process, typical of the FIR filters that follow the modulator, implies that the final input estimate is a linear combination of the digital samples produced during the conversion window. In particular, the filter assigns greater weight to the first samples of the sequence. For this reason, it is essential that the average value of the first bits d_i closely reflects the actual input signal value. To achieve this and minimize the effect of $\Delta\Sigma$ loop transients, it is possible to feed the quantizer directly with the input signal, avoiding a pre-integration phase. In this way, the first generated bits are already representative of the actual value of V_{in} [9, 10]. In addition to output reconstruction, several fundamental design concepts must be considered when optimizing incremental ADCs, especially in the context of multi-channel and low-power systems. A key element of IADCs is the presence of a *reset* signal, which transforms the architecture from a continuous-time system into a discrete-time one. This feature is particularly advantageous in multiplexed systems, where multiple channels share the same hardware. Time-domain analysis also makes it possible to derive general design guidelines, including:

- **Dynamic range scaling**: Necessary to prevent overloading of the integrators and the quantizer. This is important because higher-order structures tend to become unstable as the input signal approaches V_{ref}. Moreover, it allows determining the optimal coefficients a_i and b_i for each stage of the modulator. In the case of a 1^{st}-order IADC, $V_{\text{in}} = 0.9\,V_{\text{ref}}$ is used, whereas for a 3^{rd}-order modulator, $V_{\text{in}} = 0.75\,V_{\text{ref}}$ is typically adopted.

- **Estimation of n and digital resources**: By using the formulas for the reduction factor G and for the LSB, it is possible to estimate the number of cycles required to achieve a given resolution. A good design practice is to ensure that the *Signal-to-Quantization-Error Ratio* (SQNR) is significantly higher than the overall SNR of the system, since most of the noise budget will inevitably be associated with thermal noise [11].

In this context, it is also useful to highlight the main architectural advantages and disadvantages offered by IADCs.

2.1.5 Advantages of Incremental ADCs

- The decimation filter is simpler to implement compared to that required in conventional $\Delta\Sigma$ converters.

- The duration of the conversion window is known (T_W), simplifying the timing management of sampling.

- The architecture is well-suited for use in multiplexed systems.

- Possibility of conditional activation and sleep mode to reduce power consumption.

2.1.6 Limitations and Design Trade-Offs

- As in conventional $\Delta\Sigma$ converters, the SNR is determined by kT/C noise.
- In higher-order incremental modulators, the input-referred noise is not uniformly distributed across the samples [9]. Each conversion presents a weighting factor associated with each input sample, and the total input-referred noise power is:

$$\overline{v_n^2} = \sum_{i=1}^{M} \omega_i^2 \, \overline{v_s^2} = \overline{v_s^2} \sum_{i=1}^{M} \omega_i^2 \tag{2.9}$$

  where v_s represents the input noise power associated with each sample, and ω_i is the weight of the decimation filter associated with each sample.
- As the modulator order increases, the aggregated thermal noise also increases. To maintain a constant SNR, the capacitance C must be increased, which in turn leads to a higher current draw and thus increased power consumption [11].

These aspects highlight the fundamental trade-off in IADC design: achieving higher resolution and better noise rejection requires increased complexity and higher power consumption. The goal thus becomes finding an optimal balance between precision, area, and power.

2.1.7 Final IADC Architecture and Input Attenuation Design

The final architecture of the analog-to-digital converter (IADC) used in the LEM-X project is the result of an iterative design and optimization process, based on the requirements of accuracy, energy efficiency, and compatibility with multiplexed systems. The chosen topology is that of a second-order incremental modulator with a discrete-time architecture, featuring two switched-capacitor integrators and a single-bit comparator. This structure is based on the scheme proposed by Bernhard E. Boser and described in detail in [12]. The final specifications and measured results, updated in the most recent project revision, have been collected in the technical reference document [8].
Figure 2.7 shows the block diagram of the implemented architecture. The A/D converter consists of a main analog core implemented with two switched-capacitor integrators, a synchronous one-bit comparator with sampled-data feedback, a digital state machine, a decimation filter, and auxiliary blocks for testing (voltage reference buffer, current reference generation, and clock distribution). The entire circuit was designed in 0.35 µm CMOS technology with a 3.3 V supply voltage, occupying an area of approximately $1\,\text{mm}^2 \times 1.2\,\text{mm}^2$. The modulator is activated only upon a trigger event, initialized (reset), and operated over a closed time window typically composed of 256 clock cycles. At the end of each window, the digital code is reconstructed by computing the *sum of sums* over the bit-stream produced by the comparator, in accordance with the behavior of a second-order modulator. The feedback coefficients are set to 0.5 for both stages, ensuring system stability and linearity even under high signal conditions. The comparator acts as an ideal quantizer (zero quantizer), making binary decisions on each integrated sample. As reported in [12], with an *Over Sampling Ratio* (OSR) of 96, the architecture allows for an effective resolution of 11 bits, with a dynamic range of 79 dB. The out-of-band quantization noise is effectively attenuated by the digital decimation filter, which also reduces the bandwidth, resulting in a data rate compatible with the system electronics. To ensure proper operation across the full dynamic range, and in particular to prevent saturation of the comparator when

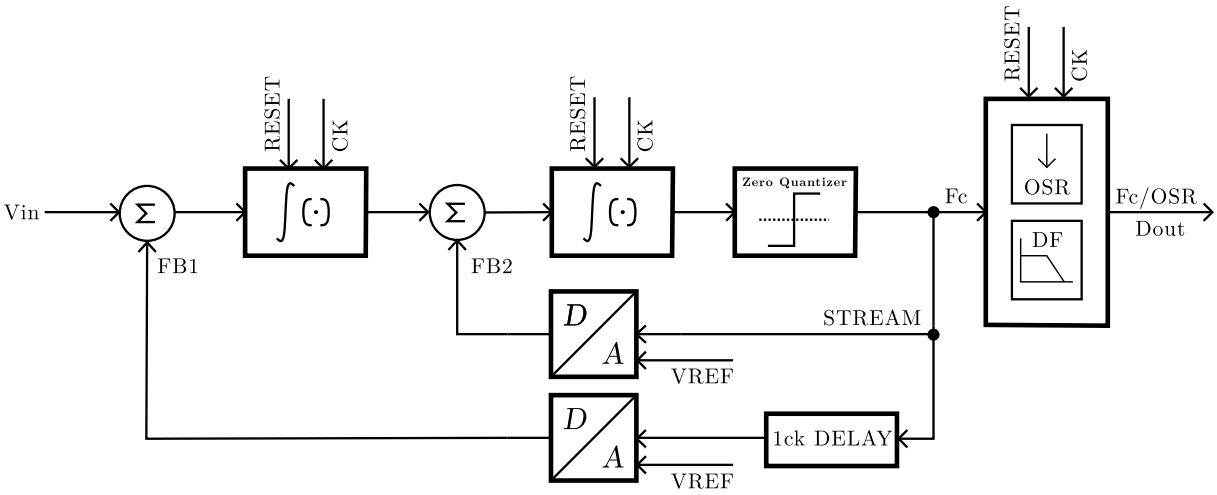

Figure 2.7: Block diagram of the incremental architecture in the LEM-X project.

V_{in} tends to V_{ref}, an attenuation stage was introduced at the IADC input. Several circuit-level solutions were evaluated to implement this feature, considering different levels of attenuation and signal configurations. The following subsections present the main design alternatives that were studied, leading to the final choice adopted in the system. The goal was to implement a path that would apply an amplitude reduction of $2/3$ *exclusively* to the signal coming from the analog front-end (VEGA2), while leaving the feedback signal returned by the DAC unaltered. This precaution is necessary to prevent the comparator from saturating under conditions where $V_{\text{in}} \rightarrow V_{\text{ref}}$, which would otherwise cause a drastic degradation in quantization noise. The option of designing a circuit that converts the single-ended signal into a differential one was also considered, in order to exploit the typical advantages of fully-differential architectures, such as improved common-mode rejection, reduced even-order harmonic distortion, and greater immunity to external disturbances.

2.1.8 Final Programmable Attenuation Network

The final solution designed represents the configuration adopted in the project. This structure allows operation with both *single-ended* and *differential* signals, always maintaining the desired attenuation factor to ensure the linearity of the IADC. In the previous solutions, the attenuation was fixed at $2/3$ on each branch. However, when working with differential signals, this would results in an overall attenuation of $4/3$ on both branches, which leads to degradation of the effective gain and the linear behavior of the integrator. To address this issue, a programmable structure was designed, capable of dynamically adapting the attenuation factor based on the operating mode. The circuit, shown in Figure 2.8, implements a switched-capacitor attenuator with two selectable paths, controlled by a configuration bit: When operating in single-ended mode, branch 1A is enabled. In this configuration, the input signal is attenuated by a factor of $2/3$ on a single branch, thus achieving the expected behavior. In contrast, when operating in differential mode, branch 1B is activated instead. In this case, each branch receives an attenuation of $1/3$, resulting in an overall attenuation of the differential signal equal to $2/3$, as desired. Thanks to this reconfigurable structure, the circuit ensures correct and linear behavior in both operating modes, allowing the full dynamic range of the system to be exploited without introducing systematic errors related to attenuation.

2.1.9 Global Logic Manager

In this section, a detailed description of the first version of the global logic (called Logic Manager), that controls and supervises all the operations performed by the channel, is provided. The

purposes of this digital block are to synchronize and manage the data acquisition from the analog input bus coming from the FE-ASIC and provide an output bit stream. The time slot available for reading the data coming from the 32 channels of the FE-ASIC is 80 µs. The primary objective is to ensure that the entire scan and conversion process is completed within this allocated time, while maintaining precise control over timing, memory storage, and output serialization. The system ensures efficient data acquisition through trigger management, conversion synchronization, and structured data output. The analysis focuses on the initial version of the logic, as it introduces interesting approaches to data management. The final implemented version can be regarded as a simplified subset of the original architecture, following area optimization choices driven by budget constraints that led to the removal of certain functionalities.

2.1.10 Internal Logic I/O Functionality

The data acquisition and conversion process is activated upon trigger signal detection. This signal is generated as an "OR" of all 32 triggers of the VEGA2 channels, ensuring that acquisition begins even if only one channel detects an event. If no event is detected, the system remains in a waiting state, reducing power consumption until a trigger occurs. As shown in Figure 2.1, the three ADCs operate in parallel, efficiently alternating between data storage and conversion. Once a signal is stored in the sampling circuit, the next signal can be stored in the second ADC, while the first ADC simultaneously starts the conversion of the previously stored data. This process repeats in a continuous loop until all the serialized 32 analog input signals have been scanned. The data is distributed among the ADCs so that ADC0 and ADC1 handle 11 samples each, while ADC2 only 10, ensuring that all conversions are completed within the 80 µs time constraint. Acquired data is stored in a memory register to maintain data integrity and minimize corruption risks. Each ADC stores its conversion results in a dedicated register. At the end of all 32 conversions, the data is transferred to the primary memory (`MEMORY`) that works as a matrix, efficiently organizing the scanned data. The output word (`WORD_OUT`) is structured to ensure an organized and synchronized data transmission. Table 2.2 below illustrates the bit allocation within the output word: In addition to internal control and data management, the logic block interfaces with the surrounding digital and analog subsystems through a set of dedicated input and output signals. The main inputs of the Logic Manager, shown in Figure 2.9, are as follows:

- **TRIGGER (asynchronous)**: A global "OR" of all 32 channel triggers, responsible for

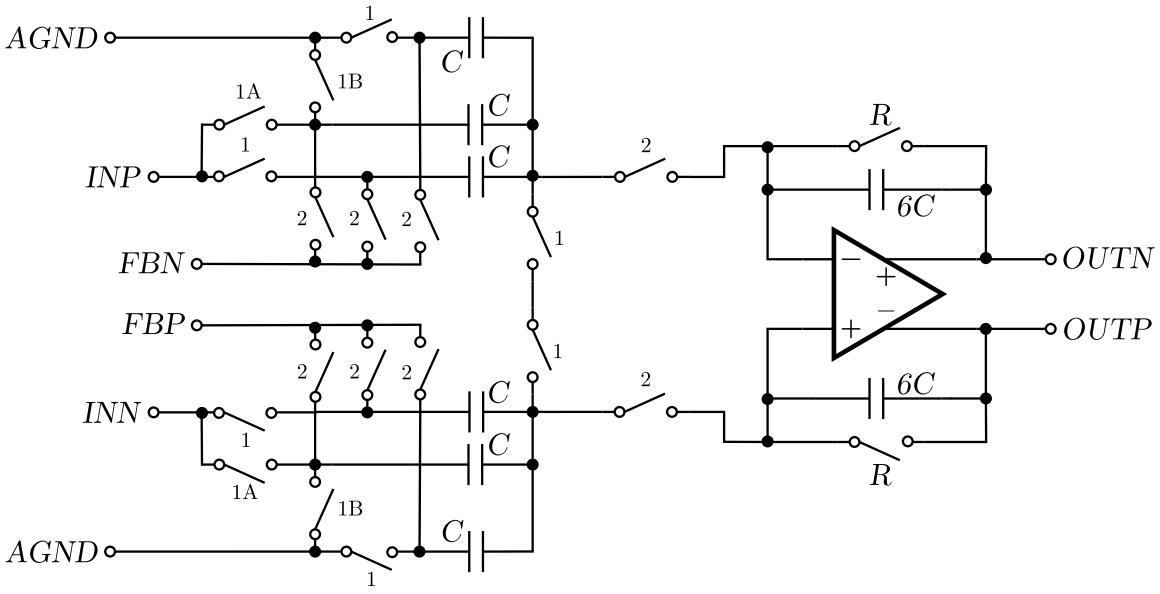

Figure 2.8: Programmable switched-capacitor attenuator for single-ended and differential signals.

Data Field	Bit Range	Description
Converted data	[415:0]	Stores the converted ADC values
Spacing bits for separation	[416]	Bit used for separation
Event information	[420:417]	Encodes event-related data
Spacing bits for separation	[421]	Additional bit for separation
TRG_WORD_MEM	[422:453]	Stores the trigger word

Table 2.2: Bit allocation within the WORD_OUT data structure.

initiating the acquisition cycle when at least one channel detects an event.

- **ADC0, ADC1, and ADC2**: 13-bit output signals from the three ADCs, representing the converted data from the sampled channels.
- **EOC0, EOC1, and EOC2**: Signals that indicate the completion of a conversion cycle for each ADC.
- **RESET (asynchronous)**: A system-wide reset signal. When high, it restores all registers and configuration settings to default values.
- **CK**: The main system clock, operating at 15 MHz (or 10 MHz in simulations for better clarity and signal analysis).
- **RESET_ACQ (asynchronous)**: Resets the ADCs after a full conversion cycle, ensuring they are ready for the next conversion.
- **RESET_CAL**: Resets the calibration parameters, restoring them to their default states.
- **DATA_CAL**: Used to transmit calibration data to the system.
- **EN_CAL**: Enables, when high, the calibration process, allowing the system to adjust settings based on external calibration inputs.
- **SER_RES (asynchronous)**: Resets the serial acquisition block.
- **SER_EN**: Enables, when high, the serial acquisition process, delivering the complete output word including the full conversion and ancillary data of the 32 analog channels.

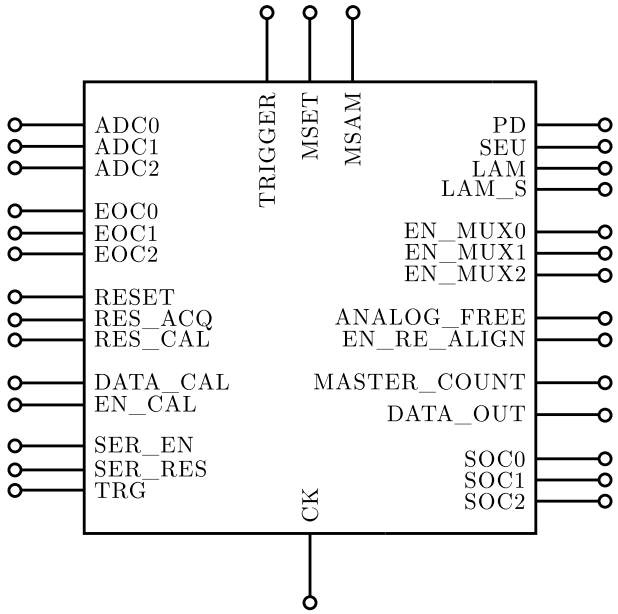

Figure 2.9: Logic manager symbol with pin list.

- **TRG**: Individual trigger signals for each channel, indicating which specific channel has detected an event.
- **SOC0, SOC1, and SOC2**: Signals used to indicate the start of the conversion process for each ADC.

The outputs of the logic block include:

- **DATA_OUT**: The data related to `WORD_OUT` is transmitted synchronously with the system clock, including opening and closing bits for synchronization.
- **PD**: Signal used to reduce power consumption when no conversion is in progress. It is activated during idle periods and deactivated upon detecting a new trigger, optimizing energy efficiency.
- **EN_MUX0, EN_MUX1, and EN_MUX2**: Signals used to enable the connection of each ADC to the sampling circuit.
- **LAM**: Indicates the end of a complete scan. It is set high at the end of the 32^{nd} conversion and remains active until the start of the next scanning cycle.
- **LAM_S**: Indicates the end of data transmission. It is set high together with the `LAM` signal but remains active until the entire data transmission process is completed.
- **SEU_C**: This signal, when high, indicates a data storage issue in configuration.
- **ANALOG_FREE**: A flag that indicates the end of analog data acquisition has been reached and the analog input bus can be freed to receive new events, even if the last conversion is still running. This is an optional mode for LEMX-DC usage.

2.1.11 Register and Data Management

The calibration process enables the system to fine-tune key timing parameters, ensuring optimal performance even in the presence of parasitic effects. Since parasitic capacitances cannot be precisely estimated without the physical chip, calibration provides a high degree of flexibility to adjust timing settings as needed. If the real parasitic effects deviate from initial estimations, the system can dynamically compensate for these variations, ensuring reliable and consistent operation. These values are stored in dedicated registers, guaranteeing a stable initialization and adaptability to different operating conditions. When either the `RESET` or `RESET_CAL` signal is high, the calibration parameters are restored to their default values as shown in Table 2.3:

Parameter	Bit Range	Default Value	Default Clock Periods
`MINIT`	[4:0]	2	18
`MSET`	[4:0]	2	24
`MSAM`	[3:0]	0	10
`LESS_CYCLES`	[3:0]	0	x

Table 2.3: Default calibration values and associated bit ranges.

If the `EN_CAL` signal is active, the system serially loads the calibration parameters into a 20-bit array called `STREAM_CAL`. The data is then assigned to the respective registers as summarized in Table 2.4:

Parameter	Bit Range (STREAM_CAL)	Description
MINIT	[4:0]	Initial settling time
MSET	[9:5]	Settling adjustment time
MSAM	[13:10]	Sampling delay
LESS_CYCLES	[17:14]	Number of channels to be read

Table 2.4: Bit allocation within the STREAM_CAL calibration word.

The process is triggered on the negative edge of EN_CAL, ensuring proper synchronization with the system clock. Calibration enables fine-tuning of several system timing parameters. Specifically, MINIT, MSET, and MSAM adjust internal delays and help improve signal stability. The parameter LESS_CYCLES allows modifying the number of channels to be read during acquisition, which is particularly useful when interfacing with different front-end configurations and SDD sizes. A key architectural constraint is that the readout must always conclude with ADC1, since memory writing operations occur within its processing stage. To ensure calibration data reliability, a backup copy of the calibration registers is maintained. If a mismatch is detected between the primary and backup registers, the system raises the SEU_C flag to "1", indicating potential corruption of the stored data. A summary of the main calibration-related control signals is reported in Table 2.5. Each channel of the FE-ASIC is equipped with a signal called TRG, which indicates whether an event has been detected by that specific channel. This signal is used to determine which conversion corresponds to an actual event and which are performed for continuity in the scanning process. To keep track of these events, each ADC could be equipped with a dedicated register. This register stores information on whether each conversion within a full scan cycle was triggered by an actual event. Each TRIGGER_WORD register has a size of 11 bits (actually 10 bits for the third ADC), but at the end of the conversion such words are re-ordered to match the channel numeration in a continuous 32-bit stream. During operation, if a conversion is genuinely triggered by an event, a "1" is recorded in the corresponding position of the TRIGGER_WORD register. For example, if ADC0 is performing its second conversion and the event is valid, the register TRIGGER_WORD0[1] will be set to "1". This mechanism allows, at the end of a complete scan, to distinguish between meaningful conversions and redundant ones. During the post-processing phase, only conversions associated with real events would be considered, while the others discarded as non-significant. The implementation of these registers is not yet final, as a process of review and simplification of the logic is underway to ensure compatibility with the project budget. For this reason, the use of these registers becomes optional. A further register is used to track the number of complete scan cycles performed by the system. The EVENT register is a 4-bit counter that tracks the number of consecutive complete scans performed by the system. It is initialized to "1111" and incremented by one bit for each completed scan cycle, implying that its value rolls over to "0000" after the first increment post-initialization. This register is used to keep track of the number of consecutive conversions completed, interpreted as full scans of the 32 channels. EVENT is reset to its default value only through the general RESET signal and not by RESET_ACQ, which exclusively handles the reset of the ADC-specific registers. If an event is not acquired correctly by the subsequent logic (FPGA) a missing count is evident.

Signal	Function
RESET, RESET_CAL	Restores default calibration values
EN_CAL	Enables serial loading of calibration data
STREAM_CAL	Stores calibration parameters (20-bit array)
SEU_C	Error detection flag for calibration data
LESS_CYCLES	Adjusts the number of read channels

Table 2.5: Summary of calibration-related control signals.

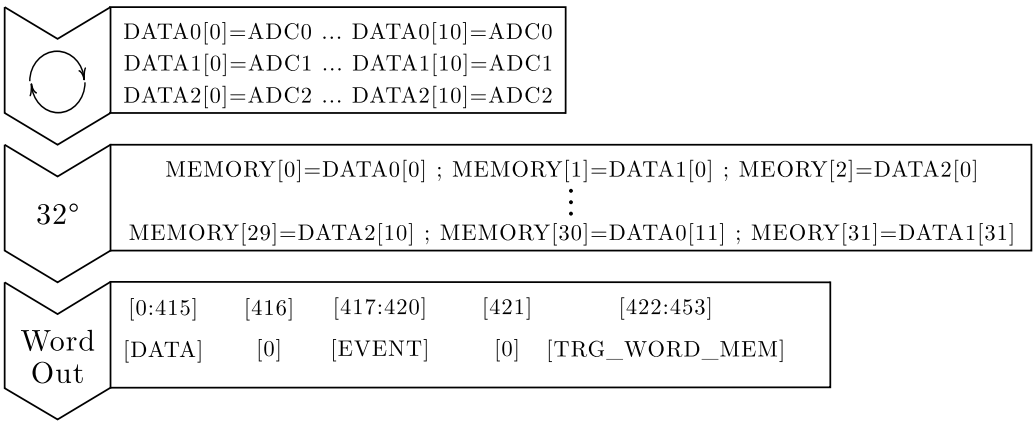

Figure 2.10: Data allocation structure across conversion registers, memory array and final output word format.

2.1.12 Operational Flow of the Logic

The operational flow described in this section is derived from a simulation conducted at a clock frequency of 15 MHz. All the timing values reported from this point onward are expressed in clock cycles. The first aspect to consider is clock synchronization and overall timing control, both of which are essential for coordinated acquisition across multiple channels. To ensure proper data handling, the system adopts a unified clock strategy: the same clock edge is used to process data within a given statement. When the clock originates from an external source, data integrity is ensured by verifying the data state on the opposite edge. This dual-edge approach enhances synchronization accuracy. System-level coordination of the conversion process is achieved using a counter-based approach. A global `MASTER_COUNT` counter orchestrates the timing of the 32 conversion scans, ensuring synchronous behavior across the system. Simultaneously, each ADC features a dedicated `LOCAL_COUNT` that governs the timing of its individual conversions. This local counter is reset after each conversion to prepare the ADC for the next sampling event. These timing values are configurable, allowing adaptation to compensate for real-world parasitic effects and system delays. After clock and counter synchronization, the system handles the timing of sampling events and memory storage. These operations are tightly coupled, as memory write operations depend directly on the synchronization of the sampling process. At the beginning of every conversion, the `ENABLE_MUX` output signal is asserted high for a duration of 34 clock cycles, enabling the corresponding ADC to perform the signal sampling. Two clock cycles after the assertion of the `SOC` signal, the `ENABLE_MUX` is deasserted, and it is then raised again 25 clock cycles before the subsequent `SOC`. The `SOC` itself remains active for 7 clock cycles, and each complete conversion takes 107 clock cycles. To avoid overlaps, an interleaved margin of 2 clock cycles is maintained between the `ENABLE_MUX` signals of adjacent ADCs, though this value can be adjusted to optimize the system timing performance. In the preliminary logic version, each ADC stores its conversion results in a dedicated register. The complete set of 32 conversions is then stored in a memory register named `MEMORY`, which is written at the end of the scan cycle, specifically after the eleventh conversion performed by `ADC1`. This memory structure is organized as a matrix of 12 elements, each 32 bits wide. As illustrated in Fig. 2.10, this structure ensures effective data management and reliability, thanks to the use of safety memory that prevents data loss. The scan cycle is re-initialized through the system reset logic. Upon the occurrence of either a `RESET` or a `RES_ACQ` signal, several reinitialization steps are performed to prepare the system for the next acquisition. These include:

- Setting `PD` to "1" and activating `EN_RE_ALIGN_INIT`, a state that persists until a new trigger is detected.
- Resetting the `MASTER_COUNT` to its default value; otherwise, it continues incrementing on

each rising edge of the clock.

- Resetting all LOCAL_COUNT registers, which are used by the ADCs to control the timing of individual conversions.
- Setting ANALOG_FREE to "0" at the beginning of the scan. This signal will be set to "1" only after the eleventh conversion by ADC1, indicating the completion of all 32 conversions.

If the signal RESET is active without RES_ACQ, the MEMORY, TRIGGER_MEM, and EVENT registers are cleared. In the specific simulation scenario considered, the trigger signal remains active throughout. Therefore, upon completion of the entire conversion cycle, a RES_ACQ signal is issued to return the system to its initial state and initiate a new scan. During conversion, the global logic receives an EOC (End Of Conversion) signal from the internal ADC logic. This signal indicates that a conversion has finished, prompting the system to immediately store the result in the respective local ADC register. The timing and synchronization of the three ADCs are managed using three main counters:

- **MASTER_COUNT**: Initialized to zero at the beginning of each scan cycle and incremented at each clock rising edge, it defines the global sequencing of operations.
- **LOCAL_COUNT**: Each ADC maintains a local counter, reinitialized with each new conversion, to align internal enable and sampling signals.
- **CYCLE**: Each ADC has a conversion counter to track how many conversions have been executed within a scan. This serves as an end-of-cycle condition:
  - For ADC0 and ADC1, once CYCLE reaches 11, no further conversions are permitted.
  - For ADC2, the limit is 10 conversions.

The multiplexer enable signals (EN_MUX) are controlled based on the following scheme:

- EN_MUX0 is activated at the start of every new scan.
- EN_MUX1 and EN_MUX2 are initially deasserted (set to 0) and are activated later through the progression of MASTER_COUNT, ensuring proper staggered sampling.

The final phase of the logic involves the transmission of conversion data. This process occurs on the negative edges of the clock signal, providing synchronized and stable data transfer. A dedicated counter, SER_POINT, manages the timing of the data transmission on the DATA_OUT line, which serves as the serial output. Transmission is governed by the SER_EN signal, which is externally controlled by the FPGA. If either RESET, SER_RES, or a low SER_EN is detected, the SER_POINT counter is reset to its initial value, and DATA_OUT is held low. Once SER_POINT is asserted, data transmission begins. A complete scan involves the transmission of 464 bits, which includes:

- A 454-bit output word [453:0].
- Opening bits (from LSB): 1010.
- Closing bits (from MSB): 001010.

The output word structure is illustrated in Fig. 2.11, providing a clear overview of the serialized data format used in the system.

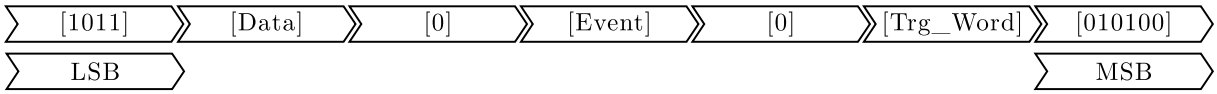

Figure 2.11: Structure of the output word.

Chapter 3

Hardware Design and PCB Implementation

3.1 Introduction to the Test Platform

The characterization of the LEMX-DC requires a dedicated mixed-signal printed circuit board capable of providing stable biasing conditions, low-noise power distribution, controlled analog interfacing, and reliable digital connectivity. Unlike a generic evaluation board, this platform was conceived as a measurement-oriented test bench, where the main objective is not only to power the device correctly, but also to make the internal operating conditions observable, repeatable, and easy to verify during laboratory activity.

For this reason, the PCB was organized around a modular architecture in which power generation, reference distribution, signal conditioning, device interfacing, and output observability are treated as separate but coordinated design problems. This approach simplifies debugging, supports incremental validation of each subsystem, and reduces the risk that a failure in one block propagates to the rest of the platform during the first experimental campaigns.

This chapter describes the hardware architecture adopted for the test platform, the rationale behind the selection of the most relevant components, and the main implementation choices used to preserve signal integrity. Particular attention is devoted to the power-supply structure, the reference and bias generation network, the routing of observable digital signals, and the analog input path used for functional characterization of the ASIC.

3.2 System Segmentation of the Test Bench

The test platform is organized into four functional blocks so that power generation, bias distribution, signal conditioning, and signal observability can be validated independently during turn on and characterization:

- **Block 1 – Main ASIC supply rail:** generation and monitoring of the adjustable 3.3 V rail used to power the LEMX-DC analog and digital domains, with support for supply-margin testing.
- **Block 2 – Buffer supply rails:** generation of the positive and negative supply voltages required by the external input-buffer stage.
- **Block 3 – Bias and reference network:** generation and routing of the reference and bias voltages needed by the ASIC during static and dynamic measurements.

- **Block 4 – Test access and observability:** routing of the key analog and digital nodes to connectors and test points so that the selected operating configuration can be measured in the laboratory.

This subdivision simplifies debugging and allows each subsystem to be verified independently before full-board integration.

3.3 Power Management Stage Design

To support supply-margin testing in the 3.0 V to 3.6 V interval, the power stage was designed around adjustable regulators rather than fixed-output devices. Block 1 is dedicated to the generation and controlled distribution of the primary 3.3 V rail, which powers both the analog and digital domains of the ASIC. The use of adjustable LDO regulators, specifically the LM317L, allows the output voltage to be tuned through external setting resistors (R_1 and R_2), making the board suitable for characterization under nominal and stressed operating conditions.

The power-distribution network also includes provisions for current measurements. By inserting a measurement bridge or jumper in the appropriate location, the current drawn by the ASIC can be evaluated independently of the rest of the discrete circuitry present on the board. The external power interface is implemented through standard 4-mm banana connectors, which provide the positive (V_{DD}) and negative (V_{SS}) input rails to the regulation stage.

Block 2 generates the dual supply rails required by the external input-buffer stage. This block incorporates two programmable LDOs. These regulators provide the biasing required by the analog front-end, with a nominal operating point of 5 V and -2 V. Because the negative rail directly affects the quality of the conditioned analog signal, a low-noise linear regulator such as the ADP7185 is used to minimize the injection of ripple and broadband noise into the measurement path. Dedicated test points are provided so that the effective output voltages of the regulators can be checked directly during board validation and troubleshooting.

3.4 Power Supply Unit (PSU) Design and Supporting Components

The PSU is designed to generate stable and low-noise supply rails while maintaining the flexibility required for electrical characterization and environmental stress testing. In this project, power integrity is not only a functional requirement, but also a measurement requirement: any ripple, drift, or inaccurate regulation would directly affect the accuracy of the analog front-end and, consequently, the validity of the acquired results.

3.4.1 Component Selection

The selection of the regulators was driven by two main criteria: the need for manual adjustability for margin testing and the need for ultra-low noise on the rails feeding the analog blocks. For this reason, the positive adjustable rails were based on the LM317L family, while the sensitive negative rail was assigned to a dedicated low-noise regulator.

LM317L Voltage Regulator (Variable Positive Voltage Section)

This regulator is used in **Block 1** to generate the primary 3.3 V supply rail and, when required, the 5 V rail used in Block 2. The main reason for its selection is the possibility of performing margin testing by varying the supply around the nominal value.

Key features based on the LM317L datasheet

- **Type:** Adjustable floating positive voltage regulator.
- **Voltage adjustability:** The output voltage can be programmed from 1.25 V to 32 V. This feature makes it possible to tune the supply in the 3.0 V to 3.6 V range by acting on the external resistors (R_1, R_2) and the adjustment trimmer (R_{adj}).
- **Current capability:** The LM317L version adopted here supports output currents up to 100 mA, which is adequate for the loads assigned to this stage.
- **Accuracy and stability:** Typical load regulation of about 0.5% and line regulation of about 0.01% provide sufficiently stable operation for characterization purposes.
- **Ripple rejection:** A typical power-supply rejection of about 80 dB at 120 Hz helps attenuate disturbances coming from the upstream supply.

Role in the project

The LM317L is the core element of the variable-supply test setup. By adjusting the feedback network, the board supply can be intentionally shifted above or below the nominal operating point, allowing the ASIC behavior to be evaluated under under-voltage and over-voltage conditions.

ADP7185 Regulator (Precise Negative Voltage Section)

This regulator is used in **Block 2** to generate the −2 V rail. This rail is critical for biasing the analog front-end and therefore requires a particularly clean supply.

Key features based on the ADP7185 datasheet

- **Type:** Negative low-dropout linear regulator.
- **Ultralow noise:** The output noise is approximately 4 μV_{rms} in the 100 Hz to 100 000 Hz band, making the device suitable for precision analog biasing.
- **Current capability:** The regulator can source up to −500 mA, providing ample margin for the expected negative-rail load.
- **High PSRR:** A high power-supply rejection ratio, about 68 dB at 10 kHz and 50 dB at 100 kHz, suppresses high-frequency ripple before it reaches the sensitive analog nodes.
- **Voltage range:** The device accepts an input between −2.0 V and −5.5 V and provides adjustable or fixed outputs from −0.5 V to −4.5 V.

Role in the project

The ADP7185 acts as the clean negative supply source for the analog path. By isolating the input-buffer stage from noise and ripple generated elsewhere on the board, it helps preserve the measurement accuracy required by the characterization setup.

3.4.2 Supporting Resistive Components

The regulator stages also rely on a suitable passive network for voltage setting, trimming, filtering, and long-term stability. In this design, the same resistor families selected for the rest of the board are also directly involved in the PSU implementation. Their choice was not dictated only by nominal resistance value, but also by long-term stability, trimming resolution, environmental robustness, and compatibility with repeated laboratory use.

General-purpose resistor positions in the feedback and monitoring networks are well suited to the Vishay D/CRCW e3 family, whose AEC-Q200 qualification and stable thick-film construction make it appropriate for standard biasing and current-limiting functions. Where fine manual adjustment is required, especially for supply trimming and reference calibration, the Bourns 3296 multiturn trimmer is advantageous because it provides high mechanical resolution and good long-term stability. The Stackpole HVC family is not the primary choice for the main low-voltage regulator loop, but its low voltage coefficient and high-impedance capability make it suitable for auxiliary divider or sensing locations whenever elevated impedance or high potential difference must be handled with good linearity.

Vishay D/CRCW e3: Standard Thick Film Chip Resistor

The D/CRCW e3 series is used as the baseline choice for general-purpose resistor positions on the board.

- **Technical architecture:** These resistors use a metal-glaze film deposited on a ceramic substrate. A protective overglaze improves environmental robustness, while pure tin terminations on a nickel barrier layer ensure good solderability and resistance to migration.
- **Key performance metrics:**
  - **Environmental stability:** $\Delta R/R \leq 1\%$ after 1000 hours at 70 °C.
  - **Qualification:** Fully AEC-Q200 qualified, making the family suitable for harsh operating environments.
  - **Operating range:** From -55 °C to 155 °C.
- **Project selection rationale:** The main reason for choosing the D/CRCW e3 family is its **proven reliability in demanding environmental conditions**. Using these components in pull-up, pull-down, divider, and current-limiting positions improves the robustness of the board during repeated laboratory use.

Stackpole HVC Series: Precision High-Voltage Chip Resistor

The HVC series is used where high impedance and high voltage handling are more important than compact low-cost implementation.

- **Advanced technology:** Unlike conventional thick-film devices, the HVC family uses fine-film deposition, which improves pulse performance and reduces excess noise.
- **High-voltage specifications:**
  - **Voltage capability:** Working voltages up to 3500 V for the 3512 size and up to 600 V for smaller 0805 packages.
  - **Voltage coefficient (VCR):** As low as 1 ppm/V, which helps maintain linearity as the applied voltage changes.
  - **Resistance range:** Available up to 50 GΩ.
- **Project selection rationale:** This family is useful as a **precision high-impedance divider or bleeder resistor**, especially in locations where high voltage capability and low VCR are necessary.

Bourns 3296: 3/8" Square Trimpot® Trimming Potentiometer

For subcircuits that require manual calibration, the Bourns 3296 provides the necessary adjustment resolution.

- **Mechanical design:** The device is a multiturn potentiometer with a worm-gear mechanism. Its 25-turn travel allows much finer adjustment than a single-turn trimmer.
- **Durability and sealing:**
  - **Chevron seal:** Suitable for board-washing processes and harsh industrial environments, with sealing compliant with MIL-STD-202.
  - **Material:** The cermet element provides a temperature coefficient of approximately $\pm 100\, ppm/^{\circ}\mathrm{C}$.
  - **Resolution:** The cermet track provides effectively continuous adjustment.
- **Project selection rationale:** The 3296 was selected for **voltage reference tuning and fine manual calibration**. Its high adjustment resolution reduces the risk of accidental overcorrection and helps maintain the set value over time.

3.4.3 Comparative Summary

Feature	LM317L (Positive)	ADP7185 (Negative)
Primary function	Variable voltage supply	
(3.3 V and 5 V)	Clean analog supply	
(−2 V)		
Max current	Up to 100 mA	Up to −500 mA
Noise / ripple behavior	Ripple rejection: about 80 dB	Output noise: 4 μV_{rms}
Selection reason	Easy adjustability for margin testing	Ultralow noise for analog precision

Table 3.1: Comparison between the positive and negative regulators used in the PSU.

3.5 Reference and Bias Generation

Block 3 generates the main reference and bias nodes required by the ASIC. The target nominal voltages for the key nodes are the following:

- $V_{CASC\_BUFI} = 1.0\,\mathrm{V}$, generated from V_{analog} using variable resistor VR5 set to approximately 690 kΩ.
- $V_{CASC\_ADC} = 1.65\,\mathrm{V}$, generated from V_{analog} using variable resistor VR5 set to approximately 300 kΩ.
- $V_{REFN} = 1.15\,\mathrm{V}$, directly routed to pin 26 as required by the ASIC bias scheme.

Feature	Vishay D/CRCW e3	Stackpole HVC	Bourns 3296
Type	Standard thick film	Precision high voltage	Multiturn trimmer
Resistance range	$1\,\Omega$ to $10 \times 10^6\,\Omega$	$10 \times 10^3\,\Omega$ to $1 \times 10^{12}\,\Omega$	$10\,\Omega$ to $2 \times 10^6\,\Omega$
Standard tolerance	±1% to ±5%	Down to ±0.1%	±10%
Max working voltage	Up to 500 V	Up to 3500 V	300 V dielectric strength
Temperature range	−55 °C to 155 °C	−55 °C to 150 °C	−55 °C to 125 °C
Key feature	AEC-Q200 qualified	Low VCR (1 ppm/V)	25-turn adjustment

Table 3.2: Comparison of the technical specifications of the selected resistor families.

- $V_{REFP} = 2.15\,\text{V}$, directly routed to pin 24.
- $AGND = 1.65\,\text{V}$, directly routed to pin 25 and used as the analog common-mode reference.
- The I_{BIAS} setting node is designed for approximately 1.4 V and 5 µA, in accordance with the target bias current.

These target values define the nominal operating point for the analog front-end and the ADC bias network during standard measurements. The bias-current generation stage is designed so that the relevant node can be checked directly on the board, for example through a dedicated jumper or test access, thereby supporting rapid validation during the initial turn on phase.

3.5.1 Voltage Divider / Reference Voltage

The output voltage produced by the resistive divider is

$$V_x = 3.3\,\text{V} \cdot \frac{R_F}{R_F + R_V} \tag{3.1}$$

Rearranging the expression gives

$$V_x(R_F + R_V) = 3.3\,\text{V} \cdot R_F \tag{3.2}$$

and solving for R_V yields

$$\boxed{R_V = \left(\frac{3.3 - V_x}{V_x}\right) \cdot R_F} \tag{3.3}$$

3.5.2 Current Through Reference

When the equivalent resistance is high, the current remains in the order of a few microamperes:

$$I = \frac{V_x}{R} \tag{3.4}$$

3.5.3 Total Resistance Calculation

For a 3.3 V supply, a 1.4 V reference, and a target current of 5 µA, the total resistance is

$$R_{TOT} = \frac{3.3\,\text{V} - 1.4\,\text{V}}{5\,\mu\text{A}} = 380\,k\Omega \tag{3.5}$$

3.5.4 RV Values for Different Output Voltages

Starting from $V_{ref} = 3.3\,\text{V}$ and assuming $R_F = 300\,\text{k}\Omega$:

Output voltage	R_V **(in terms of** R_F**)**	R_V **value**	**Current** I
1.0 V	$2.3\,R_F$	690 kΩ	3.3 µA
1.65 V	$1.0\,R_F$	300 kΩ	5.5 µA
1.15 V	$1.87\,R_F$	561 kΩ	3.83 µA
2.15 V	$0.54\,R_F$	162 kΩ	7.16 µA

Table 3.3: Resistor values and currents for various reference output voltages.

As an additional design example, for $R_{TOT} = 1.9\,\text{M}\Omega$ one obtains:

$$R_F = 350\,k\Omega, \qquad R_V = 1.75\,M\Omega \tag{3.6}$$

3.6 Passive Components Summary

Component	**Value**	**Notes**
Capacitor (C_{IN})	30 µF	Compatible with the regulator specifications
Capacitor (C_{BYP})	3 µF	Compatible with the regulator specifications
Trimmer	—	Required for fine voltage adjustment

Table 3.4: Summary of the passive components used in the reference and bias network.

3.7 Observable Outputs and STROBE Routing

Block 4 routes the main observable outputs required for functional verification of the selected test configuration. In the standard single-channel setup (channel 0), the following signals are made available to the user:

- `LAM_S<0>`
- `DATA_OUT<0>`
- `DATA_OUT_N<0>`
- `EN_RE_ALIGN<0>`
- `SEU_OUT`
- `STROBE`

All of these signals are brought out to pin headers and buffered in order to isolate the ASIC outputs from probing capacitance and external loading. STROBE is particularly useful during readout because it acts as a timing marker aligned with the relevant clock phases, making waveform interpretation and debug considerably easier. A selectable routing option also allows either STROBE or CK to be forwarded to the buffered observation point through a dedicated jumper. Figure 3.1 shows the 3D view of the PCB used in the documentation.

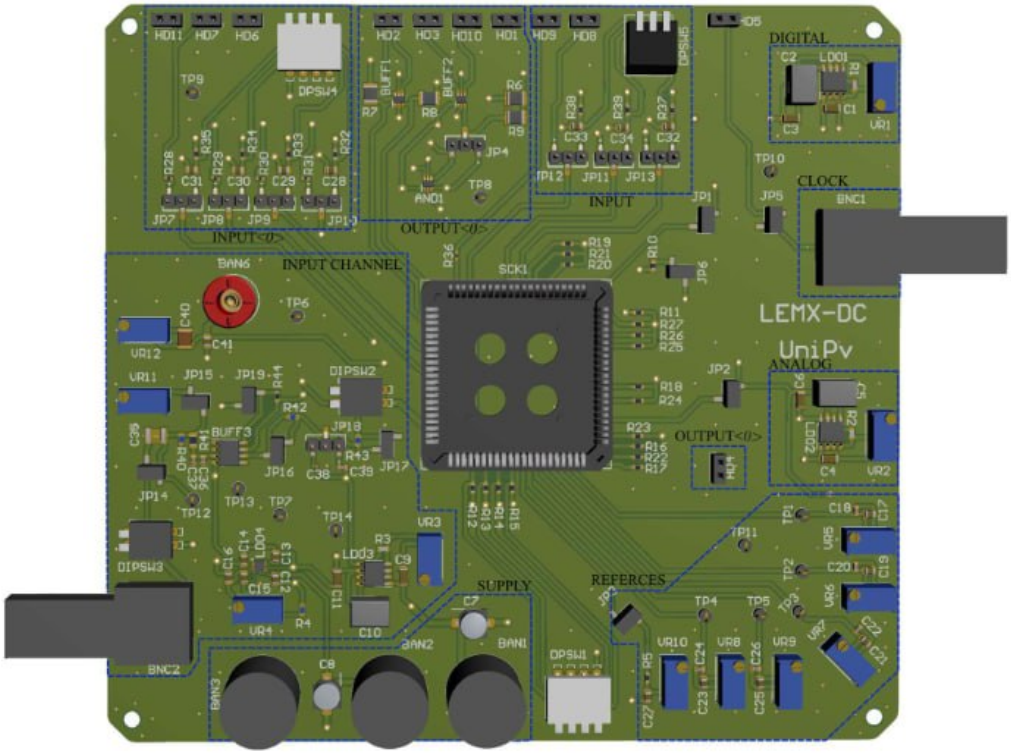

Figure 3.1: 3D overview of the board and its main connectors.

3.7.1 SN74LVC1G11: Single 3-Input Positive-AND Gate

Component details:

- **Functionality:** Single 3-input positive-AND gate implementing the Boolean function $Y = A \cdot B \cdot C$.
- **Voltage rating:** Operates from 1.65 V to 5.5 V, with inputs tolerant up to 5.5 V.
- **Performance:** Maximum propagation delay of about 4.1 ns at 3.3 V, with ±24 mA drive capability.
- **Power:** Very low supply current, with a maximum I_{CC} of about 10 µA.
- **Protection:** ESD robustness above 2000 V HBM and 1000 V CDM, with latch-up tolerance above 100 mA according to JESD 78 class II.

3.7.2 SN74LVC2G34 and Logic-Buffering Advantages

Component details:

- **Functionality:** Dual non-inverting buffer gate implementing the positive-logic relation $Y = A$.
- **Voltage rating:** Designed for 1.65 V to 5.5 V operation, with inputs tolerant up to 5.5 V.
- **Performance:** Maximum propagation delay of about 4.1 ns at 3.3 V, with ±24 mA output drive capability.
- **Power:** Maximum quiescent current of about 10 µA.
- **Protection:** ESD protection includes 2000 V HBM, 200 V MM, and 1000 V CDM ratings.

The use of the SN74LVC1G11 and SN74LVC2G34 devices provides several practical advantages in the observation network:

- **Level translation compatibility:** Because the inputs can tolerate voltages up to 5.5 V independently of the supply level, these devices simplify the interface between logic domains operating at different voltages.
- **Power efficiency:** Their low quiescent current makes them well suited to a characterization setup in which unnecessary local power dissipation should be minimized.
- **Partial-power-down support:** The I_{off} capability prevents damaging backflow currents when one part of the system is unpowered.
- **Compact implementation:** The small package options reduce the board area required by the observation network.
- **Robust output drive:** The available output current is sufficient to drive headers, short cables, and moderate probing loads without significantly degrading the logic signal quality.

The following signals are also equipped with pull-down resistors to guarantee a defined default state when they are not actively driven:

- LAM_S<0>
- DATA_OUT<0>
- DATA_OUT_N<0>
- STROBE

3.8 Clock Input and Conditioning

3.8.1 Block 5: Clock Distribution

Block 5 implements the clock input, basic conditioning, and distribution network. The clock is brought to the board through a 50 Ω BNC connector. In the selected operating mode, CK is used as the active clock input, while CKN is forced to a defined logic level through a pull-down network.

The block also provides on-board termination and routing options. Depending on the selected configuration, a 50 Ω termination or series element can be inserted to improve signal integrity, and the clock can be forwarded to a header for direct observation. In the implemented network, $R10 = 50\,\text{k}\Omega$ and $R11 = 100\,\text{k}\Omega$ are used to establish the required pull-down conditions.

3.8.2 Unused-Pin Management

Unused or configuration-dependent pins are managed through DIP switches and pull-down resistors so that they remain in a known logic state during operation. The configured pins include:

- SE_S_H (mode selection)
- ATT_N (gain / attenuation selection)
- EN_EN_RE_ALIGN (aligner enable)

- PD_ANA_ALL (analog power-down control)
- INP<6>, INN<6>
- EN_CAL<6>, TRIGGER<6>, SER_EN<6>, RESET_ACQ<6>
- INP<7>, INN<7>
- EN_CAL<7>, TRIGGER<7>, SER_EN<7>, RESET_ACQ<7>

3.9 The Analog Input Stage (Block 7)

The analog front-end of the PCB is designed to interface standard laboratory equipment, such as signal generators, with the custom ASIC inputs. Block 7 implements the analog input path used during characterization. In the standard setup, the excitation signal is applied through a BNC connector and can follow one of two paths selected by a DIP switch: a direct path, which routes the source to the ASIC input for comparison purposes, and a filtered path, which passes through the on-board band-pass filter before reaching the device under test. The direct path is not intended for the final operating mode; it is provided as a diagnostic option to compare the behavior of the raw and conditioned signals.

The filtered path improves signal conditioning before conversion and suppresses unwanted spectral components outside the useful band. The high-pass section is implemented by the interaction of $R40$ with $C35$, which defines the lower cut-off frequency and removes slow drifts and offset components. The low-pass section is formed by $R41$ together with $C36$ and $C37$, thereby limiting the upper-band content and attenuating high-frequency noise. The overall response therefore behaves as a band-pass filter with an approximate useful range from 60 Hz to 6.25 kHz.

A variable resistor is used to adjust the DC operating point of node A so that the waveform is centered within the available analog range. For example, if the input signal spans approximately from 0.3 V to 1.6 V, its midpoint is close to 0.8 V; the adjustable network is therefore tuned so that node A tracks this intermediate bias level. This operation is performed with respect to the analog supply and the ratio between $R40$ and $VR11$, ensuring that the input common-mode voltage remains compatible with the expected ASIC operating range.

This conditioning stage allows the user to compare the ASIC response under two controlled conditions: direct unfiltered excitation and band-limited excitation. The filtered path is the one intended for normal use because it reduces interference and improves measurement repeatability, whereas the direct path remains useful during debugging and laboratory verification. In this way, Block 7 supports both practical turn on activities and controlled signal-quality comparisons during characterization.

Figure 3.2 shows the schematic excerpt of the board-level laboratory input network used to implement the direct and filtered paths.

3.9.1 High-Impedance Buffering

Directly connecting the signal source to the sample and hold switching input of the delta-sigma modulator can lead to settling errors due to possible bonding parasitic inductance related ringing. To prevent this, unity-gain buffers are implemented using high-speed, low-noise operational amplifiers such as the AD8066.

- **Impedance matching:** The buffer presents a high input impedance to the source and a low output impedance to the ADC input (IN_P, IN_N).

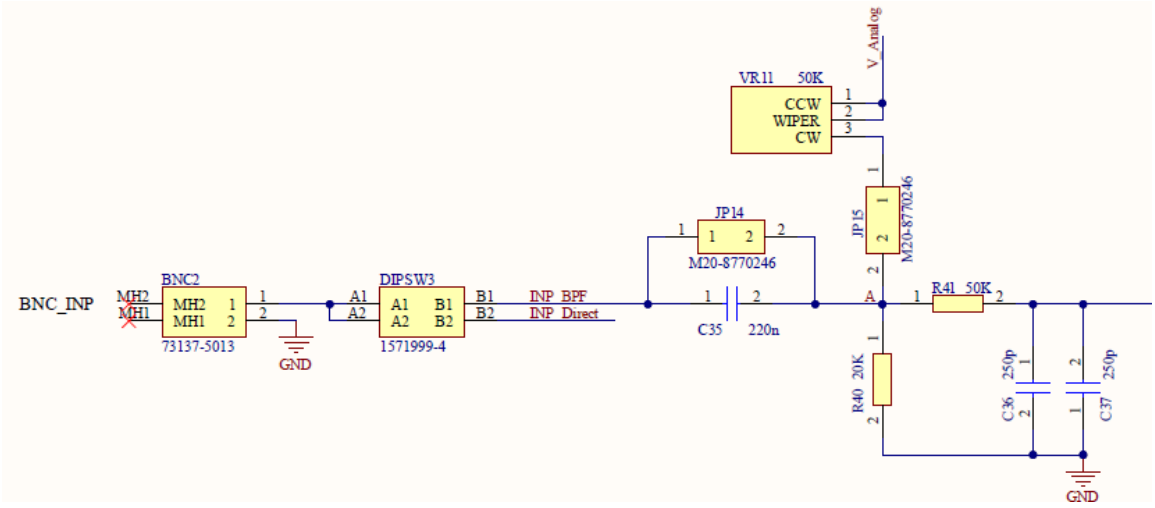

Figure 3.2: Schematic excerpt of the board-level input network used during characterization.

- **Common-mode setting:** A resistive divider sets the input common-mode voltage to 1.65 V ($V_{DD}/2$), centering the signal within the available supply range.

3.9.2 Connectivity

Standard BNC connectors are used for the analog inputs in order to provide robust shielding against environmental electromagnetic interference (EMI).

3.10 Device Under Test (DUT) Interface

The central element of the PCB is the interface dedicated to the LEMX-DC.

- **JLCC-84 socket:** An 84-pin J-leaded chip carrier socket is used to allow non-destructive testing of multiple ASIC samples.
- **Pin routing:** The routing follows the *LEMX_DC_pinsorting* document. Particular care was taken to keep the analog (AV_{DD}) and digital (DV_{DD}) supply paths physically separated in order to reduce crosstalk.

3.11 Digital Connectivity and FPGA Interface

3.11.1 Connector Selection

A **Samtec QTE-040-01-L-D-A** connector is used to interface the board with the external digital electronics. This connector satisfies the required pin count while remaining compatible with the target signal-speed constraints.

3.11.2 Signal Integrity on Digital Lines

The digital outputs ($DATA\_OUT < 0 : 7 >$) and the clock lines (CK, CKN) exhibit fast transitions. To limit reflections, **series termination resistors** in CRCW0402 packages with a nominal value of 49.9 Ω are placed close to the source pins. This choice helps maintain clean digital edges during operation at 15 MHz.

3.12 Grounding Strategy

To reduce noise coupling, the PCB adopts a **star-grounding** strategy:

- **Separation:** Analog ground (AGND) and digital ground (DGND) are maintained as separate copper regions on the board.
- **Connection point:** The two grounds are connected at a single star point close to the power-entry connector so that noisy digital return currents do not flow through the sensitive analog reference path.

Chapter 4

Measurement

This chapter collects the laboratory instrumentation used for the first validation campaign and outlines the main electrical quantities that must be acquired from the test platform. Since the present revision of the thesis is primarily focused on board design and laboratory preparation, the chapter emphasizes the measurement workflow, the role of each instrument, and the observables that will be compared against design expectations.

The measurement activity is organized around three complementary goals: verifying that the board powers the ASIC safely and reproducibly, confirming that the analog conditioning path behaves as expected, and observing the timing relationship between clock, strobe, and digital data outputs during conversion. The selected instruments therefore cover both static measurements, such as bias voltages and current consumption, and dynamic measurements, such as waveform integrity, trigger alignment, and digital readout activity.

4.1 Measurement Tools

4.1.1 Function Generator

A function generator is the primary stimulus source used to excite the analog input path with repeatable test waveforms. In general, this class of instrument can generate standard repetitive signals such as sine, square, triangular, and sawtooth waveforms over a wide frequency range, with controllable amplitude, offset, and timing characteristics. More advanced signal generators can also perform sweep-based tests and generate deliberately impaired or distorted signals to study how a device under test behaves under non-ideal operating conditions [13].

Within this project, the function generator is used to apply controlled excitation to the input BNC connector of Block 7. Its main role is to verify the response of the direct path and of the band-pass-filtered path, to sweep the useful frequency band, and to evaluate whether the conditioned waveform presented to the ASIC remains compatible with the intended common-mode and dynamic-range constraints. Because the function generator is deterministic and easily repeatable, it is also the natural reference instrument for correlation between laboratory observations and circuit simulations.

4.1.2 Power Supply

A bench power supply is the instrument responsible for delivering clean and stable DC power to the device under test. In laboratory practice, it is valued not only because it can provide a specified output voltage and current, but also because it allows the user to set current limits, monitor load conditions, and minimize damage in the event of wiring or start-up faults. Official Keysight application material emphasizes that a good bench supply must provide stable output,

suitable regulation, and protection features while remaining easy to configure for general-purpose testing, circuit biasing, troubleshooting, and teaching-lab activity [14].

For the present board, the external bench supply feeds the PCB regulation stages and therefore determines the quality of the upstream electrical environment seen by the on-board regulators. During the first measurements, it is especially useful for controlled turn on, current-limited start-up, and supply-margin testing around the nominal operating conditions. In addition, it allows the behavior of the adjustable on-board rails to be checked under different input conditions, helping distinguish between external-supply effects and board-level regulation effects.

4.1.3 Digital Multimeter

The digital multimeter is the standard instrument for accurate measurement of electrical quantities such as voltage, current, and resistance. Compared with older analog meters, a digital multimeter provides direct numerical readout, improved accuracy, high input impedance, and a wider set of test functions collected into a single bench or handheld instrument. Fluke describes the DMM as a versatile electrical test tool that combines the functionality of several traditional meters and is routinely used for diagnostics, component checks, and laboratory verification of electrical quantities [15].

In this work, the digital multimeter is essential for static validation of the PCB before any full dynamic acquisition is attempted. It is used to verify the main supply rails, the reference nodes, the generated analog common-mode level, and the bias-setting voltages described in the previous chapter. It also supports current-consumption checks and continuity verification during assembly and debugging. Because these measurements are comparatively low bandwidth but high importance, the DMM serves as the first instrument used to confirm that the board is safe and correctly biased before the oscilloscope or logic-analysis tools are connected.

4.1.4 Logic Analyzer

The logic analyzer used in this activity is based on the Tektronix TLA5202B family documentation provided with the thesis material. According to the datasheet, the TLA5202 offers 68 acquisition channels, supports up to 235 MHz state acquisition, and combines deep timing acquisition with 125 ps MagniVu high-resolution timing. The associated manual also highlights integrated analysis functions such as waveform and listing views, setup/hold violation analysis, and time-correlated operation with an external oscilloscope through the iView capability [16, 17].

For the characterization board, the logic analyzer is the key instrument for observing the digital behavior of the ASIC and of the test-interface circuitry. It is intended to capture signals such as STROBE, DATA_OUT<0>, DATA_OUT_N<0>, LAM_S<0>, and other timing markers routed to the observation headers. Its value is not limited to simple state decoding: by correlating edges, trigger positions, and digital transitions over multiple channels, it allows the readout sequence of the converter to be checked against the expected logical behavior and against the timing assumptions used in simulation.

4.1.5 Digital Discovery

Digilent describes the Digital Discovery as a compact mixed digital instrument centered on logic analysis and pattern generation. The official reference material presents it as an embedded-development companion that combines a logic analyzer, pattern generator, digital I/O, protocol-analysis tools, and software control through the WaveForms environment. Depending on the active channel configuration and accessories, the device can reach high digital sample rates, while its configurable logic levels make it adaptable to a range of low-voltage digital systems [18, 19].

In the context of this project, the Digital Discovery complements the bench logic analyzer rather than replacing it. Its portability and rapid software setup make it convenient for quick checks during assembly, continuity validation of digital paths, and exploratory observation of control lines before migrating to a more comprehensive acquisition on the Tektronix system. It is also useful when simple pattern generation or lightweight digital stimulus is needed for auxiliary tests, especially during iterative debugging of connectors, pull-down networks, or observation headers.

4.1.6 Oscilloscope

An oscilloscope is the primary instrument used to visualize electrical signals as a function of time. Tektronix defines it as a diagnostic instrument that draws a graph of an electrical signal and emphasizes that practical oscilloscope performance depends on several fundamental parameters, including bandwidth, rise time, sample rate, record length, and triggering capability. These characteristics determine whether the instrument can capture a waveform faithfully, resolve fast transitions, and reveal intermittent events without aliasing or misleading distortion [20, 21].

For this characterization platform, the oscilloscope is the main tool for observing the analog input waveform, the conditioned node after filtering, and the quality of fast transitions on selected digital or clock lines whenever an analog view is useful. It enables direct verification of amplitude, offset, settling, filter behavior, and transient events that would not be visible through static measurements alone. When used together with digital timing instruments, the oscilloscope also helps establish a more complete picture of the interaction between analog excitation and digital conversion activity on the board.

4.2 Measurement Procedure, Setup, and Preliminary Results

This section consolidates the measurement procedure and the first experimental results obtained with the LEMX-DC characterization platform. The material is based on the dedicated test report and is included here to establish a direct link between the hardware platform described in Chapter 2 and the first laboratory validation campaign performed on silicon.

4.2.1 Step-by-Step Acquisition and Readout Sequence

Figure 4.1 summarizes the control and observation sequence used during a basic measurement on the LEMX-DC test PCB. The standard configuration is intended for single-ended operation on a single channel (channel 0). In this mode, the stimulus is applied to the positive input, while the negative input is kept at the defined reference level; `CKN` is not used and the clock is provided through `CK` only. Before starting, the supply rails and reference/bias nodes must be correctly set and stable, and the instruments must be connected to the appropriate headers and test points.

The first required action is to set the static configuration inputs to the desired operating mode before enabling an acquisition, and to keep them stable throughout the measurement. In the standard single-ended setup, `ATT_N`, `SE_S_H`, and `DATA_CAL` are set according to the default operating configuration and are kept constant during the conversion and readout window. The serial interface is initialized by the global `RESET`; therefore `SER_RES` is optional and can remain inactive unless a dedicated re-initialization of the serial block is needed without toggling `RESET`. If calibration is not part of the current run, `EN_CAL` is kept inactive and `DATA_CAL` remains at its default logic level. Conversely, if calibration is required, `EN_CAL` is asserted and the intended calibration stream is applied on `DATA_CAL` following the dedicated calibration procedure, after which `EN_CAL` is returned to the inactive state before starting the measurement.

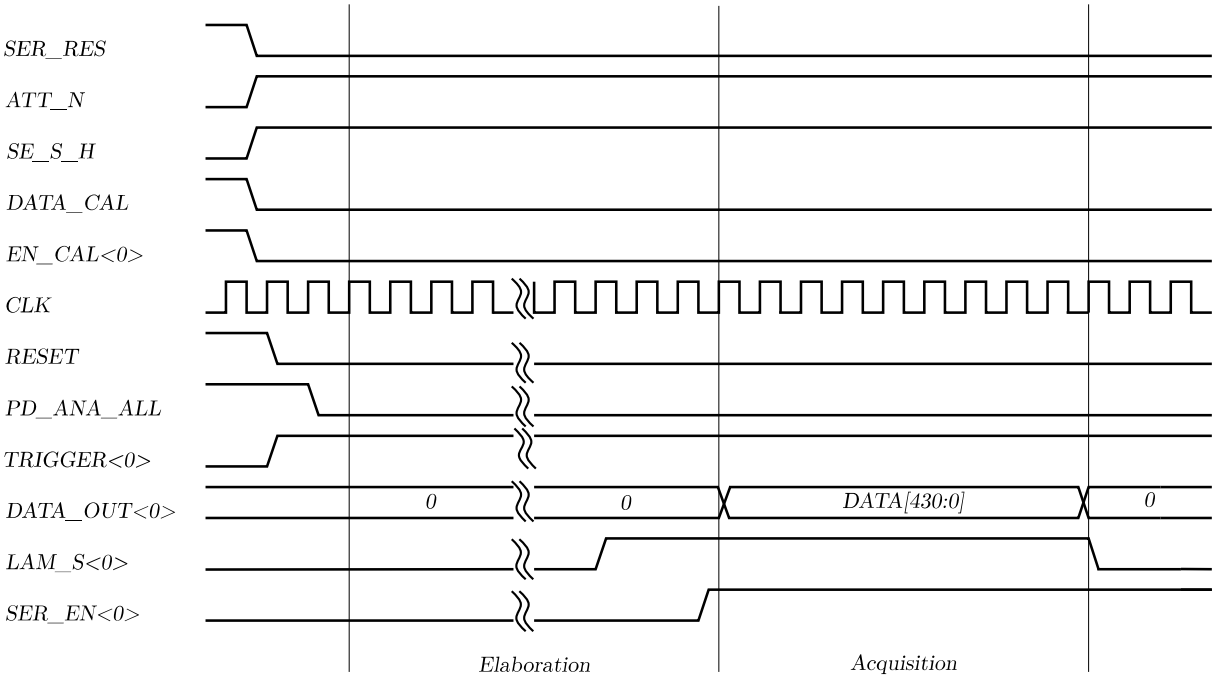

Figure 4.1: Timing diagram of the measurement flow.

The clock is then applied on CK and kept running continuously throughout the procedure, while CKN remains unused. With the clock active, RESET is asserted high to initialize the system registers and then deasserted to enter normal operation. The analog section is explicitly enabled by setting PD_ANA_ALL to logic 0, after which a short settling time is allowed so that the biasing and reference nodes reach steady state before TRIGGER is issued. The acquisition starts by asserting TRIGGER; after the trigger is detected, the logic enters the internal processing interval indicated as *Elaboration* in Figure 4.1, during which the system completes the conversion and readout preparation and DATA_OUT remains in its idle state. At the end of the conversion sequence, the logic asserts LAM_S to indicate end-of-scan and data-ready status.

Once LAM_S is asserted, the measurement data can be read out. Serial transmission is enabled by asserting SER_EN; the converted data are then shifted out on DATA_OUT as a single frame, denoted in the report as DATA[430:0]. The serial stream is synchronous with CK and follows the defined timing: DATA_OUT is updated on the falling edges of the clock. When the frame is complete, DATA_OUT returns to the idle level and SER_EN can be deasserted, concluding the transmission. This sequence provides a reproducible baseline procedure for external laboratory users.

4.2.2 Measurement Scope and Test Setup

The electrical characterization and functional verification campaign is organized so as to progressively validate device operation, starting from basic single-path functionality checks and extending toward multi-channel operation and preliminary static and dynamic performance evaluation. The main classes of measurements considered in the campaign are the following:

- **Single-path functionality verification:** known input signals are applied to a single acquisition path, following the acquisition and readout protocol defined by the control logic. This provides a qualitative verification that the ASIC correctly performs sampling, conversion, and serialization according to the expected behavior.

- **Multi-acquisition-path functionality verification:** the functionality of multiple acquisition paths is verified by enabling more than one Sample-and-Hold block and exercising the serial stream-in mechanism. This test is not necessarily performed on all 32 sub-channels

during the initial campaign, but it validates the multi-channel architecture and the shared digital resources.

- **Spot static performance evaluation:** known static input values are applied to the analog input and the corresponding digital output codes are acquired. Linearity is then evaluated by analyzing the measured codes and comparing them against the expected response, providing a first-order assessment of the static performance.
- **Quasi-static and dynamic performance evaluation:** a slowly varying input signal, such as a low-frequency sinusoid or a slow ramp, is applied to a single acquisition path. The output data stream is recorded and processed offline through FFT-based tools in order to extract figures of merit such as SNR, SNDR, and dynamic range. In this context, the term quasi-static refers to low-frequency excitation around 100 Hz, while dynamic performance is intended to extend toward higher frequencies up to about 1 kHz.

Unless otherwise specified, these measurements are performed on a single acquisition path. A satisfactory verification with static input signals is considered a prerequisite before moving to the more demanding dynamic measurements.

Test Instrumentation

The laboratory equipment used for the measurements includes a dual power supply (+7 V, -5 V), an HP Universal Source signal generator and/or an Audio Precision signal generator, a pattern generator or Digital Discovery, an HP and/or Digital Discovery logic analyzer, a Keithley multimeter, and an oscilloscope for test-point monitoring. The role of these instruments within the thesis framework was introduced in Section 3.1; here they define the practical bench used during the first measurement campaign.

4.2.3 Experimental Setup and Operating Conditions

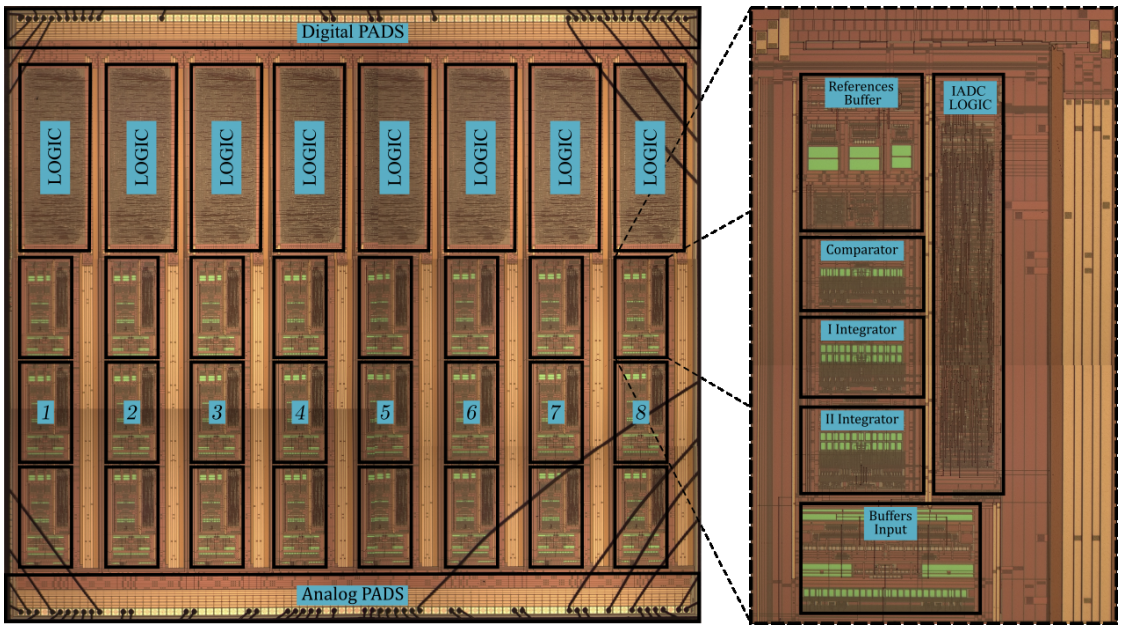

Figure 4.2: Optical micrograph of the complete LEMX-DC ASIC together with a magnified view of a representative channel, highlighting the main IADC building blocks: first integrator, second integrator, comparator, reference buffers, and internal logic.

Because of a delay in the delivery of the fabricated chip, which became available only at the beginning of April, the first measurement campaign was limited to a preliminary static

characterization of the ASIC. For completeness, Figure 4.2 reports an optical micrograph of the fabricated LEMX-DC ASIC together with a magnified view of a representative channel. The image highlights the eight integrated channels and shows the main IADC building blocks, namely the first integrator, second integrator, comparator, reference buffers, and the internal logic.

Measurement Setup

This section describes the experimental setup adopted for the preliminary static characterization of the LEMX-DC. First, the board configuration, bias conditions, and digital control settings are introduced; then the input stimulus, clock conditions, and output-acquisition strategy are discussed.

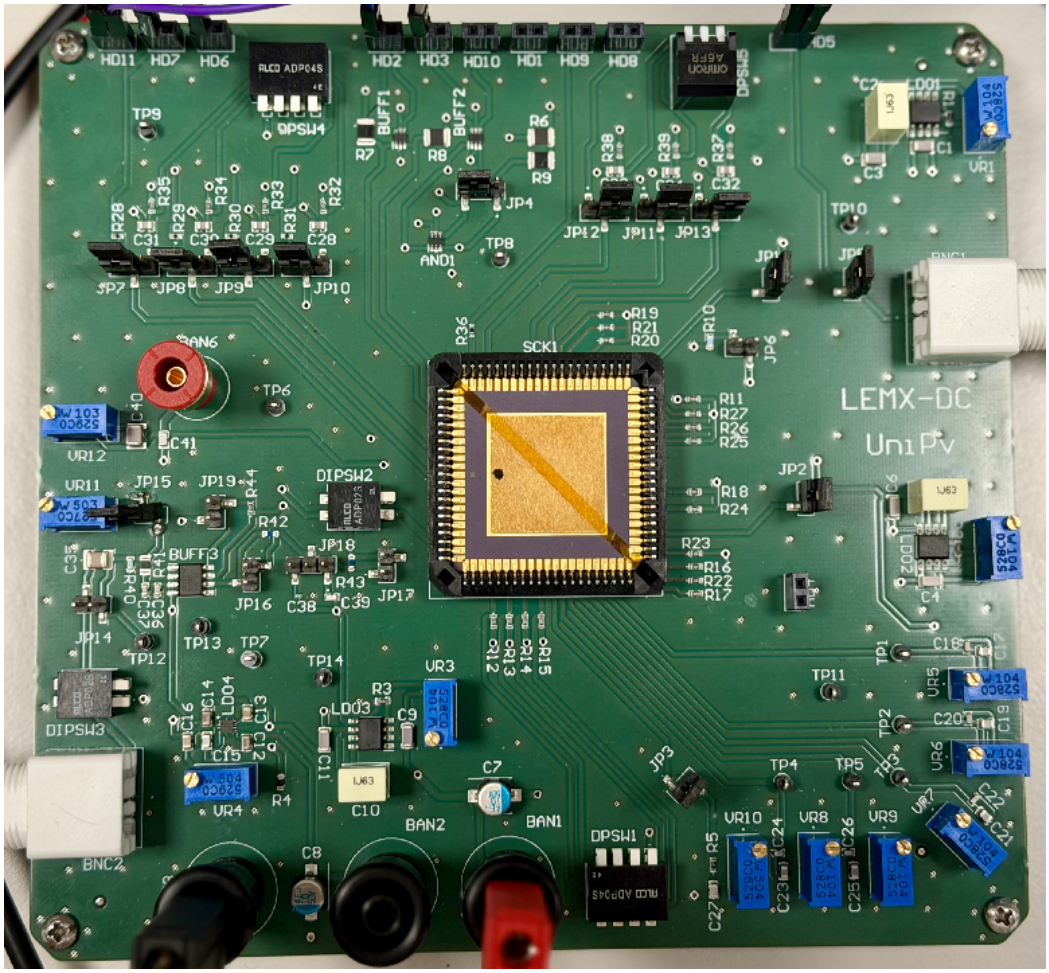

Figure 4.3: Photograph of the LEMX-DC characterization PCB with the ASIC mounted in the JLCC84 package used for the preliminary measurement campaign.

The measurements were performed using the dedicated LEMX-DC characterization PCB, whose architecture and main functional sections were described in Chapter 2. As shown in Figure 4.3, the ASIC was assembled in a JLCC84 package and mounted on the dedicated test board used for the experimental activity. In the adopted package configuration, three channels out of the eight available ones were wire-bonded, namely channels 0, 6, and 7. This first revision of the characterization board was specifically conceived for the experimental validation of a bonded channel, and the preliminary characterization was therefore carried out on channel 0.

The experimental setup is shown in Figure 4.4. The measurement bench included a DC power supply, a digital multimeter, two function generators, a Digital Discovery unit, an oscilloscope, and a logic analyzer. Within this setup, the DC power supply was used to bias the characterization

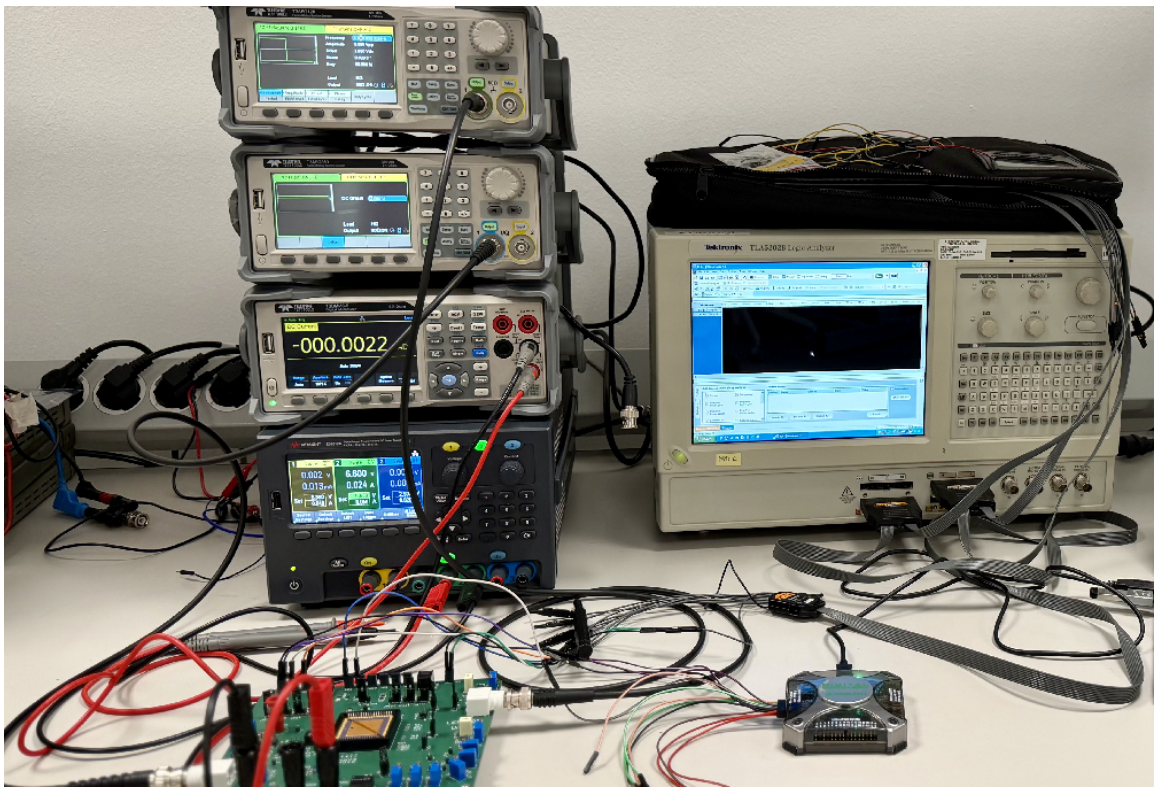

Figure 4.4: Experimental setup used for the preliminary LEMX-DC characterization, including the characterization PCB, power supply, function generators, Digital Discovery, oscilloscope, and logic analyzer.

board, while the digital multimeter was used for preliminary electrical checks. Two function generators were employed to independently provide the input stimulus and the clock signal. The Digital Discovery was used to generate the local digital control signals required by the channel under test. The oscilloscope was used to inspect waveform quality during the setup phase, whereas the logic analyzer was used to acquire the serialized output word produced by the ASIC.

Before starting the measurements, the PCB was configured by applying the required supply voltages and bias conditions to the ASIC. The supply and bias values adopted in the campaign are summarized in Table 4.1.

Table 4.1: Supply and bias conditions used during the measurements.

Parameter	**Value**
DVDD	3.3 V
AVDD	3.3 V
I_{bias}	5 µA
$V_{\text{CASC\_BUFI}}$	1.0 V
$V_{\text{CASC\_ADC}}$	1.65 V
V_{REFN}	1.15 V
V_{REFP}	2.15 V
AGND	1.65 V

The static configuration of the global control signals was implemented through two on-board DIP switches. These signals directly affect the operating conditions of the ASIC during the measurement setup and therefore had to be carefully defined before the acquisition phase. The selected configuration is reported in Table 4.2. Particular attention was given to the configuration of `SE_S_H` and `ATT_N`, since these signals directly determine the analog operating

mode used during the test. In the adopted setup, the high logic level applied to these pins enabled the configuration selected for the preliminary static characterization. In particular, ATT_N set the attenuation of the first integrator to 2/3, while the combined configuration of SE_S_H and ATT_N allowed correct operation with the pseudo-differential input conditions used in the measurements. The RESET signal was instead used before and after each measurement sequence in order to initialize the chip and clear the internal register contents, thus ensuring repeatable acquisition conditions.

Table 4.2: Global control signals used in the measurement setup.

Signal	**Setting**
SE_S_H	High
ATT_N	High
EN_EN_RE_ALIGN	Low
PD_ANA_ALL	Low
DATA_CAL	Low
RESET_CAL	Low
SER_RES	Low

In addition to the global signals, the local control signals associated with channel 0 were externally generated during the measurements by means of the Digital Discovery unit. In particular, the signals RES_ACQ<0>, TRIGGER<0>, EN_CAL<0>, and SER_EN<0> were driven externally in order to control the acquisition and readout sequence of the channel under test. This solution made it possible to operate the channel in a flexible and controlled way throughout the measurement activity, while also reducing the risk of signal-integrity issues that could arise from less controlled manual driving.

Input Stimulus, Clock Conditions, and Output Acquisition

The board was powered by an external DC power supply set to 6.6 V (values from 6.5 V to 8 V are fully compliant) and limited to 50 mA, namely one order of magnitude above the expected current consumption of a single channel. This external input supplied the on-board low-dropout regulators, which in turn generated the clean and stable internal voltage rails required by the ASIC. A digital multimeter was used to verify the main DC operating conditions during the setup phase and to confirm correct biasing before the measurements started.

Two independent function generators were employed: one provided the analog input signal, while the second generated the clock. This choice was made in order to keep the input path and the clock path fully independent, thus minimizing the possibility that coupling or disturbances generated by the clock source could directly affect the analog input signal during the characterization. The voltage sweep applied to INP<0> ranged from 500 mV to 2 V. This range was selected to investigate the ASIC behavior over essentially the full input dynamic range.

Although the nominal clock target for the characterization was between 15.0 MHz and 16.5 MHz, the actual measurement campaign was carried out using a 5 MHz clock. This limitation was introduced after signal-integrity issues were observed along the clock path from the board input to the chip. In particular, oscilloscope inspection showed that, at higher frequencies, the clock waveform became significantly distorted and this affected both the rising and falling edges, making the signal unsuitable for reliable conversion. The observed behavior is consistent with an impedance mismatch between the function generator and the chip input path, which produced reflections along the line and degraded the waveform quality at the ASIC pins. A dedicated impedance-matching solution based on additional parallel resistors is planned for the next revision of the setup in order to mitigate this issue. Since this corrective action could not

be implemented in time for the present preliminary campaign, the clock frequency was reduced to 5 MHz, leading to a complete scan duration of about 250 µs instead of the nominal 80 µs. At this lower frequency, the clock edges were sufficiently clean to avoid conversion inaccuracies associated with waveform distortion.

Finally, the digital output word was acquired by means of a logic analyzer. The signals connected to the analyzer were the ASIC serialized output, SER_EN<0>, and the clock. Since the ASIC serializes the output word on the falling edge of the clock, the logic analyzer was configured to sample the output on the rising edge, so that the data could be read when stable on the bus. Acquisition synchronization was obtained by using SER_EN<0> as the trigger signal for the logic analyzer, so that the analyzer started acquiring data only when the serialized output word was effectively being transmitted by the ASIC, ensuring correct temporal alignment between the control sequence and the acquired output stream.

Measurement Procedure

At the beginning of each acquisition, a RESET signal was applied in order to initialize the internal registers of the ASIC. After the reset phase, the TRIGGER<0> signal was asserted and the LAM_S<0> signal was monitored by means of the Digital Discovery unit. As soon as LAM_S<0> was asserted, the SER_EN<0> signal was applied to enable serialization of the output word. The serialized output data were then acquired by means of the logic analyzer. The acquired output word was saved as a .txt file and subsequently processed offline in MATLAB. This post-processing step was used to reconstruct the output code sequence, extract the transfer characteristics of the three ADCs, evaluate the deviation from the ideal behavior, and compute the corresponding resolution metrics.

4.2.4 Preliminary Static Characterization Results

The results obtained from the preliminary static characterization were organized according to the three ADCs operating within the channel. As discussed in the architectural description, one complete scan is distributed among the three converters: ADC0 and ADC1 each perform 11 conversions, whereas ADC2 performs 10. Consequently, the static results are presented by grouping the conversions associated with each ADC and then combining them into global performance indicators representative of the full-scan behavior.

Linearity

The measured static linearity results are reported in Figures 4.5–4.7, with one plot for each ADC. Each curve corresponds to one conversion within the complete scan sequence. As expected from the channel architecture, ADC0 and ADC1 are each represented by 11 transfer characteristics, while ADC2 is represented by 10. The measured response remains substantially linear over the entire explored input range, from 500 mV to 2.0 V, for all the analyzed conversions. This behavior confirms the correct code evolution across the input dynamic range and indicates that the acquisition and conversion chain preserves the expected monotonic transfer characteristic throughout the scan.

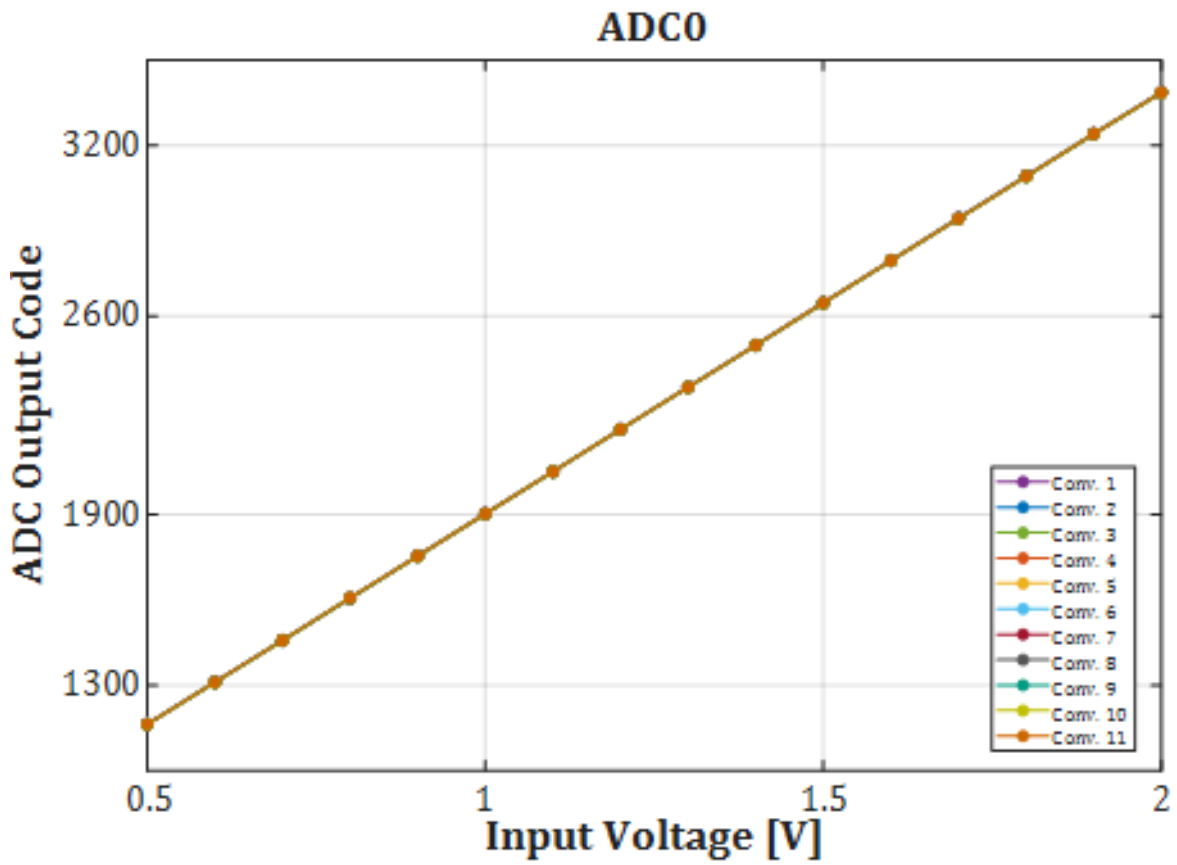

Figure 4.5: Measured static transfer characteristics of ADC0 for all the conversions performed during a complete scan.

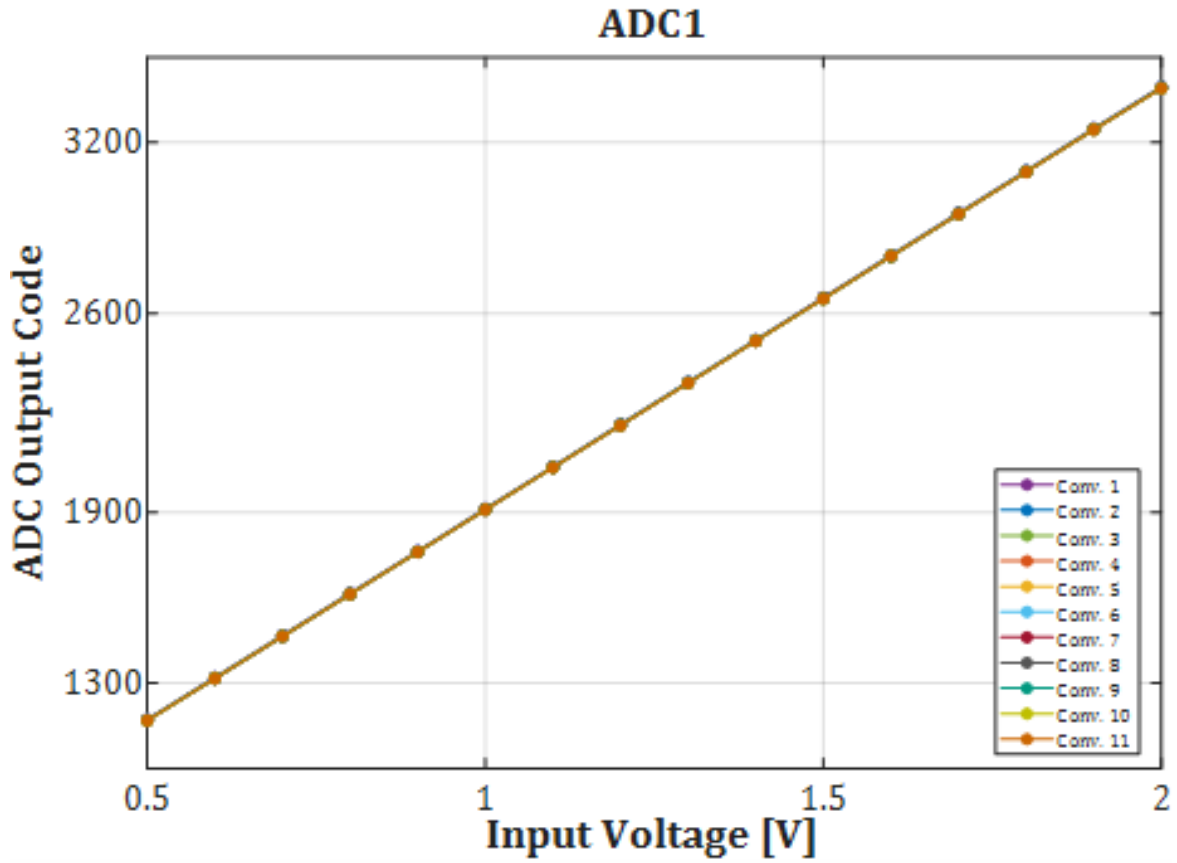

Figure 4.6: Measured static transfer characteristics of ADC1 for all the conversions performed during a complete scan.

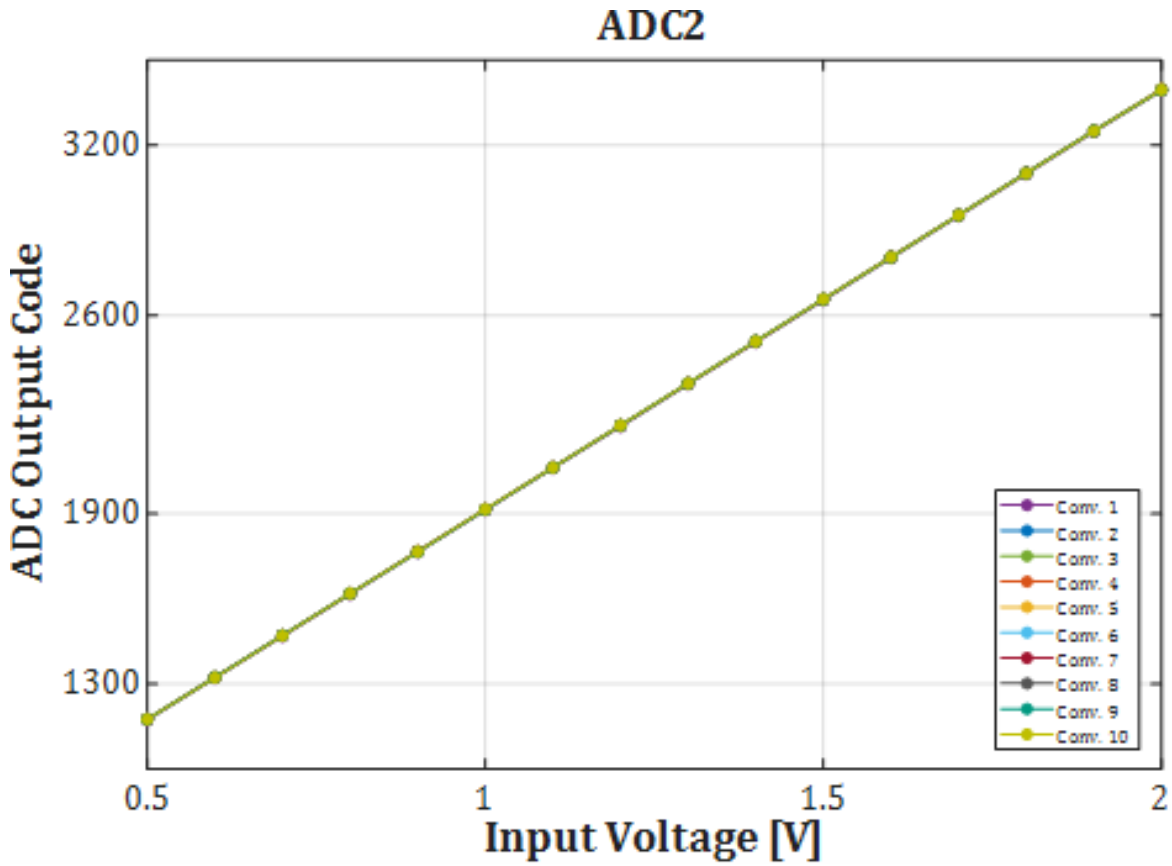

Figure 4.7: Measured static transfer characteristics of ADC2 for all the conversions performed during a complete scan.

Error with Respect to the Ideal Transfer Characteristic

The corresponding error plots are reported in Figures 4.8–4.10. These graphs show the deviation between the measured transfer characteristic and the ideal one, with the error expressed in bits. Considering that the maximum explored dynamic range corresponds to about 12.15 bits, while the converted output word is represented on 13 bits, a code variation within approximately ±2 LSB can be regarded as compatible with the 11-bit design target, which includes the combined contribution of noise and non-linearity. From this perspective, the measured deviations remain consistent with the expected static performance of the converter and confirm correct ADC behavior over the full scan sequence.

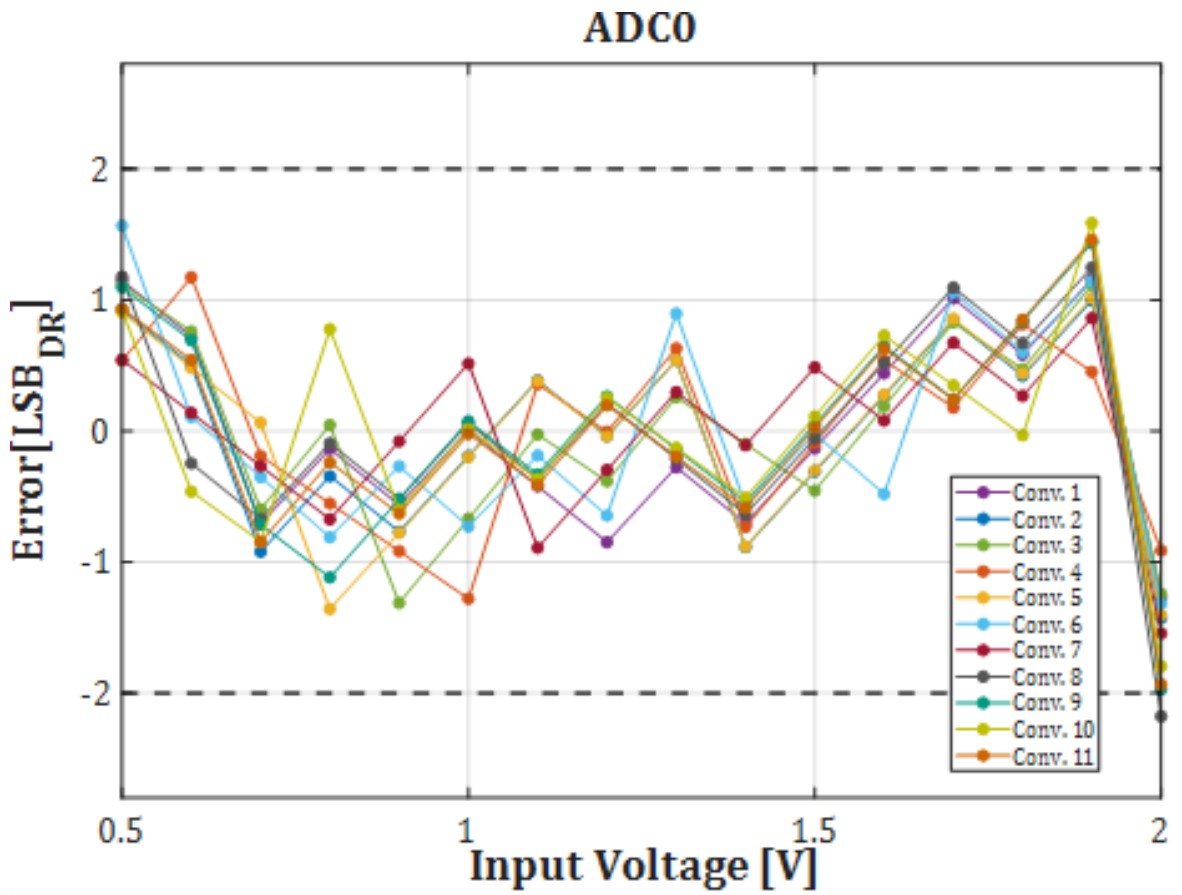

Figure 4.8: Measured error, expressed in LSB referred to the explored dynamic range, for ADC0 over all the conversions of a complete scan.

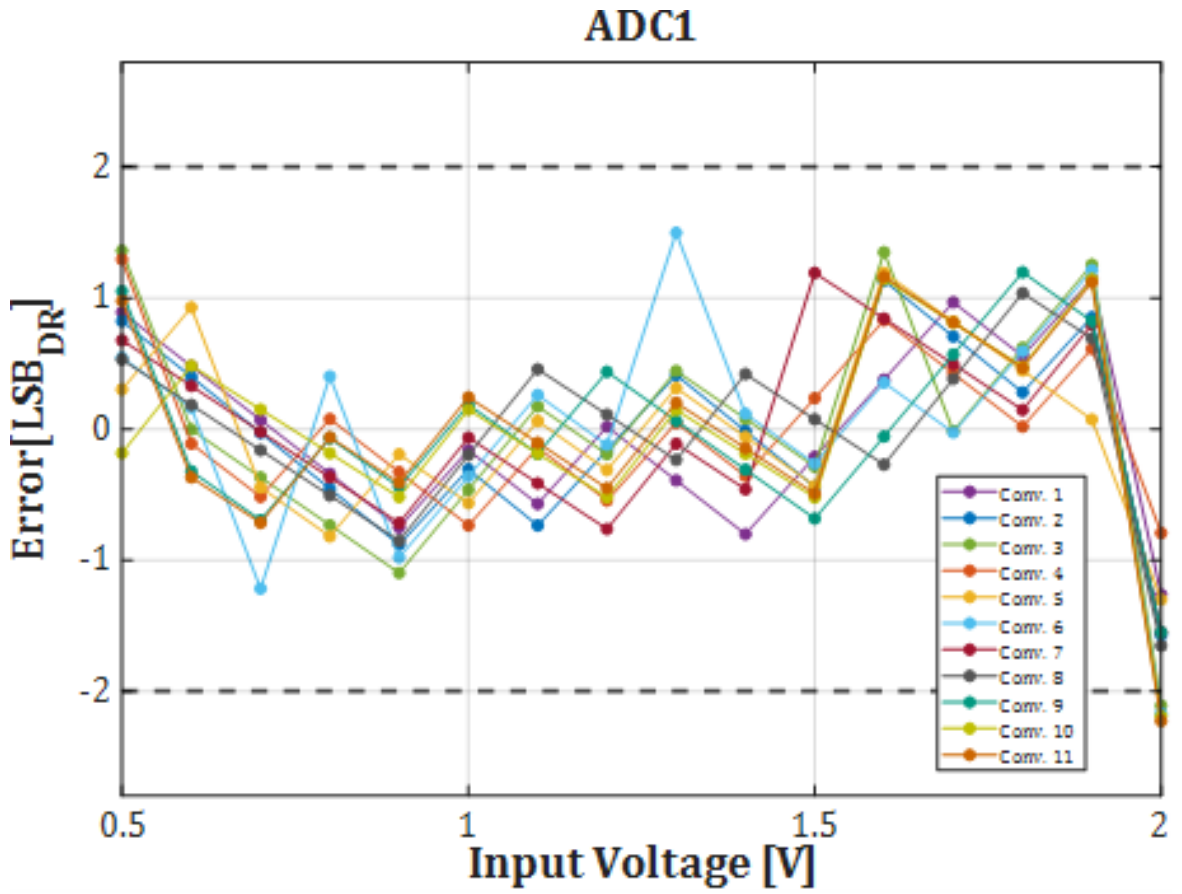

Figure 4.9: Measured error, expressed in LSB referred to the explored dynamic range, for ADC1 over all the conversions of a complete scan.

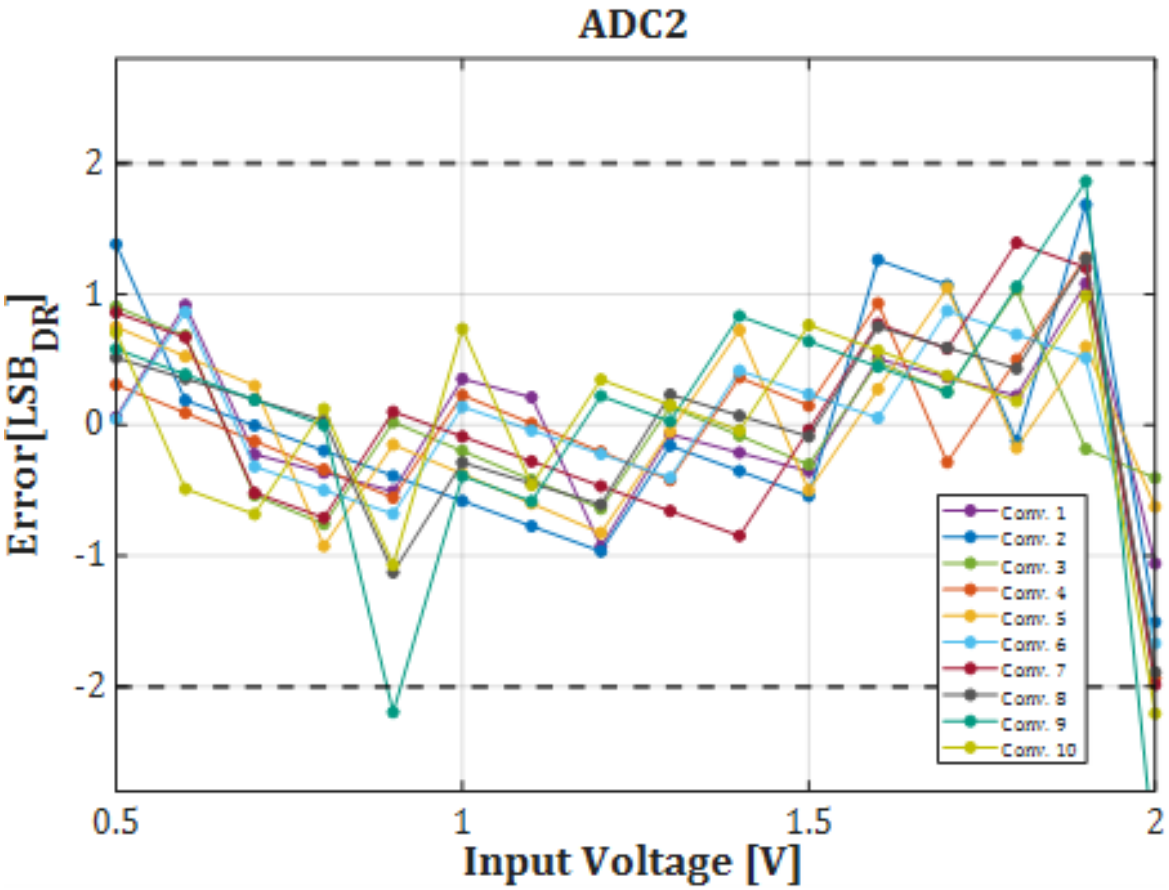

Figure 4.10: Measured error, expressed in LSB referred to the explored dynamic range, for ADC2 over all the conversions of a complete scan.

ENOB_DR

A more compact representation of the effective conversion quality is provided by the ENOB_DR parameter, whose trend for the three ADCs is reported in Figure 4.11. In this case, each curve represents the effective resolution associated with one ADC as a function of the conversion index. The parameter was derived from the root-mean-square error of each conversion set according to

$$\mathrm{ENOB_{DR}} = \log_2\left(\frac{COD_{\max}}{2 \cdot RMSE}\right)$$

where $COD_{\max} = 4560$ and $RMSE$ is the root-mean-square error extracted from the measured transfer characteristic. As shown in Figure 4.11, all the obtained values remain above 11 bits over the complete scan. This confirms that the expected effective resolution is preserved throughout the entire acquisition sequence and that no significant degradation is introduced by the multiplexed conversion scheme.

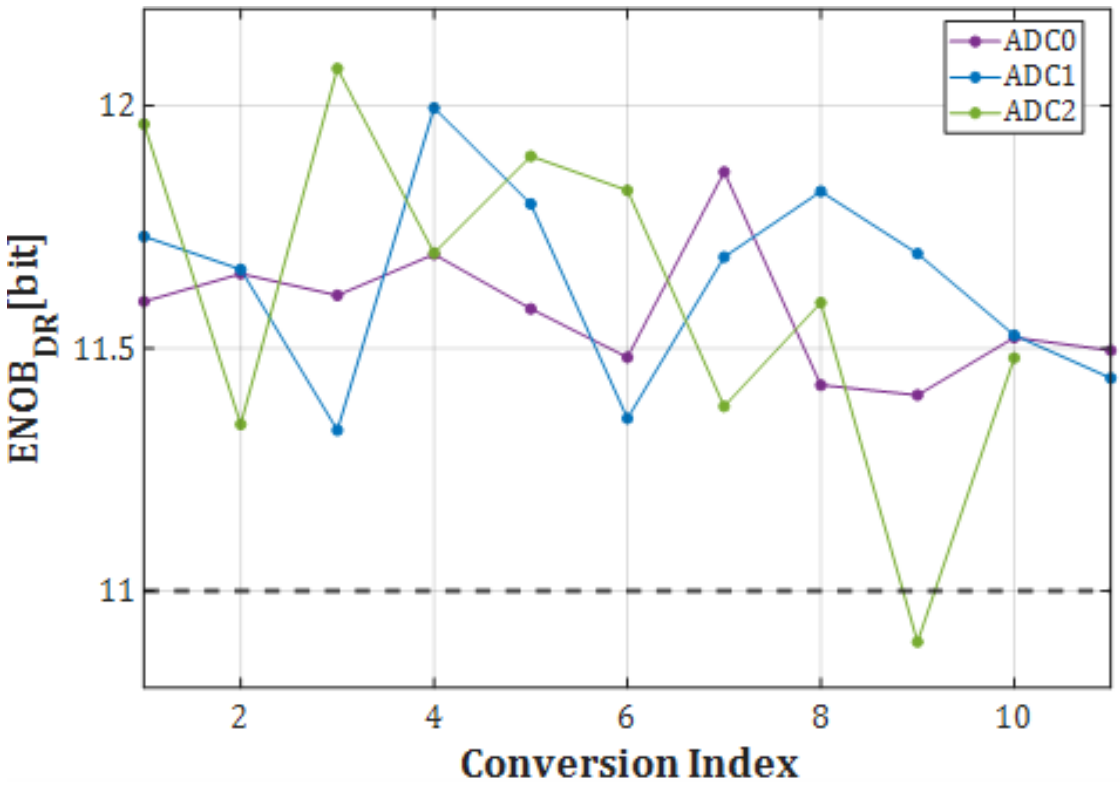

Figure 4.11: ENOB_DR trend versus conversion index for the three ADCs involved in the complete scan. The dashed line indicates the minimum required resolution of 11 bits.

Mean ENOB_DR

In order to provide a more global view of the converter behavior, Figure 4.12 reports the mean ENOB_DR, obtained by averaging the root-mean-square errors associated with the corresponding conversion positions of the three ADCs and then converting the resulting value into effective resolution. Also in this case, the extracted trend remains consistently above the minimum required specification. This confirms that, when the three ADCs are considered together as a complete conversion system, the overall quality of the conversion remains compliant with the target resolution and does not exhibit critical degradation along the scan.

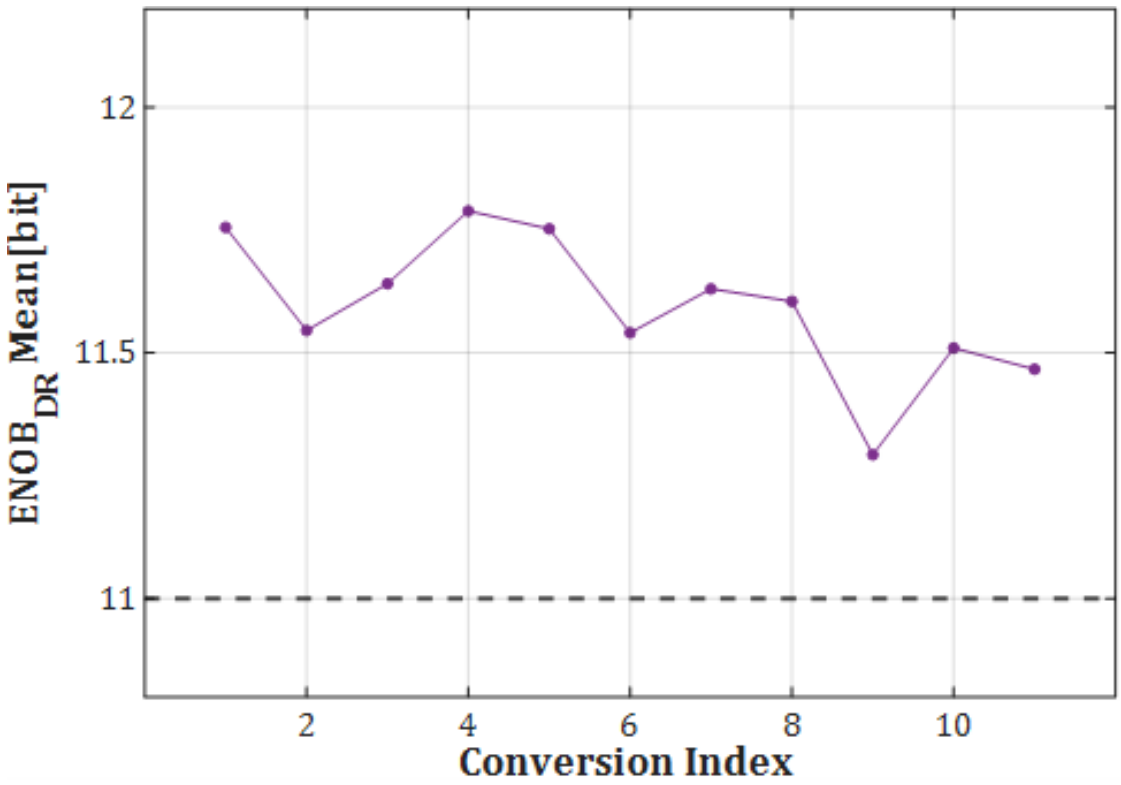

Figure 4.12: Mean ENOB_DR as a function of the conversion index, obtained from the average behavior of the three ADCs. The dashed line marks the 11-bit target specification.

Static Power Consumption

The last set of results concerns the power consumption measured under static quiescent and static operative conditions. For the static quiescent condition, the absorbed current was measured with the chip powered on and with the external operating conditions already applied, namely supply voltages, clock, and input signal, but without asserting TRIGGER<0>. Under these conditions, the measured power consumption was equal to 12.5 µW per channel. For the static operative condition, the absorbed current was instead evaluated during the active conversion interval, namely between the rising edge of TRIGGER<0> and the instant immediately before the rising edge of LAM_S<0>, corresponding to the time window in which the chip is effectively performing the conversion. In this case, the measured static operative power consumption was equal to 160 µW per channel. This relatively high on-duty value is required to guarantee high linearity and resolution, corresponding to an average THD of about 0.02%, and it also includes the power drawn by the internal reference-voltage buffers, which are necessary to suppress bonding-related ringing during switched-capacitor operation. It is worth noting that, once the active conversion phase is completed, the chip returns to the static quiescent condition only after the application of either a RESET signal or a RES_ACQ<0> signal.

Final Remarks on the Present Measurements

Because of the delayed delivery of the fabricated chip, only a preliminary static characterization of the ASIC could be completed within the available time. Moreover, the measurements were performed with a 5 MHz clock rather than at the nominal higher frequency, due to the signal-integrity limitations discussed previously. In the next stage of the activity, a more complete characterization will be carried out, including dynamic measurements and operation at higher clock frequency after resolution of the reflection issue between the signal generator and the chip input path.

Chapter 5

Conclusions

The first measurement results confirm correct static operation of the LEMX-DC, linear behavior over the full useful input range, and an ENOB_DR that remains above the 11-bit target throughout the complete scan. Even within the constraints of a preliminary campaign, these observations validate the robustness of the adopted architecture under representative operating conditions and show that the converter meets its main static specifications with the available laboratory setup.

An important outcome of this work is that the dedicated characterization platform has enabled a structured transition from design assumptions to real silicon measurements. The board provided stable biasing conditions, accessible observation points, and sufficient digital control flexibility to perform a repeatable acquisition and readout flow on the bonded channel. In this sense, the thesis objective was achieved not only through PCB realization, but also through the first successful use of that platform for ASIC validation.

At the same time, the campaign highlighted the main limitation of the current setup, namely the signal-integrity issue observed on the clock path at the nominal operating frequency. For this reason, the preliminary measurements were carried out with a 5 MHz clock, corresponding to a full scan duration of about 250 µs instead of the nominal 80 µs. The obtained results nevertheless confirm that the specifications are met under these conditions and provide a solid baseline for the next experimental phase.

Future work will therefore focus on completing the dynamic characterization, extending the measurements to higher clock rates after the impedance-matching issue is corrected, and broadening the validation to additional operating modes and channels. The present platform is already suitable for this continuation and can support a more exhaustive experimental campaign in the next stage of the project.

Bibliography

[1] "Progetto EMM - Earth-Moon-Mars," https://pnrr.inaf.it/progetto-emm/, 2025, accesso: giugno 2025.

[2] "Capitolato Tecnico - Progettazione dell'ASIC DC per LEM-X," INAF - Istituto di Astrofisica e Planetologia Spaziali, Tech. Rep. Prot. n. 3141, 2023, capitolato tecnico, documento ufficiale della gara.

[3] "Proposta Tecnica - Progettazione dell'ASIC DC per LEM-X," INAF - Istituto di Astrofisica e Planetologia Spaziali, Tech. Rep. EMM-INAF-B-0004, 2023, procedura negoziata per il progetto LEM-X.

[4] F. Mele, "LEM-X ASIC FE - Internal Design Report," INAF - Istituto di Astrofisica e Planetologia Spaziali, Tech. Rep., 2024, versione preliminare, EMM Project.

[5] F. Mele, I. Dedolli, and G. Bertuccio, "A CMOS Peak Stretcher/Peak Detector for Wide Dynamic Range Spectroscopy Applications With 32-uW Power Consumption," *IEEE Solid-State Circuits Letters*, vol. 5, pp. 74–77, 2022.

[6] P. Malcovati, M. Grassi, and M. Tambussi, "LEMX DC RA1 - Internal Technical Document," Università degli Studi di Pavia, Tech. Rep., 2024, aggiornamento Gennaio 2024, V2.

[7] P. Malcovati, M. Grassi, M. Tambussi, and J. Giani, "LEMX DC RA2 - Internal Technical Document," Università degli Studi di Pavia, Tech. Rep., 2025, aggiornamento Febbraio 2025, V6.

[8] M. Tambussi and J. Giani, "LEMX DC ASIC Internal Design Report," Università degli Studi di Pavia, Tech. Rep., 2025, revision checked by M. Grassi and P. Malcovati.

[9] Z. Tan, C.-H. Chen, Y. Chae, and G. C. Temes, "Incremental Delta-Sigma ADCs: A Tutorial Review," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 12, pp. 4161–4173, 2020.

[10] J. Márkus, J. Silva, and G. C. Temes, "Theory and Applications of Incremental Delta-Sigma Converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 4, pp. 678–690, 2004.

[11] S. Pavan, R. Schreier, and G. C. Temes, *Understanding Delta-Sigma Data Converters*, 2nd ed. IEEE Press and Wiley, 2017.

[12] M. Grassi and P. Malcovati, "A Robust and Versatile Analog-to-Digital Converter for Space Exploration Spectroscopy on Satellites," in *Proceedings of RSTI Workshop*, 2023, abstract PDF available from internal documentation.

[13] Tektronix, “XYZs of Signal Generators,” https://download.tek.com/document/76W_16672_7_XYZ-Signal-Gen_PR.pdf, 2016, accessed: 2026-04-09.

[14] Keysight Technologies, “Considerations for Buying a Bench Power Supply,” https://www.keysight.com/us/en/assets/7018-01411/application-notes/5989-5278.pdf, 2010, application note, accessed: 2026-04-09.

[15] Fluke, “What is a Digital Multimeter?” https://www.fluke.com/en/learn/blog/electrical/what-is-a-digital-multimeter, 2026, accessed: 2026-04-09.

[16] *TLA5000 Series Logic Analyzers: TLA5201, TLA5202, TLA5203, TLA5204*, Tektronix, 2004, datasheet provided with the thesis material.

[17] *Tektronix Logic Analyzer Family Quick Start User Manual*, Tektronix, 2004, manual provided with the thesis material.

[18] Digilent, “Digital Discovery Reference Manual,” https://digilent.com/reference/test-and-measurement/digital-discovery/reference-manual, 2026, accessed: 2026-04-09.

[19] ——, “Digital Discovery Specifications,” https://digilent.com/reference/test-and-measurement/digital-discovery/specifications, 2026, accessed: 2026-04-09.

[20] Tektronix, “Oscilloscope Basics,” https://www.tek.com/en/documents/primer/oscilloscope-basics, 2026, accessed: 2026-04-09.

[21] ——, “Evaluating Oscilloscopes,” https://www.tek.com/en/documents/primer/evaluating-oscilloscopes, 2026, accessed: 2026-04-09.