

UNIVERSITÀ
DI PAVIA

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Department of Electrical, Computer and
Biomedical Engineering

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Analog Design Optimization and Digital-Assisted Offset Compensation for Thermal Drift Reduction in a Precision Error Amplifier

Advisors: Profs. Edoardo Bonizzoni and Piero Malcovati

Co-Advisor: Prof. Elisabetta Moisello

Supervisor: Stefano Beria

Co-Supervisor: Salviano Marino

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Raul Mattia Avram

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Abstract

Precision analog systems often require stringent requirements on voltage accuracy and thermal stability, as these parameters directly impact overall system performance. This thesis investigates two different approaches for improving the accuracy and temperature-drift performance of a precision error amplifier and provides a comparative assessment of their effectiveness.

The first approach focuses on transistor-level optimization of the amplifier itself. Through systematic analysis of device dimensions, mismatch sensitivity, frequency response, and temperature behavior, several design modifications are introduced to reduce the intrinsic offset voltage and its thermal drift while preserving the original circuit architecture. The impact of these changes is evaluated through extensive simulations, including Monte Carlo analyses.

The second approach explores a digitally-assisted offset compensation technique based on a mixed-signal calibration loop. The proposed architecture employs a SAR ADC, an R-2R DAC, and custom digital trimming logic implemented in Verilog to estimate and compensate the amplifier offset by generating an appropriate correction voltage. The design and operation of the calibration loop are investigated with particular attention to convergence behavior, stability, quantization effects, and analog-to-digital interface considerations.

The two approaches are developed independently and compared in terms of offset reduction capability, thermal stability, implementation complexity, hardware overhead, and design trade-offs. Simulation results demonstrate that both techniques can significantly improve the overall accuracy of the system, although through fundamentally different mechanisms. The comparison highlights the benefits and limitations of intrinsic analog optimization versus digital-assisted calibration, providing useful design guidelines for the development of high-precision analog and mixed-signal integrated circuits.

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Introduction

0.1 DC-DC Converters

Every electronic system requires a power supply. As semiconductor technology continues to evolve and increasingly complex functionalities are integrated into a single device, power management has become a key aspect of modern electronic systems. It directly impacts system size through power density, overall performance through efficiency and power distribution, and obviously the total system cost.

Power converters [1] can be broadly classified into two categories:

- **Linear converters**, where power is continuously transferred from the source to the load and the regulating devices operate in the linear region.
- **Switching converters**, where power is transferred in discrete packets of energy and the power devices periodically switch between ON and OFF states.

The fundamental building block of modern power conversion systems is the switching converter. In these circuits, a control signal determines how the input power is processed in order to provide a regulated output voltage or current. Several classes of switching converters exist, including DC-DC, AC-DC, and DC-AC converters.

The focus of this work is on DC-DC converters, where a DC input voltage is converted into a DC output voltage with either higher or lower magnitude. Depending on the topology, the output voltage may also have opposite polarity or be galvanically isolated from the input. High power efficiency is a fundamental requirement in power conversion applications. A highly efficient converter dissipates less power, resulting in reduced thermal stress, smaller cooling requirements, and higher power density. Consequently, the overall converter size and weight can be significantly reduced.

Capacitors and magnetic components [1] [2] are fundamental elements in switching converters because, ideally, they do not dissipate power. Conversely, resistive elements and semiconductor devices operating in the linear region introduce losses and should be minimized whenever possible. The

main advantage of switched-mode operation lies in the operating principle of the power transistors. When used as switches, transistors alternate between the ON and OFF states. In the OFF state, only a small leakage current flows, while in the ON state the voltage drop across the device is ideally very low. As a result, the power dissipated by the switching devices is significantly lower than in linear regulators, leading to substantially higher conversion efficiency.

0.2 Buck Converter Fundamentals

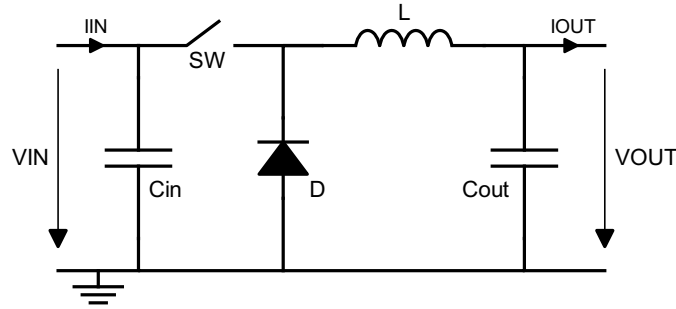


Figure 1: Basic Buck converter topology.

A buck converter [3] is a switched-mode DC-DC power converter designed to step down an input voltage to a lower regulated output voltage with high efficiency. Compared to linear regulators, buck converters achieve significantly higher efficiency by employing switching devices that operate primarily in either the fully ON or fully OFF state, minimizing power dissipation.

The basic buck converter [Fig. 1] consists of a power switch, a diode (or a synchronous MOSFET), an inductor and an output capacitor. During operation, the power switch is periodically turned ON and OFF. While the switch is ON, energy is stored in the inductor; when the switch is OFF, the stored energy is transferred to the load while maintaining current flow through the inductor. Assuming ideal components and Continuous Conduction Mode (CCM) operation, the output voltage is directly related to the input voltage through the duty cycle D according to

$$V_{OUT} = D \cdot V_{IN}$$

Therefore, by adjusting the duty cycle, the converter can regulate the output voltage despite variations in the input supply voltage or load conditions.

To guarantee accurate voltage regulation, buck converters employ a closed-loop feedback system. The output voltage is sensed directly or through a resistor divider and compared against a reference voltage by the error amplifier and the resulting error signal is subsequently processed by the

compensation network and the Pulse Width Modulation (PWM) controller, which adjusts the duty cycle of the power stage. As a result, both the regulation accuracy and the dynamic performance of the converter strongly depend on the characteristics of the feedback loop.

Among the feedback-loop building blocks, the error amplifier plays a fundamental role. Its offset voltage directly translates into a systematic deviation of the regulated output voltage, while temperature-dependent variations introduce additional inaccuracies across the operating temperature range. Minimizing both the offset and its temperature drift is essential for achieving high regulation accuracy.

For this reason, the optimization of the error amplifier offset and thermal stability represents the primary focus of this work.

0.3 Control Loop Architectures

A control loop [1] is a system designed to regulate a specific variable by continuously comparing its measured value with a desired reference. The difference between the reference and the measured quantity, commonly referred to as the error signal, is processed by a controller in order to adjust the system behaviour and reduce the regulation error.

Several control techniques have been developed for switching DC-DC converters to achieve voltage regulation under varying operating conditions. These techniques can be classified into variable-frequency control and fixed-frequency control architectures.

In variable-frequency control architectures, the switching frequency is not fixed but varies according to the converter operating conditions. The switching action is directly determined by the behavior of the output voltage or current, resulting in fast transient response and relatively simple implementations. One of the most common variable-frequency techniques is hysteretic control. In this architecture, the output voltage is continuously monitored and compared against predefined upper and lower thresholds around the desired value. When the output voltage exceeds one threshold, the power switch changes state, causing the voltage to move toward the opposite threshold. Another widely adopted approach is the constant ON-time (COT) or constant OFF-time control technique. In these architectures, either the ON-time or the OFF-time of the power switch is kept fixed, while the complementary interval varies according to operating conditions.

Fixed-frequency controllers maintain a constant switching frequency regardless of load conditions. This characteristic simplifies filter design, facilitates EMI control, and makes these architectures particularly attractive for integrated power management solutions. The simplest fixed-frequency approach is Voltage-Mode Control (VMC). In this architecture, the output voltage is sensed through a feedback network and compared with a refer-

ence voltage. The resulting error signal is processed by an error amplifier and compared with a periodic ramp waveform to generate the PWM duty cycle. To improve dynamic performance, many modern converters employ Current-Mode Control (CMC) [4]. In addition to the outer voltage loop, an inner current loop is introduced by sensing the inductor current. The voltage loop generates a reference current, while the current loop directly controls the power stage. As a result, the converter exhibits faster transient response, simplified compensation, and improved line regulation.

Variable-frequency architectures generally provide superior transient response and simplified control structures, but at the expense of varying switching frequency and potentially higher EMI complexity. Fixed-frequency architectures, on the other hand, offer predictable spectral characteristics and easier system integration, making them the preferred choice in many commercial power management applications.

Among fixed-frequency techniques, voltage-mode control is characterized by its simplicity, whereas current-mode control achieves improved dynamic performance through the addition of an inner current-feedback loop. The choice of control architecture depends on the specific requirements of the application, including regulation accuracy, transient performance, efficiency, implementation complexity, and noise constraints.

0.4 Role of the Error Amplifier

The error amplifier is a key block of a current-mode controlled converter [Fig. 2]. Its purpose is to compare the feedback voltage V_{FB} , derived directly from the output voltage or through a resistor divider, with a reference voltage ' V_{REF} '. The resulting error signal is then used to generate the current reference for the inner current-control loop.

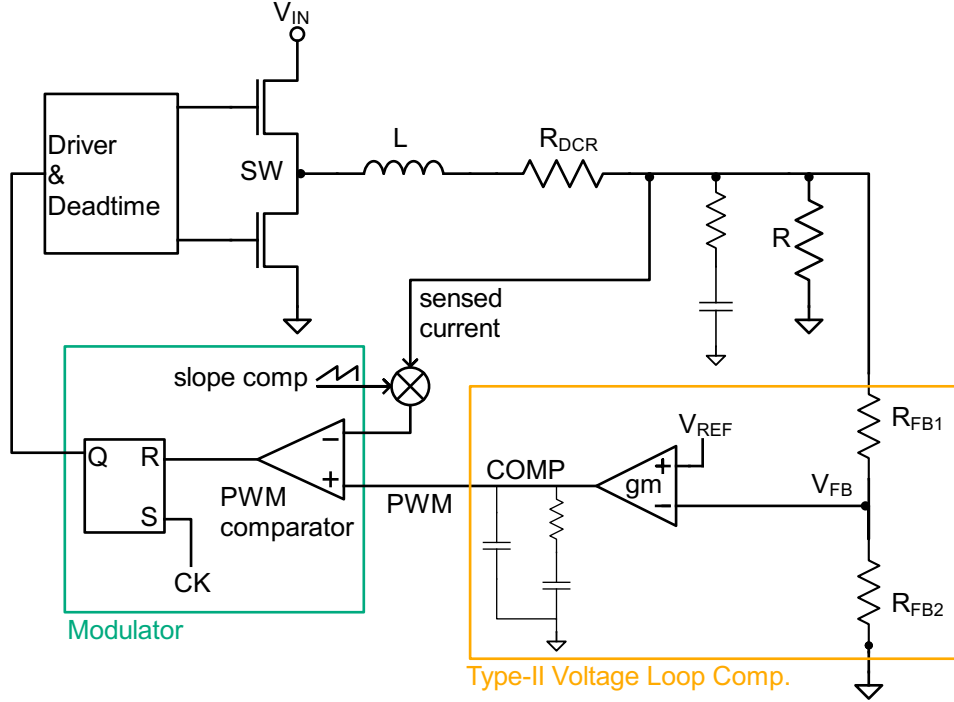


Figure 2: Peak current mode controlled Buck converter topology.

By continuously monitoring the difference between V_{FB} and V_{REF} , the error amplifier enables the outer voltage loop to regulate the output voltage despite variations in load current, input voltage, and operating conditions. Together with the compensation network, it also contributes to the overall stability and dynamic behavior of the converter.

Since the output voltage is regulated by forcing V_{FB} to match V_{REF} , any offset voltage present in the error amplifier directly translates into a regulation error. Similarly, temperature-dependent variations can lead to output voltage drift over temperature. For this reason, the offset and thermal performance of the error amplifier are critical parameters in precision power management applications.

0.5 Thesis Objectives

Modern automotive applications such as ADAS, camera-based sensing systems, radar modules and centralized domain controllers require highly reliable power-management solutions capable of maintaining accurate output voltages over a wide operating temperature range. The increasing demand for precise sensing, monitoring and processing capabilities has progressively reduced the margin available for power-supply-induced errors, making voltage accuracy and thermal stability critical design objectives. For this reason,

improving the regulation accuracy of switching converters remains an active area of research in modern automotive electronics.

The converter considered in this work already achieves an output-voltage accuracy of $\pm 0.8\%$, which is comparable to that of state-of-the-art automotive power-management devices [5]. However, the continuous evolution of automotive systems toward higher levels of sensing, processing and functional integration is driving research efforts toward further reductions of the error contributions associated with voltage regulation. Increasing the available accuracy margin enables greater robustness against load transients and temperature variations while facilitating the adoption of future high-precision automotive electronic systems. [6]

The accuracy of a buck converter is strongly influenced by the performance of its feedback loop, particularly by the characteristics of the error amplifier. Input offset voltage and temperature drift introduce deviations between the actual and the desired output voltage, limiting the achievable regulation accuracy.

The objective of this thesis is to investigate two different approaches to mitigate these effects. The first approach focuses on transistor-level optimization of the error amplifier to reduce its intrinsic offset and temperature coefficient. The second approach explores a digitally-assisted calibration technique based on ADC and DAC blocks to compensate for the offset through a dedicated servo loop that does not affect the loop dynamics. Finally, the two solutions are compared in terms of offset reduction, thermal stability, implementation complexity, and design trade-offs.

Chapter 1

Offset and Thermal Drift Analysis in the Voltage Loop

1.1 Architecture

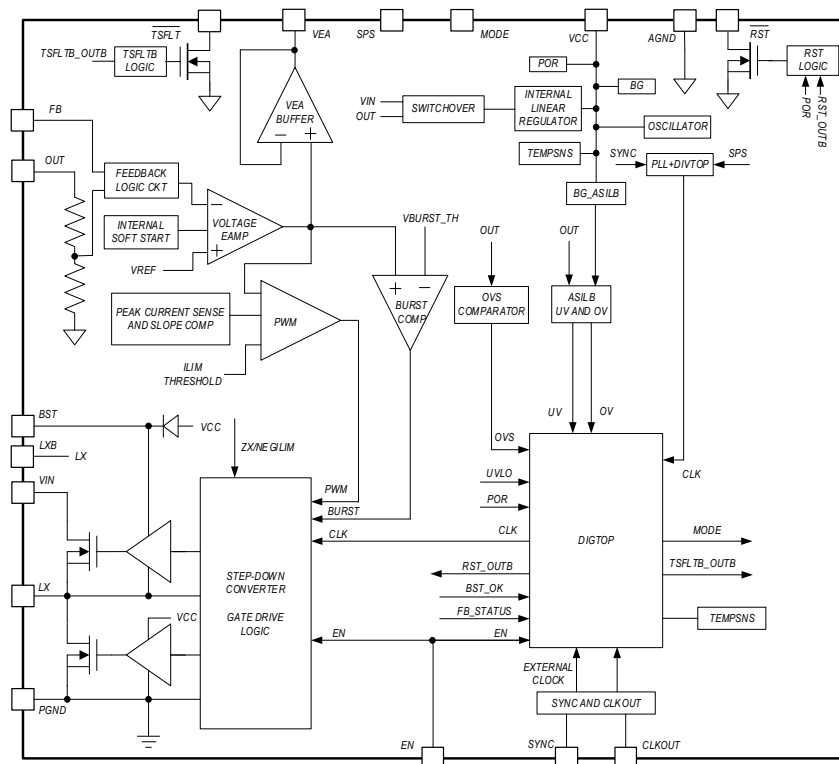


Figure 1.1: System architecture of the 'ARM' Buck converter. [image from the ADI product datasheet]

Fig. 1.1 shows the architecture of a synchronous buck converter, hereafter referred to as "ARM", with internal high-side and low-side switches featuring Silent Switcher architecture designed to minimize EMI emissions while delivering high efficiency at high switching frequencies. The ICs deliver up to 18A with input voltages from 3.0V to 36V.

The converter is available with either adjustable or fixed output voltage options and it has four selectable switching frequencies: [200 kHz - 400 kHz - 1 MHz - 2.1 MHz].

The first stage of this work focuses on the analysis of the blocks forming the voltage loop, with particular attention to offset and thermal drift. The complete signal chain is visible in Fig. 1.1, and each block of the OUT-REF path is analyzed separately to evaluate its individual contribution. The main goal is to identify the dominant sources of temperature-dependent offset drift in the voltage loop and to improve the converter performance across the standard automotive temperature range of -40°C to 150°C .

The analysis is carried out through Monte Carlo simulations performed at three different temperatures, namely -40°C , room temperature, and 150°C , using a total of 600 simulation samples.

1.2 Resistor Divider Analysis

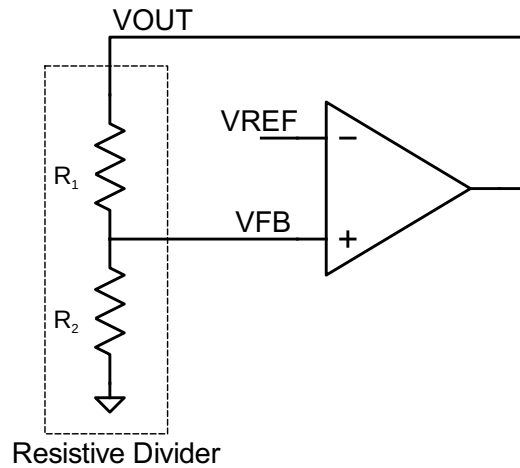


Figure 1.2: ARM resistive divider buffer configuration.

The first block under investigation is the resistor divider, which is used to scale down the output voltage in order to generate a signal comparable with the reference voltage employed by the subsequent error amplifier stage. To evaluate its contribution, the resistor divider is isolated from the rest of

the circuit and configured in a buffer setup using an ideal voltage-controlled voltage source (VCVS) with a very high gain, as shown in Fig. 1.2. Assuming a nominal output voltage of 3.3 V (all the simulations in this thesis will be conducted with a desired V_{OUT} equal to 3.3 V), the corresponding reference voltage is equal to 412.5 mV considering the x8 factor of the resistive divider.

The results reported in Table 1.1 show an output offset standard deviation of approximately 3.5 mV, which represents nearly 0.1% of the nominal 3.3 V output voltage. Moreover, the variation across the considered temperature range is almost negligible, indicating that the resistor divider exhibits a virtually temperature-independent offset behavior; on top of that, the final output-trimming procedure performed by the test engineer during production testing can compensate for most of this static contribution, leaving a negligible residual error.

Test	Min	Max	Mean	Std Dev
OFFSET	-9.608m	10.57m	467.9u	3.57m
-40 °C	-9.573m	10.31m	387.9u	3.57m
27 °C	-9.608m	10.28m	355.7u	3.57m
150 °C	-9.31m	10.57m	660u	3.568m

Table 1.1: Resistive divider offset MonteCarlo simulation results, 200 runs for each temperature. [values referred to V_{OUT}]

The behavior was expected, since the output voltage depends primarily on the ratio between the resistors rather than on their absolute values. As both resistors are implemented using the same resistor type and share similar temperature coefficients, first-order temperature variations cancel out, resulting in a nearly temperature-independent division ratio. Residual drift is mainly caused by resistor mismatch, non-ideal thermal tracking, and higher-order temperature effects, and is generally much smaller than the drift introduced by the reference voltage and the error amplifier offset.

1.3 Buffer Analysis

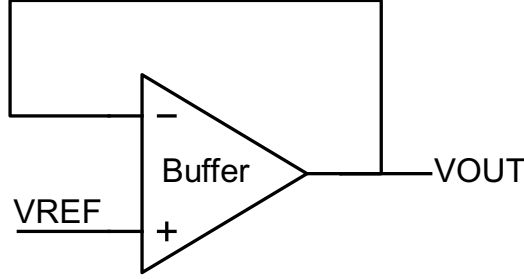


Figure 1.3: ARM Buffer configuration.

The next analyzed block is the Buffer [Fig. 1.3] used in the reference voltage generation path of the error amplifier. Applying the same methodology adopted for the resistor divider, a standard deviation of approximately 650 μV is obtained, as reported in Table 1.2. When referred to the converter output through the divider scaling factor of 8 ($3.3 \text{ V} / 0.4125 \text{ V}$), this corresponds to an output-referred offset of about 5.2 mV (8 times 650 μV), which is equivalent to approximately 0.16% of the nominal output voltage. As observed for the resistor divider, the offset variation with temperature is practically negligible, indicating that the contribution of this block remains substantially constant over the entire operating temperature range.

Test	Min	Max	Mean	Std Dev
OFFSET	-1.959m	1.904m	-1.223u	706.8u
-40 °C	-1.65m	1.714m	-1.327u	638.7u
27 °C	-1.677m	1.735m	-2.683u	643.5u
150 °C	-1.66m	1.742m	-7.842u	648.8u

Table 1.2: Buffer offset MonteCarlo simulation results, 200 runs for each temperature.

1.4 Error Amplifier Analysis

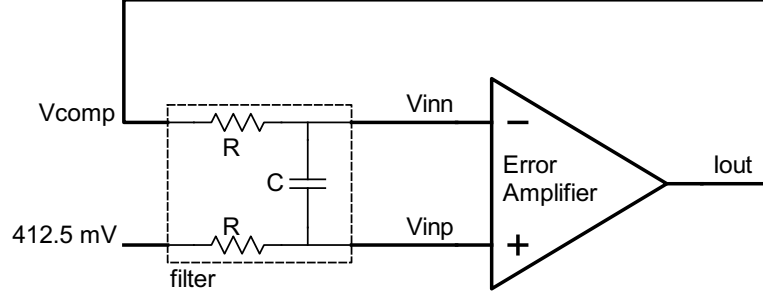


Figure 1.4: ARM error amplifier configuration.

Finally, the transconductance stage [Fig. 1.4], namely the error amplifier itself, is investigated. Using the same analysis procedure, the results reported in Table 1.3 are obtained. In this case, a significant difference can be observed among the various temperature conditions as shown in Fig. 1.5. In particular, starting from an offset standard deviation of 3.38 mV at room temperature, at -40°C the offset standard deviation reaches approximately 3.6 mV. Referred to the converter output through the divider factor of 8, this value corresponds to about 29.3 mV, which represents nearly 0.9% of the nominal 3.3 V output voltage. Meanwhile, at 150°C , the offset standard deviation reaches 3.076 mV, which corresponds to 24.6 mV referred to V_{OUT} , or 0.745% of the nominal output voltage.

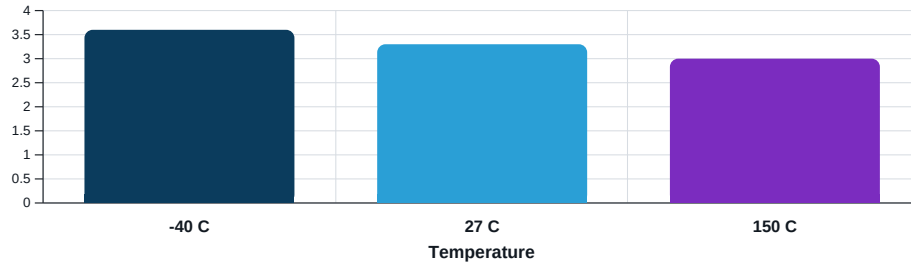


Figure 1.5: Error amplifier offset temperature drift.

These results indicate that the error amplifier is the dominant temperature-dependent offset contributor to the analyzed voltage loop. Moreover, a temperature-induced variation of almost 600 μV over the full temperature range can be observed in Table 1.3. When referred to the converter output, this corresponds to an offset drift of approximately 0.145%, which cannot be considered negligible for a high-performance automotive-oriented design.

Consequently, the error amplifier emerges as the primary target for the optimization techniques presented in the following chapters.

Test	Min	Max	Mean	Std Dev
OFFSET	-8.932m	10.68m	59.2u	3.673m
-40 °C	-8.932m	10.68m	82.49u	3.673m
27 °C	-7.956m	9.492m	75.23u	3.381m
150 °C	-6.91m	8.199m	93.16u	3.076m

Table 1.3: Error amplifier offset MonteCarlo simulation results, 200 runs for each temperature.

1.5 Contribution Comparison

Fig. 1.6 illustrates the contribution of each block to the overall offset as a function of temperature. Since both the resistor divider and the buffer exhibit a negligible temperature dependence of the offset, their contribution can be considered substantially constant across the entire operating temperature range. For this reason, the main objective of this work is to reduce the temperature drift of the voltage loop offset by focusing the analysis and optimization on the transconductance stage, which represents the dominant temperature-dependent contribution; in fact, the device typically undergoes an offset-trimming procedure which takes place only at room temperature, so the main focus is therefore the behavior when the temperature drifts from the trimmed case.

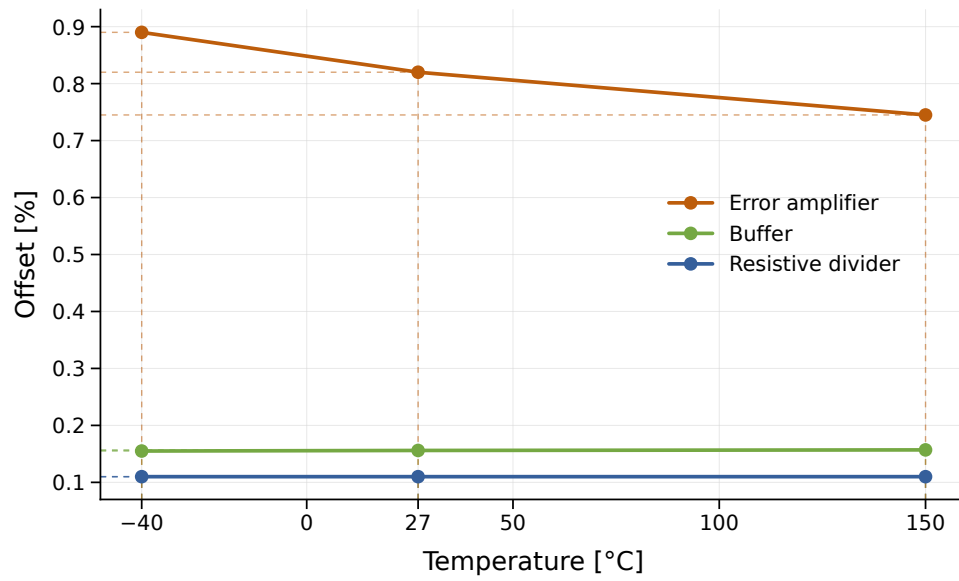


Figure 1.6: Offset temperature drift comparison [red: error amplifier, green: buffer, blue: resistive divider]

1.6 SIMPLIS Model

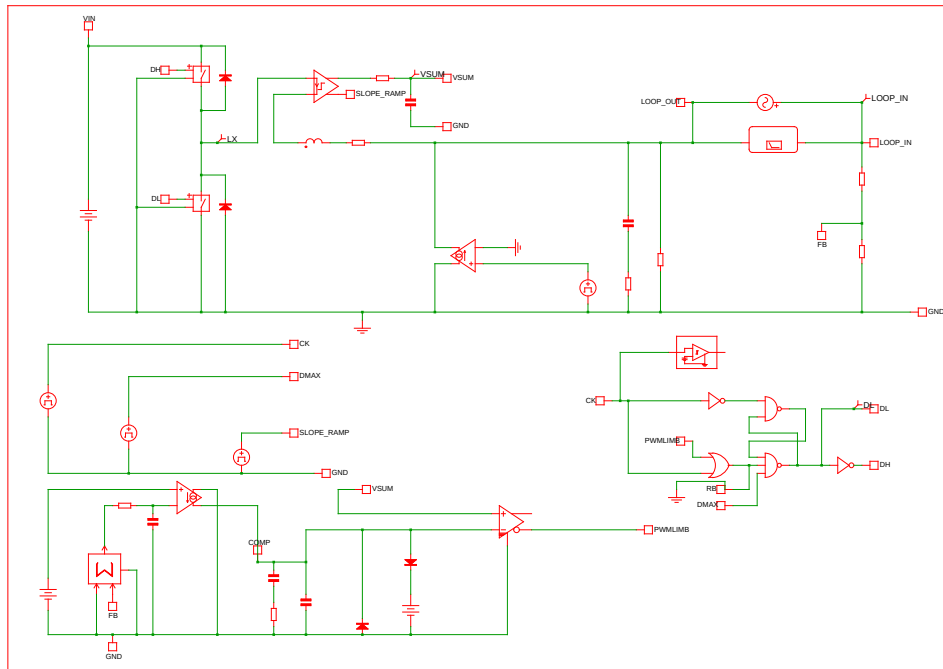


Figure 1.7: Simplified Buck converter SIMPLIS model.

For the preliminary investigation of new design solutions, a simplified converter model has been implemented in SIMPLIS. The objective of this approach is to provide a fast and intuitive environment for studying the general behavior of feedback-controlled switching converters. By reducing the complexity of the system, SIMPLIS allows a rapid evaluation of the effects introduced by poles and zeros on the loop stability and dynamic response, avoiding the computational cost associated with full transistor-level simulations.

The developed model in Figure 1.7 is therefore used as a theoretical framework to investigate how variations in the compensation network or in the characteristics of the error amplifier can affect bandwidth, phase margin, and overall loop stability. Such an analysis is directly relevant to the present work since any modification introduced to reduce the amplifier offset temperature drift may also alter the frequency response of the control loop.

The model operates at a switching frequency of 400 kHz, as shown in Fig. 1.8; This choice simplifies the initial investigation while allowing the evaluation of the system response when additional non-dominant poles are introduced within the loop bandwidth. In this case, the initial value of the Phase Margin PM is 77.36 degrees.

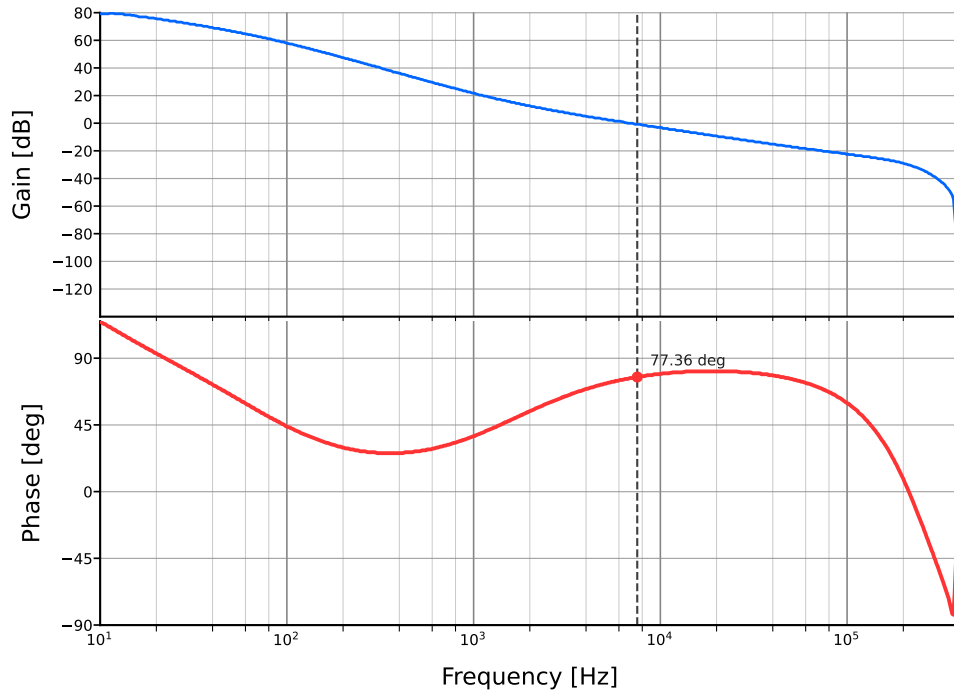


Figure 1.8: 'ARM' Buck converter SIMPLIS Bode graph without in-band poles. [blue: Gain, red: Phase]

Such behavior is expected when the transconductance stage is modified to reduce the offset temperature drift, due to the inherent trade-off between offset, bandwidth, and phase margin. The effects of these additional poles on the loop dynamics can be observed in Fig. 1.9, where it has been introduced a secondary pole at 20 kHz, initially at a higher-frequency, and the simulated system response highlighted the expected degradation of the dynamic performance, that clearly indicate the phase margin is the parameter most strongly affected by the introduction of additional singularities within the loop bandwidth, in fact we have a degradation from 77.36 degrees to 56.74 degrees.

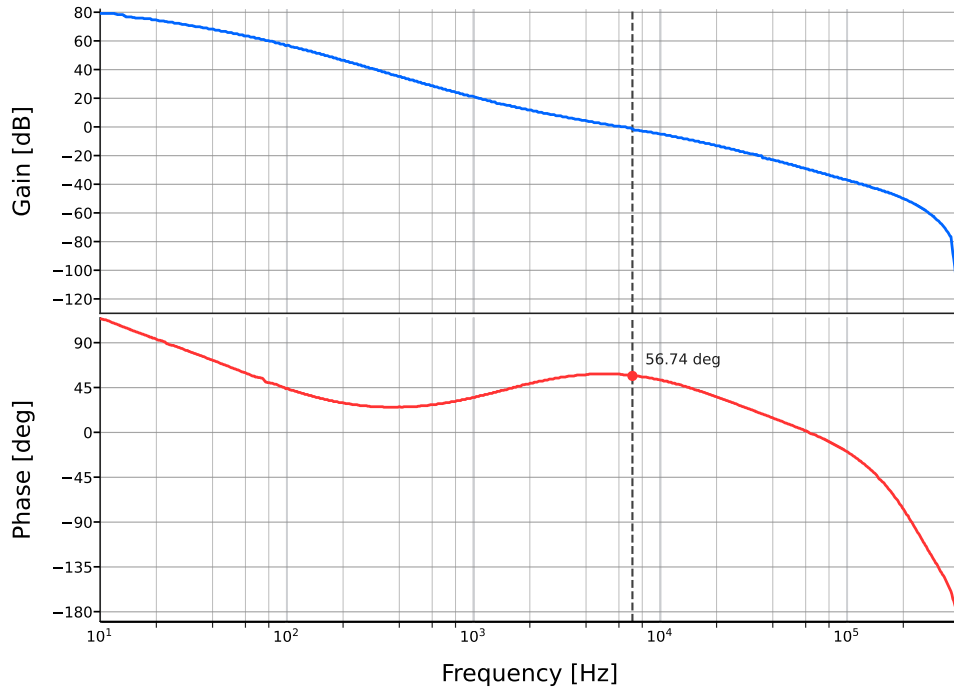


Figure 1.9: 'ARM' Buck converter SIMPLIS Bode graph with in-band poles. [blue: Gain, red: Phase]

Chapter 2

State of the Art for Offset and Thermal Drift Reduction

2.1 Introduction

In current-mode regulated buck converters, the accuracy of the output voltage is strongly influenced by the performance of the feedback loop. Among all the blocks involved in the regulation process, the error amplifier represents one of the main sources of systematic error due to input offset voltage and temperature drift. Any input-referred offset voltage present in the amplifier is translated, through the feedback network, into an output voltage regulation error. In addition, variations of the offset voltage with temperature introduce additional output drift, degrading the regulation accuracy over the entire operating temperature range.

For this reason, the reduction of offset voltage and temperature drift has been widely investigated in CMOS operational amplifiers and operational transconductance amplifiers. The main origin of offset is device mismatch, mainly due to random variations of threshold voltage, mobility-related parameters and geometrical dimensions. In conventional CMOS differential stages, the dominant contribution is usually associated with the input differential pair, while additional contributions can arise from current mirrors and active loads [7, 8, 9]. These effects become especially critical in precision power management circuits, where even a few millivolts of offset can lead to a non-negligible output voltage error.

To address this challenge, a number of research papers dealing with low-offset OTA design and offset compensation techniques were studied [10] [11] [12] [13] [14]. The analysis of the literature provided the foundation for the two approaches investigated in this work: transistor-level optimization and digitally assisted offset compensation.

Particular attention was devoted to [14] that systematically collects and compares the most effective techniques for reducing OTA offset and its

temperature-dependent drift. Since this work presents several practical implementations and compensation strategies, it represented a valuable reference point for the investigation adopted in this thesis; Analyzed with specific attention to the temperature drift of both trimmed and untrimmed offset voltage, the paper discusses conventional static offset compensation methods, such as constant current injection, MOS physical size programming and tail offset voltage trimming, and also introduces temperature-aware techniques such as temperature-compensated current injection, temperature-compensated active-load trimming, constant-resistance tail offset generation and series input-referred voltage generation.

It should be noted that dynamic offset cancellation techniques, such as auto-zeroing and chopper stabilization, were not considered within the scope of this work. Although these approaches are capable of achieving very low residual offset levels, their implementation would require significant modifications to the original amplifier architecture and would introduce additional switching circuitry inside the control loop. For the buck converter considered in this thesis, the resulting impact on loop dynamics, stability analysis and overall system verification would substantially increase the design complexity. Furthermore, the development and validation of such solutions would require a time effort that exceeds the scope and duration of the present work. For these reasons, the investigation was focused on static offset reduction techniques and on system-level calibration approaches that can be integrated while preserving, as much as possible, the original error amplifier architecture.

2.2 Offset Sources in CMOS OTAs

In a CMOS OTA, the input-referred offset voltage originates from the mismatch between nominally identical devices. In a differential pair, threshold voltage mismatch is typically one of the most important contributors. Even if the two input transistors are designed with the same geometry and placed using a symmetric layout, process variations introduce a finite difference between their electrical parameters. This generates an equivalent differential input voltage that must be applied to balance the output currents.

The active load and current mirrors also contribute to the total input-referred offset. Mismatch in mirror devices produces an imbalance between the output branch currents, which is then referred back to the input through the transconductance of the differential pair. Therefore, the total offset of the OTA can be interpreted as the sum of the input-pair contribution and the current-mirror or active-load contribution [8][14].

Temperature adds a second level of complexity. Some mismatch components, such as threshold voltage differences between matched devices, can be relatively stable with temperature. Other terms, however, are weighted

by temperature-dependent quantities such as carrier mobility and transconductance. As a result, a trimming action that cancels the offset at a single temperature does not necessarily guarantee a low residual error over the full temperature range $[-40;150]$.

2.3 Conventional Static Offset Compensation Techniques

A common way to compensate offset consists of introducing an auxiliary signal that generates an equivalent input-referred correction with opposite sign. One of the simplest methods is based on programmable current injection. In this approach, a trimming current is injected into one of the branches of the differential stage or into the active load. By selecting the proper current value, the imbalance caused by mismatch can be reduced or canceled [14]. However, current injection has an important limitation. Although it provides a relatively simple trimming mechanism, its effectiveness is strongly related to the temperature behaviour of the differential-pair transconductance. Consequently, excellent offset cancellation at the trimming temperature may not guarantee low drift over the entire operating range. This makes simple current injection less attractive when the main target is not only offset cancellation at room temperature, but also drift reduction over a wide temperature range.

Another possibility is to modify the effective dimensions of selected MOS devices. This can be done by enabling or disabling elementary transistor segments, changing the effective width of the input pair or of the current mirror. This method is conceptually simple and can be implemented with digital trimming bits. It is especially interesting when the designer wants to reduce mismatch contributions while preserving the general structure of the original OTA. Nevertheless, the achievable resolution depends on the segmentation strategy, and the modification of device sizes can also affect parasitic capacitances, bandwidth and bias conditions.

Tail offset voltage trimming represents a further solution. In this case, a programmable voltage is generated between the source terminals of the input differential pair, producing an equivalent input-referred offset. This approach can provide an effective correction of voltage offset, but it introduces source degeneration. As a consequence, the differential-pair transconductance is reduced, which can decrease the amplifier gain and bandwidth [14].

2.4 Temperature-Aware Compensation Techniques

More advanced techniques try to generate a compensation signal with a temperature behavior matched to that of the offset component to be can-

celed. In [14], temperature-compensated current injection is proposed as an improvement over constant current injection. In this method, the auxiliary current is generated with a thermal dependence designed to follow the temperature characteristic of the input differential pair transconductance. If the thermal behavior is properly matched, the input-referred compensation term becomes more stable with temperature.

A similar concept can be applied to the active-load current mirror. Instead of injecting a generic constant correction current, the active load is modified in such a way that the resulting current imbalance has a temperature dependence compatible with the OTA transconductance. This allows the compensated offset to remain more stable across temperature, provided that the compensation branch and the input stage are properly matched from a thermal point of view [14]. However, additional trimming branches and bias circuitry are required, increasing the implementation complexity of the amplifier.

Other solutions use constant-resistance tail offset generators or series input-referred voltage generators. These approaches aim to generate a more temperature-stable voltage correction, which can directly compensate the temperature-stable terms of the offset equation. In addition, the concept of transconductance temperature damping can be used to modify the temperature dependence of the ratio between current-mirror transconductance and input-pair transconductance [14]. Overall, these methods show that offset compensation cannot be considered only as a static cancellation problem. The temperature behavior of the compensation mechanism is equally important, especially in applications where the circuit must operate over a wide temperature range.

2.5 Digitally Assisted and System-Level Compensation

An alternative approach consists of moving part of the compensation task from the transistor level to the system level. In this case, the error produced by analog offset is measured by an auxiliary sensing path, and a digital controller adjusts the control loop reference voltage provided through a DAC. The compensation code can then be stored or updated depending on the operating mode.

This type of solution is particularly suitable when the objective is not only to compensate the intrinsic offset of the error amplifier, but also to correct the combined effect of several blocks in the feedback path. In a buck converter, the final output voltage error can be affected by the resistive divider, buffer, error amplifier and other analog interfaces. A system-level ADC-DAC loop can therefore compensate the residual error observed at the system output, instead of acting only on a single internal mismatch source.

Compared to transistor-level trimming, a digitally assisted compensation loop offers higher flexibility. It can be implemented as a calibration procedure during test mode or as a slow correction loop during operation. Moreover, it allows the original analog cell to remain unchanged, which is a relevant advantage when the circuit under study is part of an existing and already verified design.

2.6 Discussion and Motivation

Among the techniques reviewed in the literature, the most relevant reference for this work is the approach presented in [14]. The proposed temperature-compensated current injection and active-load trimming methods directly address the same physical problem considered in this thesis: the reduction of input-referred offset voltage and its temperature drift in CMOS OTAs. From a theoretical point of view, these solutions are very interesting because they try to generate a correction term whose thermal behavior follows the OTA transconductance, reducing the residual drift after trimming.

However, it is worth noting that the objective of this thesis is not to design a dedicated offset-trimmed OTA from scratch. Instead, the starting point is an existing error amplifier already integrated within a validated buck converter architecture. Under this constraint, the introduction of dedicated trimming branches, auxiliary mirrors and additional bias circuits would significantly increase design complexity and verification effort.

[Table 2.1 shows the various characteristics of each implementation, allowing for a quick comparison of the pros and cons]

For this reason, a less invasive strategy is preferred. Instead of introducing a dedicated auxiliary trimming structure inside the OTA, the original amplifier cell is kept unchanged at topology level, and the design effort is focused on transistor-level optimization. In particular, device dimensions are modified to improve matching, reduce the intrinsic input-referred offset and limit the temperature sensitivity of the amplifier. This approach is less invasive and is more compatible with a cell that already belongs to an existing product architecture.

The second strategy proposed in this thesis follows a different direction. Rather than forcing the complete offset compensation inside the analog amplifier, a digitally assisted servo loop is introduced at system level. Referring to Figure 5.1, the ADC measures the residual output error associated with the analog offset, while the DAC applies a corrective signal controlled by digital logic. In this way, the compensation is performed on the actual regulated quantity, taking into account not only the error amplifier offset but also the contribution of the surrounding feedback path.

Technique	Offset Reduction	Temp. Drift	Complexity	Impact on OTA
Chopper	Excellent	Excellent	High	High
Auto-zero	Excellent	Excellent	High	High
Current Injection	Good	Poor	Medium	Low
Tail Trimming	Good	Good	Medium	gm degradation
Active Load Trimming	Good	Good	Medium	Low
Michal Temperature Compensation	Very Good	Very Good	High	Medium
Proposed Cell Optimization	Excellent	Excellent	Low	Minimal
Proposed ADC-DAC Servo Loop	Excellent	Excellent	Medium	No OTA modification

Table 2.1: State-of-the-Art comparative table.

Therefore, although the solution proposed in [14] represents the most relevant and technically meaningful approach found in the literature for OTA offset and drift compensation, it is not the most suitable choice for the objective of this thesis. The preferred design direction is either to optimize the dimensions of the existing error amplifier cell without changing its architecture, or to compensate the residual offset at system level through the proposed ADC-DAC digital servo loop. This choice provides a better trade-off between accuracy, implementation complexity and compatibility with the original buck converter architecture.

Error Amplifier Analysis

The diagram illustrates a two-stage CMOS operational amplifier. The first stage (highlighted in green) is a differential pair consisting of PMOS transistors Mb1 and Mb2, and NMOS transistors MP1 and MP2. The input nodes are VIN_P and VIN_N. The second stage (highlighted in blue) is a common-source stage with PMOS load transistors Mb3 and Mb4, and NMOS input transistors MN1 and MN2. The output is taken from the common source of MN1 and MN2, labeled as n1 and n2. The diagram also shows bias voltages Vb and Vc, and various intermediate nodes like MP3, MP4, MP5, MP6, MP7, MP8, MP9, MP10, MN3, MN4, MN5, and MN6.

The error amplifier [Fig. 3.1] adopted in the ARM buck converter is a multi-stage analog architecture specifically designed to provide high DC gain while maintaining adequate bandwidth and stability within the converter feedback loop. At a high level, the amplifier can be divided into different functional blocks:

- 25

3. Cascode branch with Internal Loop.
4. Output transconductance stage.

The input section receives the feedback and reference voltages and performs the required level shifting to properly bias the internal signal path. This block allows the following amplification stages to operate around their desired common-mode voltage while preserving the available signal swing.

After the input conditioning network, the signal is processed by the main differential stage. This block represents the core of the error amplifier and is responsible for converting the input voltage difference into a differential current. As in most high-gain CMOS amplifiers, the overall offset performance is largely determined by the matching properties of the devices of this section.

The differential pair is followed by a cascoded gain stage. The purpose of this block is to increase the intrinsic output resistance seen by the signal path and therefore maximize the achievable open-loop gain. The use of cascoding also improves isolation between different nodes of the amplifier, reducing the sensitivity to supply and bias variations. A further amplification stage is implemented close to the output node in order to provide the required transconductance and drive capability for the compensation network and the following control circuitry. Particular attention is devoted to the local feedback structure.

This auxiliary high-frequency loop is not intended to control the converter itself, but rather to locally linearize the output transconductance stage. More specifically, the local feedback reduces the dependence of the overall cell transconductance on the intrinsic transconductance of the individual MOS devices. As a consequence, variations of the MOS parameters due to process spread, mismatch and temperature have a reduced impact on the effective transconductance seen by the signal path. This improves the robustness and predictability of the amplifier behaviour while maintaining a sufficiently large bandwidth.

In order to better identify the origin of the offset voltage and its temperature drift, the error amplifier will be separated into two main blocks: the input level shifter and the signal path extending from the differential pair to the output stage.

This partition allows the two sections to be analyzed independently, making it possible to identify and quantify their respective contributions to the overall offset voltage and temperature drift. By isolating the effects generated by each block, a more accurate understanding of the mechanisms responsible for the observed thermal offset variation can be obtained. The results of this analysis will then be used in the following chapters for the optimization process.

3.2 Input Stage Analysis

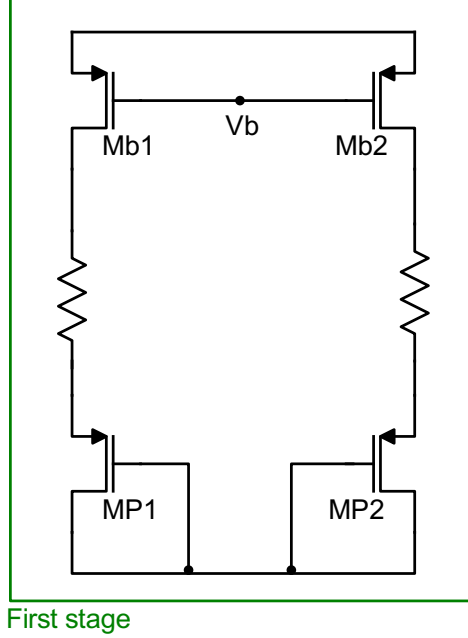


Figure 3.2: Isolated error amplifier level shifter stage.

The first block under investigation is the input level shifter, shown in Fig. 3.2.

The purpose of this stage is to translate the input common-mode level to the internal operating range required by the subsequent amplification stages while preserving the differential information carried by the input signal. The circuit is mainly composed of a bias generation network, source-follower structures and bias stabilization devices that establish the proper DC operating point of the internal nodes.

From a functional perspective, the level shifter does not provide voltage gain (it is slightly lower than 1). Its primary role is instead to generate the required voltage translation and bias conditions needed by the differential amplification stage. Nevertheless, transistor mismatch and temperature-dependent variations within this block can still introduce an input-referred offset contribution that propagates through the entire signal path.

For this reason, the level shifter is analyzed separately from the main amplification stage. The objective is to quantify its contribution to the overall offset voltage and to evaluate whether its temperature behaviour plays a significant role in the measured offset drift of the complete error amplifier.

By performing a MonteCarlo analysis in temperature of the isolated level shifter over a total of 600 simulation points, it can be observed from

Table. 3.1 that the offset temperature drift is negligible. Note: The MonteCarlo simulation was configured to include both process variations and mismatch effects, although mismatch is expected to be the dominant contributor. Simulations confirmed that process variations have a negligible impact on the offset temperature drift, in agreement with the theoretical analysis. Nevertheless, both cases were evaluated throughout this work.

Test	Min	Max	Mean	Std Dev
OFFSET	-4.946m	4.709m	13.77u	1.824m
-40 °C	-4.946m	4.709m	13.97u	1.824m
27 °C	-4.914m	4.685m	13.8u	1.816m
150 °C	-4.853m	4.637m	13.53u	1.799m

(a) Real implementation results

Test	Min	Max	Mean	Std Dev
OFFSET	-5.167m	5.465m	39.48u	1.863m
-40 °C	-5.167m	5.465m	39.51u	1.863m
27 °C	-5.127m	5.431m	39.79u	1.852m
150 °C	-5.087m	5.357m	39.16u	1.834m

(b) Ideal implementation results

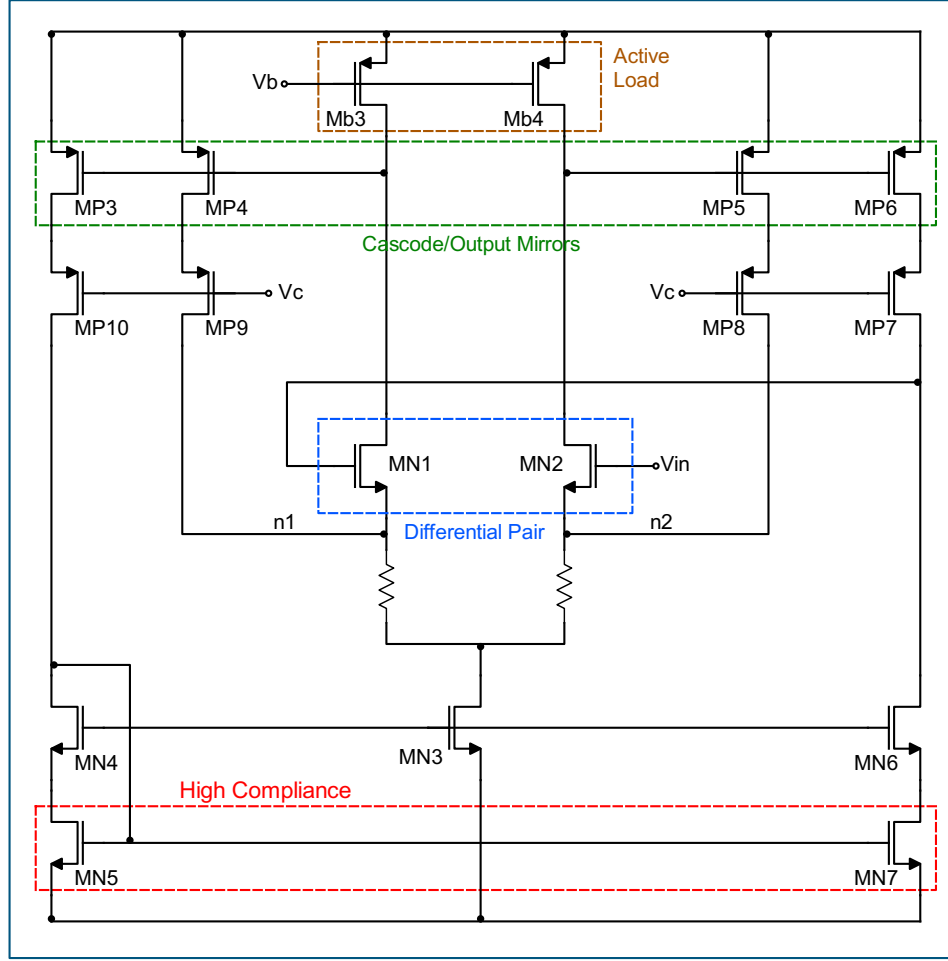
Table 3.1: Error amplifier level shifter offset MonteCarlo simulation results, 200 runs for each temperature.

As reported by Michal [14], this behavior is expected when the offset is dominated by the input threshold voltage mismatch term, $\Delta V_{TH,IN}$, whose temperature dependence is generally weak.

The simulation results support this interpretation, in fact, the simulated value of $\Delta V_{TH,IN}$ is approximately 1.8 mV, which is in good agreement with the observed result, while only a very small variation is observed across temperature. This indicates that the level shifter is not the primary source of the offset drift observed in the complete error amplifier and that the dominant temperature-dependent contribution is generated in the following stage. Moreover, by idealizing the p-current mirror, it can be observed from Table 3.1b that its behavior remains essentially unchanged. Therefore, it can be reasonably excluded as a contributor to the measured offset drift. This observation further supports the hypothesis that the residual offset contribution is mainly associated with the $\Delta V_{TH,IN}$ mismatch term, whose

simulated value is approximately 1.8 mV.

3.3 Second Stage Analysis



Second stage

Figure 3.3: Isolated error amplifier second stage.

Having demonstrated that the level shifter provides a negligible contribution to the overall offset temperature drift, the analysis can now be focused on the second macro-block of the error amplifier, shown in Fig. 3.3. This section includes the input differential pair, the active loads, the gain enhancement circuitry and the output stage. Unlike the level shifter, this block is responsible for the majority of the voltage gain and therefore represents the most critical portion of the amplifier from both offset and temperature drift perspectives.

The differential pair converts the input voltage difference into a current variation [9], while the active load structure and the cascoded devices increase the effective output resistance and consequently the achievable gain. Any mismatch occurring within these devices is directly translated into an input-referred offset voltage and is therefore obviously expected to have an impact on the overall amplifier behaviour.

Furthermore, several compensation mechanisms and bias-dependent terms are present within this stage. As discussed in the previous section, offset contributions dominated by threshold voltage mismatch generally exhibit a relatively weak temperature dependence. However, when current mirrors, active loads and transconductance-dependent mechanisms are involved, the resulting offset may become significantly more sensitive to temperature variations.

For this reason, the second stage is expected to be the primary source of the offset drift observed in the complete error amplifier. By isolating this block and performing MonteCarlo simulations, it becomes possible to evaluate its individual contribution and identify the dominant mechanisms responsible for the temperature-dependent offset variation.

The temperature drift of the offset voltage was first evaluated for the complete gm stage, the results are shown in Table. 3.2, and as expected here lies the drift observed in the complete error amplifier.

Test	Min	Max	Mean	Std Dev
OFFSET	-6.025m	7.873m	42.23u	2.548m
-40 °C	-6.025m	7.873m	38.07u	2.548m
27 °C	-5.497m	6.939m	36.23u	2.182m
150 °C	-4.857m	5.895m	52.39u	1.796m

Table 3.2: Error amplifier second-stage offset MonteCarlo simulation results, 200 runs for each temperature.

In a preliminary check, the active load current mirror, so the PMOS mirror above the Differential Pair, was idealized in order to verify whether it could play a relevant role in the observed drift. The obtained result remains essentially unchanged with respect to the original implementation, indicating that this mirror does not affect the temperature drift behavior of the gm stage.

3.4 Identification of the Main Contributors

The next step of the analysis is therefore focused on identifying which circuit blocks are mainly responsible for the temperature-dependent offset variation. This investigation was carried out starting from the mismatch contribution table obtained from the MonteCarlo analysis, Fig. 3.4:

Mismatch Contribution Table

Device	Block	sigmaOut (V)	sigmaVth (V)	sigmaVg (V)	sigmalds (%)
MN5	High-compliance output mirror	2.8548m	3.4511m	3.4511m	6.839
MN2	Differential pair	2.4402m	2.4403m	2.4403m	5.6305
MN1	Differential pair	-2.4402m	2.4403m	2.4403m	5.6305
MN7	High-compliance output mirror	-2.0189m	2.4403m	2.4403m	4.838
MP3	P-cascode/output mirror	2.0056m	4.0293m	4.0293m	4.7837
MP4	P-cascode/output mirror	-1.9988m	4.0293m	4.0293m	4.7837
MP5	P-cascode/output mirror	1.9958m	4.0293m	4.0293m	4.7816
MP6	P-cascode/output mirror	-1.416m	2.8492m	2.8492m	3.3811
Mb3	-	-943.58u	1.1199m	1.1199m	1.1227
Mb4	-	942.59u	1.1199m	1.1199m	1.1227
MN4	-	95.301u	17.206m	17.206m	41.47
MN6	-	-59.03u	12.167m	12.167m	29.532
MP10	-	9.0287u	9.1588m	9.1588m	18.803
MP9	-	-9.02u	9.1588m	9.1588m	18.772
MP8	-	9.0132u	9.1588m	9.1588m	18.767
MP7	-	-6.4156u	6.4762m	6.4762m	13.186
MN3	-	-3.0933u	1.7073m	1.7073m	1.7405

Figure 3.4: MonteCarlo mismatch contribution table.

In addition, a dedicated DC mismatch analysis was performed as a further confirmation, Fig. 3.5:

Contributor	Max contribution	Yield = 100.00% R²= 0.91945	Yield = 100.00% R²= 0.90967	Yield = 100.00% R²= 0.90715
Top	100%	<div><div></div></div>	<div><div></div></div>	<div><div></div></div>
MN5	24%	<div><div></div></div>	<div><div></div></div>	<div><div></div></div>
MN2	24%	<div><div></div></div>	<div><div></div></div>	<div><div></div></div>
MN1	20%	<div><div></div></div>	<div><div></div></div>	<div><div></div></div>
MP5	12%	<div><div></div></div>	<div><div></div></div>	<div><div></div></div>
MN7	10%	<div><div></div></div>	<div><div></div></div>	<div><div></div></div>
MP3	10%	<div><div></div></div>	<div><div></div></div>	<div><div></div></div>
MP4	10%	<div><div></div></div>	<div><div></div></div>	<div><div></div></div>
MP6	4%	<div><div></div></div>	<div><div></div></div>	<div><div></div></div>

Figure 3.5: DCmatch mismatch contribution table.

The two analyses led to consistent results, highlighting three main sources of contribution to the offset: the high-compliance mirror placed on the out-

put branches, the cascode mirror associated with the output loop, and, as expected, the input differential pair itself.

Based on these results, the analysis proceeds by progressively idealizing the current mirrors that were identified as relevant contributors of the offset, knowing that the current mismatch of these mirrors produces drift in temperature. The purpose of this approach is to verify whether removing the mismatch contribution of each selected mirror produces a corresponding improvement in the temperature drift of the offset voltage.

Idealization of the Mirrors

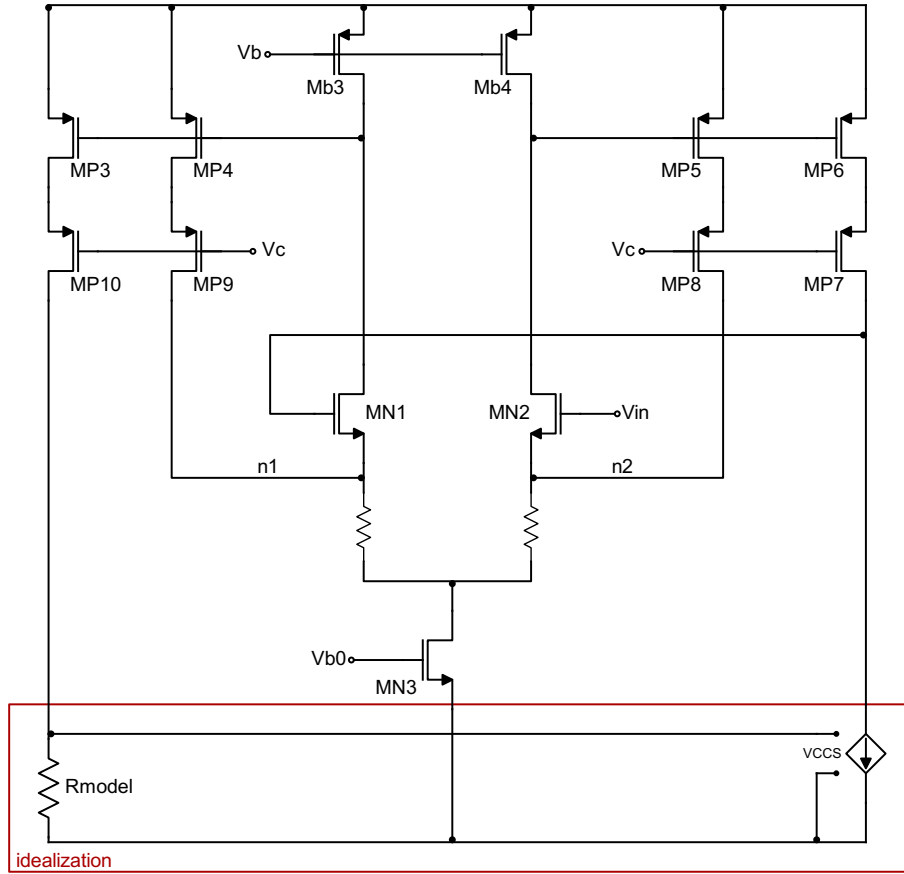


Figure 3.6: Idealized error amplifier high compliance mirror.

The first step consists in the idealization of the high-compliance current mirror. As shown in Fig. 3.6, the mirror is replaced by an equivalent structure based on a resistor and a voltage-controlled current source. These elements are implemented in such a way that the original operating condition of the circuit is preserved.

Test	Std Dev
OFFSET	2.213m
-40 °C	2.213m
27 °C	1.978m
150 °C	1.719m

Table 3.3: Error amplifier offset MonteCarlo simulation results with idealized high compliance mirror, 200 runs for each temperature.

The results reported in Table. 3.3 show that the idealization of this mirror leads to a clear reduction of the offset temperature drift. The temperature coefficient decreases from the initial value of 0.145% to approximately 0.12%. This confirms that the high-compliance mirror provides a relevant contribution to the temperature-dependent offset behavior of the stage.



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Test	Std Dev
OFFSET	2.024m
-40 °C	2.024m
27 °C	1.785m
150 °C	1.55m

Table 3.4: Error amplifier offset MonteCarlo simulation results with idealized cascode/output mirror, 200 runs for each temperature.

As reported in Table. 3.4, the idealization of this mirror also produces a significant improvement in the temperature drift of the offset voltage. In this case, the temperature coefficient is reduced to approximately 0.115%, starting from the original value of 0.145%. It is important to note that, during this second analysis, the high-compliance mirror is kept in its real transistor-level implementation. Therefore, the observed improvement can be attributed specifically to the idealization of the cascode mirror and output-loop contribution.

The input differential pair is intentionally kept unchanged throughout this analysis. This choice, imposed by the customers, is made to preserve the intrinsic transconductance of the stage and avoid modifying the core behavior of the amplifier. For the purpose of this study, acting on the current mirrors identified by the mismatch analyses is sufficient to evaluate the main design directions for reducing the offset temperature drift. Moreover the differential pair is not expected, from theory, to have a component in the drift, but only on the offset "static" value. The effect of the mirror sizing will be investigated in more detail in the following chapter, where different design solutions will be compared in terms of offset temperature coefficient at the complete cell level.

3.4.1 Loop-Gain Evaluation of the Original gm Stage

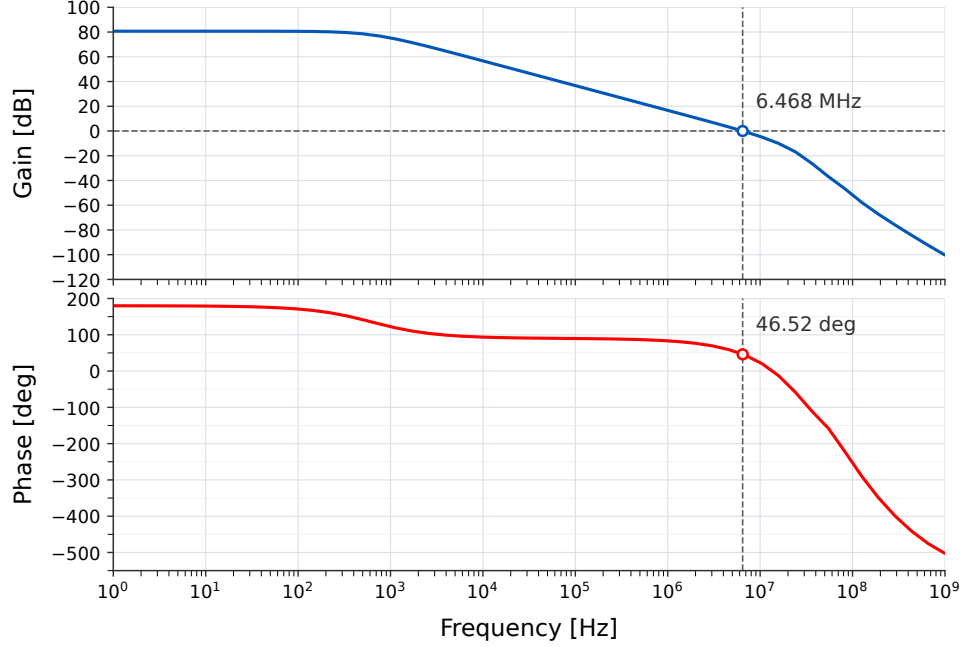


Figure 3.8: Error amplifier original loop gain. [blue: Gain, red: Phase]

Before proceeding with the sizing optimization, the loop-gain behavior of the original, unmodified cell is evaluated. Referring to Fig. 3.8, there is the stability simulation results of the original gm stage connected in a buffer configuration in order to analyze the effect of the secondary poles on the bandwidth and on the phase margin. For this analysis, an output capacitance equal to 1 pF is imposed.

This configuration provides a useful reference for the following comparisons, since it allows the stability behavior of the original implementation to be assessed before any sizing modification is introduced. In the next sections, the same analysis will be repeated after the optimization of the selected current mirrors, in order to verify how the sizing changes affect both the offset temperature drift and the dynamic behavior of the cell.

Chapter 4

Analog Design Optimization of the Error Amplifier

4.1 Device Sizing Strategy

Once the main contributors to the offset temperature drift have been identified, the next step is to determine the most suitable sizing of the involved current mirrors. The objective is not to minimize the temperature drift alone, but rather to find the best trade-off among the most relevant performance metrics of the cell, namely bandwidth, phase margin, offset voltage, and offset temperature drift. For this purpose, a set of parametric simulations is performed by varying the geometrical dimensions of the mirrors identified in the previous section.

$$\sigma_{\Delta V_{TH}}^2 = \frac{A_{V_{TH}}^2}{WL}$$

Following Pelgrom's mismatch law [7] [15], the optimization process is mainly focused on the transistor dimensions W and L , since increasing the device area is expected to reduce mismatch-related effects and consequently improve the offset temperature behavior.

$$L \uparrow \Rightarrow g_m \downarrow \Rightarrow \frac{\sigma_I}{I} \downarrow \Rightarrow \text{Offset Drift} \downarrow$$

Increasing the channel length of critical current mirror devices improves matching and reduces sensitivity to second-order process effects, resulting in a lower temperature dependence of mirror current mismatch and consequently reduced input-referred offset drift. At the same time, larger device width introduces additional parasitic capacitances [16, 15], which inevitably impact the dynamic response of the circuit.

$$W \uparrow \Rightarrow C_{\text{parasitic}} \uparrow \Rightarrow \text{Velocity} \downarrow$$

The final choice is therefore based on a global evaluation of all the considered parameters rather than on the temperature coefficient alone.

Note: the first value in the X-axis of the following plots is the initial value of the swiped parameters.

High-Compliance Mirror Optimization

The first optimization step focuses on the high-compliance mirror. Figure 4.1 reports the results obtained by sweeping the transistor length while monitoring bandwidth, phase margin and offset temperature drift.

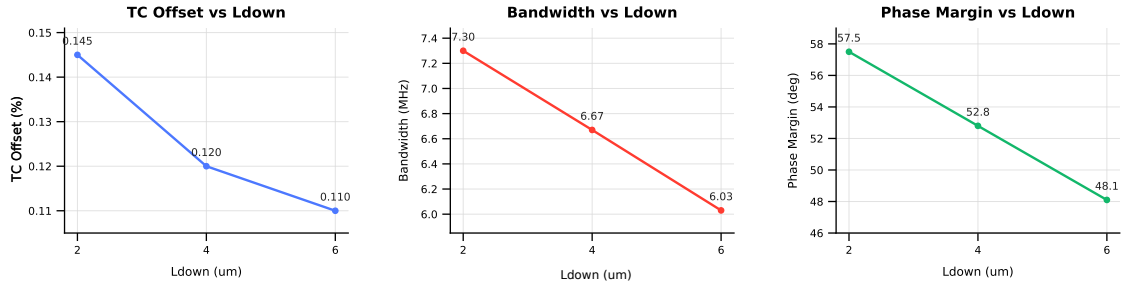


Figure 4.1: Sweep of high compliance L.

As expected, increasing the channel length leads to a significant improvement in the offset temperature drift. This behavior is consistent with Pelgrom's law [7], since the larger device area reduces the impact of mismatch on the mirror operation. However, the improvement is achieved at the expense of the dynamic performance of the stage. In particular, the increased parasitic capacitances associated with larger devices reduce the bandwidth and slightly affect the phase margin, as commonly observed in this type of trade-off.

As a design constraint, a maximum bandwidth degradation of approximately 1 MHz with respect to the original implementation is accepted. Considering this limitation together with the improvement in temperature drift, a channel length equal to 6 μm is selected as the best compromise for the high-compliance mirror.

Cascode/Output Mirror Optimization

A similar analysis is then performed on the cascode/output mirror. The obtained trends are reported in Fig. 4.2:

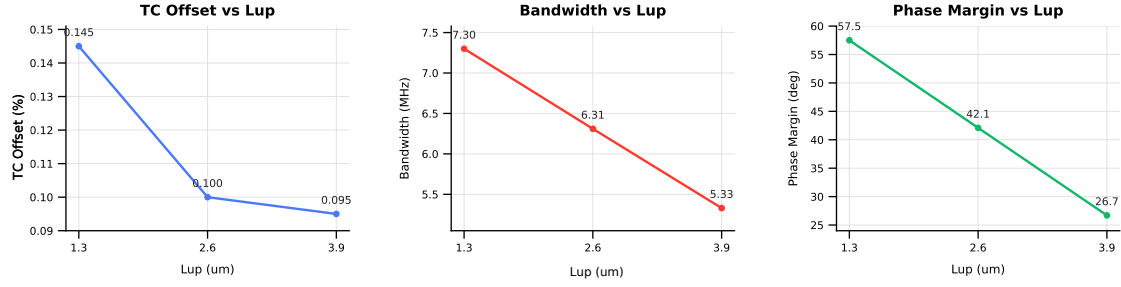


Figure 4.2: Sweep of cascode/output mirror L.

As expected, increasing the transistor length produces a behavior very similar to that observed for the high-compliance mirror. In particular, for the same scaling factor (3x), the resulting improvement in temperature drift is nearly identical. More in the detail, the temperature coefficient reduction is equal to

$$\Delta TC_1 = 0.145 - 0.11 = 0.035$$

for the first case, while

$$\Delta TC_2 = 0.145 - 0.095 = 0.050$$

for the second one, indicating that the contribution of the two mirrors to the overall offset temperature coefficient is comparable.

The optimization is again performed considering both the temperature coefficient and the dynamic performance of the stage. Although a further improvement can be observed when moving from a scaling factor of two to three, the gain in temperature coefficient becomes progressively smaller. Considering the limited benefit and the associated bandwidth reduction, a channel length of 2.6 μm is selected for the upper branch devices. This value satisfies the previously imposed bandwidth constraint while still providing a meaningful reduction in offset temperature drift.

Width Optimization

The effect of transistor width was also evaluated for both mirrors. Unlike the channel length increase, which improved the circuit temperature drift without affecting its overall dynamic performance, increasing the width Fig. 4.3 does not produce substantial improvements in the offset temperature coefficient, especially once the previously selected length modifications have already been applied.

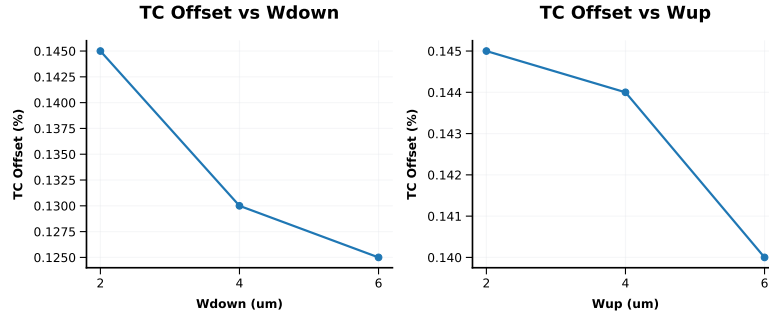


Figure 4.3: Sweep of high compliance and cascode/output mirrors widths.

Since the drift reduction is relatively limited while the larger devices would further increase parasitic capacitances and slow down the circuit, only the width of the bottom mirror will be slightly enlarged (4 um). Anyway, it is not convenient to further increase these parameters.

Considerations on Stability

It should be noted that all the previous analyses are performed with the gm stage connected in a buffer configuration. Consequently, the phase margin values obtained at this stage should be regarded only as an indicator of the relative stability variations introduced by the sizing modifications. A complete evaluation of the dynamic performance will be carried out in the following sections by integrating the optimized cell into the full converter model and performing system-level simulations in SIMPLIS. This approach will allow the actual impact of the proposed modifications on bandwidth, phase margin and overall loop stability to be assessed under realistic operating conditions.

4.2 Thermal Drift Reduction Results

Test	Min	Max	Mean	Std Dev
OFFSET	-7.082m	7.352m	54.18u	3.049m
-40 °C	-7.082m	7.352m	50.98u	3.049m
27 °C	-6.878m	7.215m	49.8u	2.943m
150 °C	-6.605m	7.069m	61.76u	2.815m

Table 4.1: Final solution error amplifier offset MonteCarlo simulation results, 200 runs for each temperature.

Table 4.1 reports the results of a 600-point Monte Carlo temperature analysis performed on the final error amplifier implementation, featuring 2u/2.6u devices in the mirror and cascode/output branches, and 4u/6u devices in the high-compliance branch. The obtained offset temperature coefficient is equal to 0.057%, representing a significant improvement compared to the initial value of 0.145%.

These results confirm the effectiveness of the proposed sizing strategy in reducing both the offset magnitude and its temperature dependence, leading to a more robust implementation across the considered temperature operating range.

4.3 Singularities

In order to gain a better understanding of the overall amplifier behaviour, the architecture can be divided into three main blocks: the level shifter, the cascode gain stage with cascode load, and the differential output stage.

The small-signal transfer function of each block has been derived independently and can therefore be combined to estimate the overall low-frequency voltage gain.

The transfer function of the level shifter is given by

$$A_{LS} = \frac{V_{out}}{V_{in}} = \frac{g_{m12}r_{27}r_{12}}{r_{12} + (r_{27} + R)(1 + g_{m12}r_{12})}$$

while the gain of the intermediate cascode stage can be approximated as

$$A_{CAS} = -g_{m39} [(g_{m39}r_{29}r_{39}) \parallel (g_{m11}r_{11}r_2)].$$

Finally, the transfer function of the differential pair stage is

$$A_{DIFF} = -\frac{g_{m1}r_1r_0(\Delta + R)}{\Delta R(1 + g_{m1}r_1) + (\Delta + R)(r_0 + r_1) + g_{m4}r_0r_4R(1 + g_{m1}r_1)(1 + g_{m30}r_{30})}$$

with

$$\Delta = r_{30} + r_4(1 + g_{m30}r_{30}).$$

Besides the low-frequency gain, the frequency response of the amplifier is mainly determined by two dominant high-impedance nodes.

The dominant pole is located at the output of the cascode gain stage, where the equivalent output resistance is maximized by the cascoding action. It can be approximated as

$$\omega_{p1} = \frac{1}{R_{out}C_{out}} = \frac{1}{[(g_{m29}r_{29}r_{39}) \parallel (g_{m11}r_{11}r_2)]C_{out}}.$$

As expected, the large equivalent resistance generated by the cascode structure together with the output capacitance produces the lowest-frequency

pole of the system, therefore defining the dominant contribution to the overall frequency response.

The second pole is instead associated with the internal high-impedance node formed by the drain of the differential pair and the gate connection of the subsequent cascode devices, where the parasitic capacitances accumulate. Its position can be approximated by

$$\omega_{p2} = \frac{1}{(r_{p0} \parallel r_{down}) (C_{gd0} + C_{gd1} + C_{gate4,5})}.$$

The capacitance term includes the gate-drain parasitic capacitances of the differential pair together with the gate capacitances of the cascoding devices. Since this node exhibits a significantly lower resistance than the output node, the corresponding pole is shifted toward higher frequencies and therefore acts as the non-dominant pole of the amplifier.

Consequently, the open-loop transfer function can be approximated by

$$A(s) = \frac{A_0}{\left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right)},$$

where

$$A_0 = A_{LS} \cdot A_{CAS} \cdot A_{DIFF}$$

represents the low-frequency gain obtained from the product of the three previously derived stages.

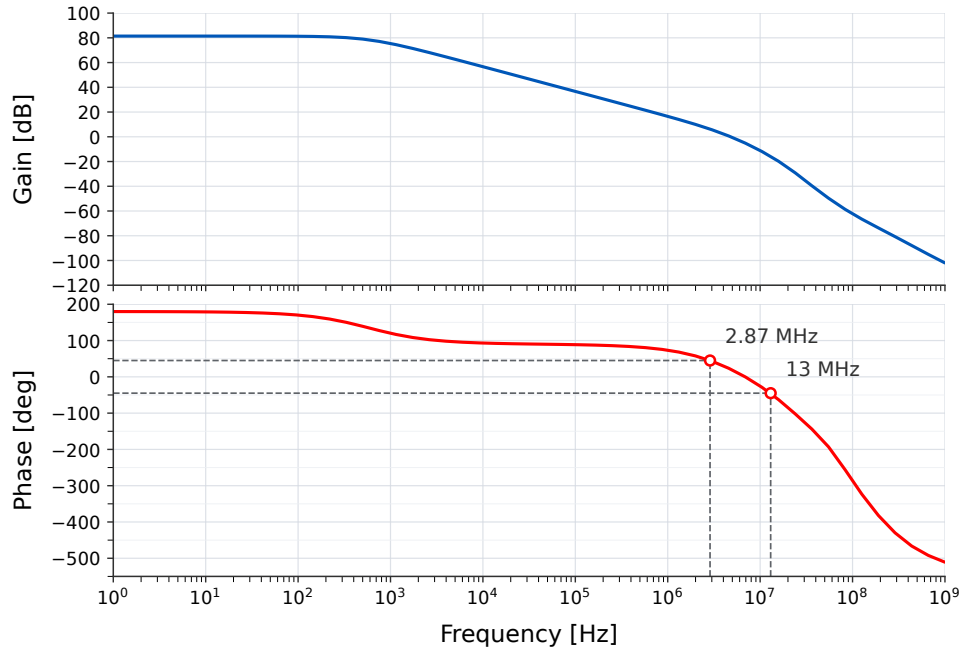


Figure 4.4: Final solution error amplifier loop gain frequency response. [blue: Gain, red: Phase]

Figure 4.4 compares the analytically predicted pole locations with the simulated frequency response. The first secondary pole is estimated around 3 MHz, while the second one is located near 13 MHz. These values are in good agreement with the behaviour observed in simulation, confirming the validity of the simplified small-signal model.

It is worth noting that, before the sizing optimization, they were located at approximately 6 MHz and 13.6 MHz, respectively. Therefore, the adopted transistor sizing strategy mainly affects the first in-band pole, moving it toward lower frequencies and justifying the behavior shown in the previous L sweep.

4.4 Slew Rate

Step	Default Positive	Default Negative	Solution Positive	Solution Negative
30 mV	1.89 MV/s	1.88 MV/s	1.24 MV/s	1.20 MV/s
50 mV	2.90 MV/s	2.97 MV/s	2.05 MV/s	2.20 MV/s
80 mV	3.89 MV/s	4.19 MV/s	3.07 MV/s	3.29 MV/s

Table 4.2: Slew rate comparison

As a drawback of the proposed optimization, besides the reduction in bandwidth and phase margin previously discussed, a degradation in the large-signal response can also be observed in terms of slew-rate.

The slew-rate performance was evaluated by applying a pulse stimulus with a period of 20 μ s, a delay time of 100 ns, rise and fall times of 100 ps, and a pulse width of 10 μ s.

Three different input step amplitudes were considered: 30 mV, 50 mV, and 80 mV.

The results are reported in Table. 4.2. As expected, the optimized solution exhibits a slower response compared to the original implementation. From the measured values, the slew rate decreases by approximately 25 % for both positive and negative transitions across the considered input step amplitudes. Although this reduction represents a dynamic drawback of the proposed solution, it can be considered fully acceptable in the context of the overall design objectives. In fact, the penalty in transient response is relatively limited when compared to the substantial improvement achieved in terms of offset temperature coefficient reduction. Therefore, the obtained trade-off can be regarded as favorable, since a moderate degradation of the large-signal response enables a significant enhancement of the offset stability over temperature.

4.5 SIMPLIS

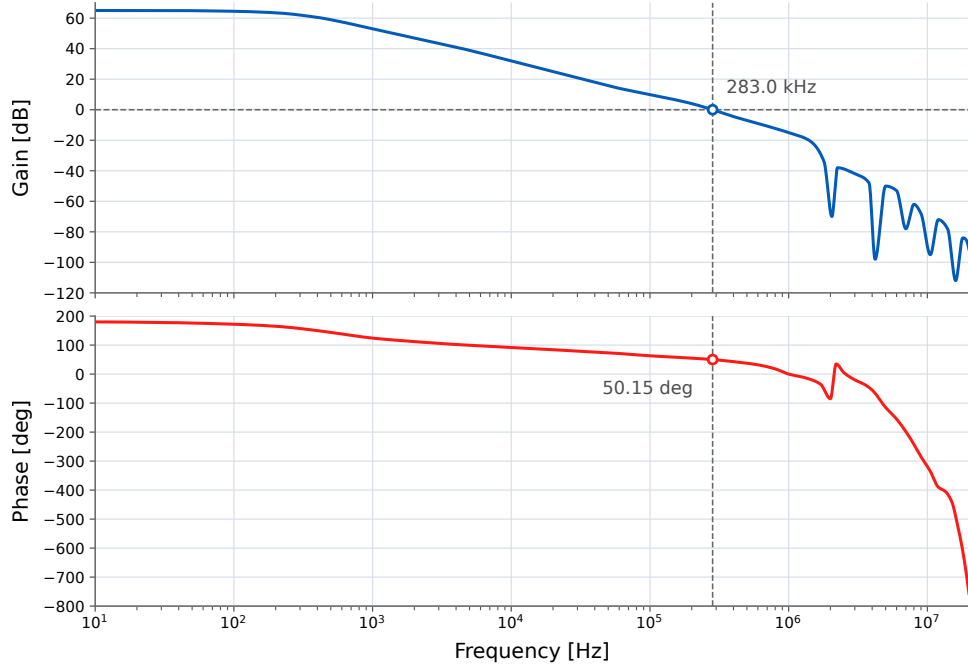


Figure 4.5: SIMPLIS solution voltage loop frequency response. 2.1 MHz application. [blue: Gain, red: Phase]

Figure 4.5 shows the SIMPLIS simulation results obtained using the complete buck converter model, where the transconductance stage is implemented according to the solution identified during the previous optimization study. In this case the model considered an application at 2.1 MHz, the best to evaluate the behavior of new solutions since it is the highest switching frequency selectable and so the worst case scenario.

The resulting behavior is in good agreement with the expected performance.

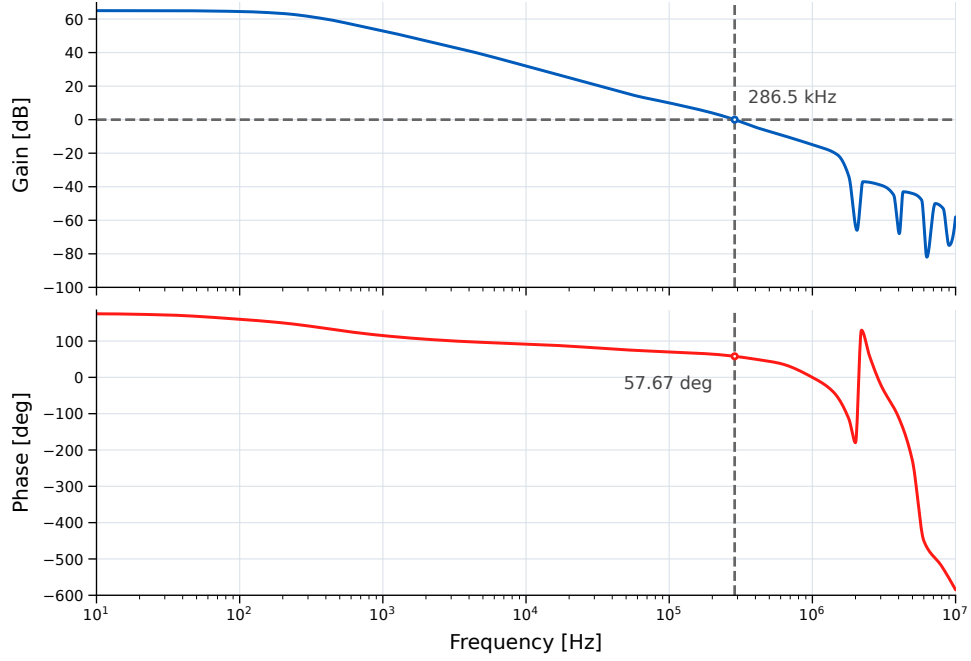


Figure 4.6: SIMPLIS original voltage loop frequency response. 2.1 MHz application. [blue: Gain, red: Phase]

Observed differences are acceptable and mainly affect the phase margin, which decreases by approximately 7.5 degrees with respect to the initial design Figure 4.6. Conversely, the remaining stability parameters exhibit only minor variations, confirming that the proposed sizing modifications do not significantly alter the overall loop dynamics.

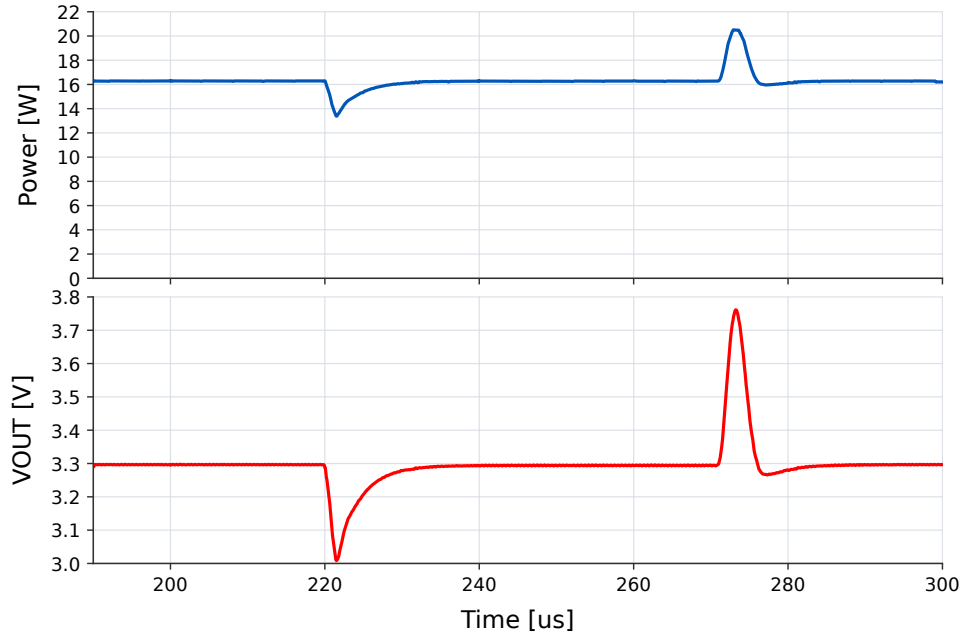


Figure 4.7: Final solution SIMPLIS transient. [blue: Power, red: V_{OUT}]

The transient response in Figure 4.7 further validates the effectiveness of the adopted solution. As shown in the simulation results, the converter operates correctly without oscillations, excessive overshoot, or any anomalous behavior. This confirms that the reduction in phase margin does not compromise the stability of the closed-loop system and that the optimized architecture still provides a robust dynamic response under normal operating conditions.

Chapter 5

Digital-Assisted Offset Compensation

5.1 System-Level Approach

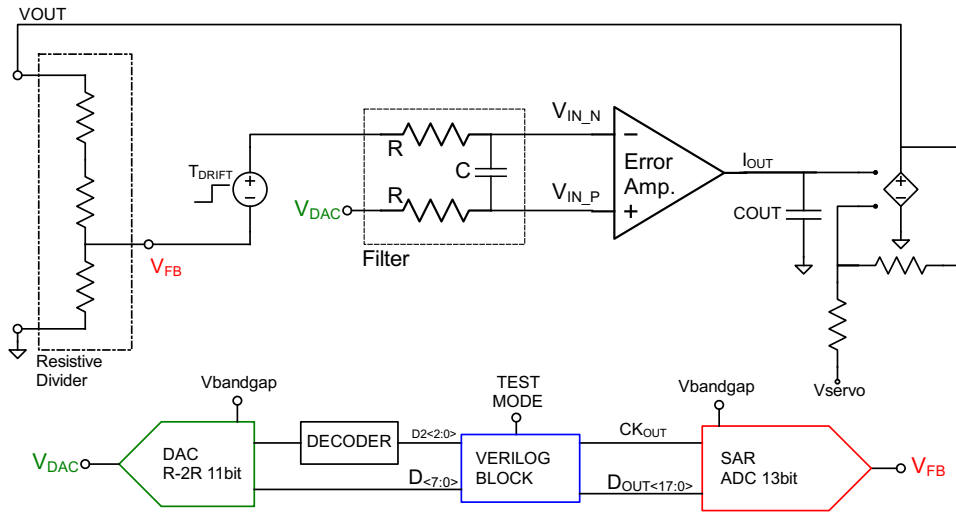


Figure 5.1: Complete system solution architecture.

As an alternative to the transistor-level optimization of the error amplifier, a system-level approach Figure 5.1 was investigated. Instead of directly modifying the analog architecture, the offset compensation is achieved through an auxiliary digital-assisted servo loop, allowing the original error amplifier to remain unchanged.

The main advantage of this solution is that the intrinsic performance of the error amplifier is preserved, avoiding the bandwidth, phase-margin, and slew-rate degradations introduced by the analog optimization. The main

drawback is the additional silicon area required to implement the ADC, DAC, and (to a lesser extent) digital control logic.

The proposed architecture is composed of three main building blocks: a 13-bit SAR ADC (1-bit sign), an 11-bit R-2R DAC, and a digital trimming controller implemented in Verilog. The first two were blocks that were already available, needing only to be correctly implemented by an appropriate study of the IP document, meanwhile the Verilog block was created from scratch.

The ADC continuously monitors the feedback voltage, while the DAC generates a correction voltage that is injected into the analog loop to compensate for the offset introduced by the error amplifier. The digital logic manages the calibration procedure, stores the target value, and updates the DAC code until the offset is minimized.

During the initial calibration phase, the converter output is measured and the corresponding ADC code is stored as a reference value. During normal operation, subsequent ADC conversions are compared against the stored target, and the DAC code is adjusted accordingly. In particular, during production testing, the device is placed in TEST MODE and trimmed to cancel the offset at room temperature. The target code obtained after the trimming procedure is then stored and subsequently used as a reference during the offset cancellation process, where the compensation code is compared against the calibrated value. As a consequence, any offset variation is translated into a correction voltage that counteracts the error introduced by the analog circuitry.

5.2 Theoretical Accuracy

From a theoretical point of view, the achievable compensation accuracy is limited by the quantization step of the trimming loop. Since the minimum correction that can be applied corresponds to one DAC LSB, the residual error after convergence can be approximated as half an LSB.

$$\text{Accuracy} = \text{LSB} = \frac{1.25 \text{ V}}{2^{11}} \approx 610 \mu\text{V}$$

Based on the selected SAR ADC and R-2R DAC resolutions, the theoretical trimming accuracy is approximately

$$\pm \frac{\text{LSB}_{\text{DAC}}}{2} \approx \pm 305 \mu\text{V}$$

which is comparable to the best result achieved through the transistor-level optimization of the error amplifier alone ($234 \mu\text{V} = 0.057\%$).

5.3 ADC Implementation

A Successive Approximation Register (SAR) Analog-to-Digital Converter [3] is one of the most widely adopted architectures for medium-resolution and low-power data conversion. Its operation is based on a binary search algorithm that progressively identifies the digital code corresponding to the sampled analog input voltage. The conversion process starts by sampling the input signal and storing its value on an internal capacitor array. A comparator then evaluates the difference between the sampled input voltage and the output generated by an internal Digital-to-Analog Converter (DAC). Beginning from the most significant bit (MSB), the SAR logic successively determines each output bit by comparing the input signal against a series of reference levels generated by the DAC. After each comparison, the corresponding bit is either retained or cleared, and the procedure continues until the least significant bit (LSB) has been evaluated. As a result, an N-bit SAR ADC requires only N comparison cycles to complete a conversion. This characteristic provides an excellent trade-off between conversion speed, power consumption, silicon area, and resolution, making SAR converters particularly suitable for mixed-signal integrated circuits and digitally-assisted analog systems.

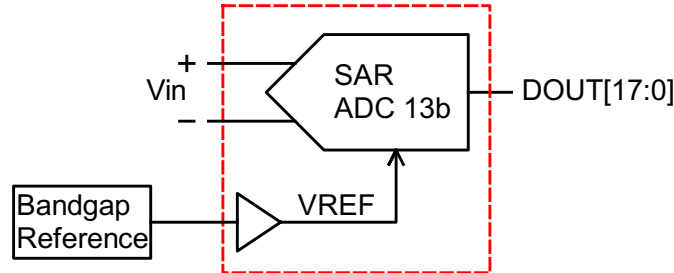


Figure 5.2: SAR ADC architecture.

The measurement stage of the proposed servo loop is based on a 13-bit SAR ADC Figure 5.2. Although the operating principle of the converter is relatively straightforward, its integration within the overall architecture proved to be significantly more challenging than initially expected.

As highlighted by the integration guide, the converter exposes a large number of analog and digital pins dedicated to clock generation, startup control, calibration, configuration, status monitoring, debug functionalities, and communication interfaces. As a consequence, a considerable amount of work was required to correctly configure the block and identify the minimum set of signals necessary for its operation in the proposed application. Particular attention had to be paid to the management of the sampling clock, conversion clock, enable signals, calibration controls, and status outputs, as an incorrect configuration could prevent the converter from producing reli-

able conversion results. In Figure 5.3 is shown the conversion mechanism of the implemented Sar ADC 13b. It can be noticed that each change in the SAR ADC bits corresponds to the DAC R-2R moving closer to the correct value, reaching the expected value 412.5 mV.

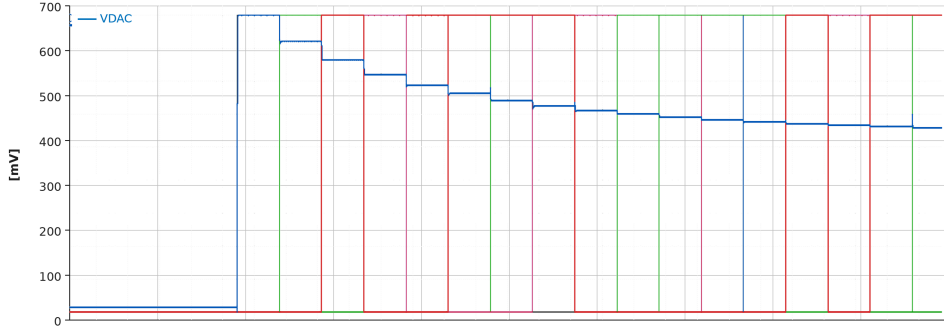


Figure 5.3: SAR ADC complete conversion transient [blue: V_{DAC} , others: ADC bits]

Unlike the DAC block, whose integration was relatively straightforward, the SAR ADC required a much deeper analysis of the available documentation before it could be successfully incorporated into the trimming loop. Several iterations were necessary to understand the behaviour of the various control signals and to verify the correct interaction between the converter and the surrounding digital logic.

Another important aspect concerns the format of the conversion result. The ADC provides its output through an 18-bit bus, denoted as `DOUT<17:0>`. However, only a subset of these bits is useful for the proposed compensation strategy. In particular, the relevant information is contained within the range `DOUT[15:3]`, while the remaining bits are not required by the trimming algorithm.

A further consideration arises from the resolution mismatch between the selected SAR ADC and the R-2R DAC used to generate the correction voltage. While the ADC provides a 12-bit measurement, the DAC resolution is limited to 11 bits. Consequently, the least significant bit contained in the selected output range cannot be directly translated into a corresponding correction step at the DAC output.

For this reason, bit `DOUT[3]` is intentionally discarded before the data is processed by the trimming controller. The useful information is extracted from bits `DOUT[15:4]`, while the quantization mismatch introduced by the one-bit resolution difference is managed entirely with the Verilog control logic. The same Verilog block is also responsible for routing the ADC output bits to the appropriate DAC inputs, also shown in Figure 5.1, according to the mapping strategy adopted for the trimming loop.

From a system-level perspective, the main challenge associated with the

ADC was not related to its conversion accuracy, but rather to its correct integration inside a mixed-signal environment composed of analog circuitry, digital control logic, and a programmable DAC. Once the configuration and data-routing issues had been resolved, the converter provided an accurate measurement of the feedback voltage, enabling the proper operation of the offset compensation algorithm.

5.4 Digital Trimming Logic

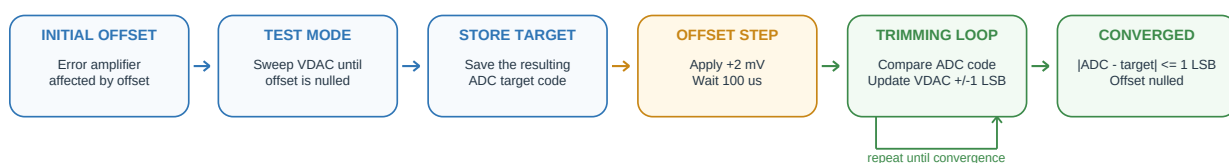


Figure 5.4: Digital trimming logic verification flowchart.

The compensation algorithm shown in Figure 5.4 is implemented through a dedicated digital controller developed in Verilog. In this case, the flowchart represents the procedure adopted to verify the correct operation of the proposed system-level solution. The focus is on validating the offset cancellation mechanism and its interaction with the trimming process. The normal operation of the complete system will be discussed later in Chapter 6. Its main purpose is to continuously compare the value measured by the SAR ADC with a previously stored reference value and update the DAC code accordingly, compensating for offset and temperature-induced variations of the error amplifier. The overall calibration procedure can be divided into two operating phases: an initial calibration phase and a normal trimming phase. Note Table 5.1, that summarizes the Verilog-AMS functionality without inserting the raw code into the thesis document.

Functional block	Role in the trimming loop
wreal-to-digital conversion	Converts ADC outputs, DAC test-mode inputs, clock and control signals from wreal voltage levels into internal digital logic values.
Initialization	Sets the internal registers, trimming code, target code, output registers, clock divider and control flags to a defined initial state.
Test mode operation	Uses the externally imposed DAC code during the calibration phase and stores the initial trimming condition before automatic operation.
Target definition and settling	Defines the target ADC code when exiting test mode and waits before enabling trimming, allowing the analog loop to settle.
Clock division	Updates the trimming code once every four clock cycles, reducing the digital loop speed to match the slower analog dynamics.
Digital trimming algorithm	Compares the current ADC code with the stored target and increments or decrements the DAC correction code by one LSB.
Dead-band logic	Introduces a tolerance window of plus or minus one LSB around the target to avoid unnecessary toggling at convergence.
ADC/DAC resolution management	Uses DOUT[15:4] and discards the least significant selected ADC bit to account for the one-bit resolution difference with the 11-bit DAC.
Bit routing	Maps code_out[10:8] to D2[2:0] and code_out[7:0] to D[7:0], generating the two digital buses required by the DAC.
Digital-to-wreal conversion	Converts the final digital DAC command back into wreal voltage levels equal to either 0 or Vsupply for mixed-signal simulation.

Table 5.1: Trimming logic

During the final test in factory, in the initial calibration phase, the system is operated under controlled conditions and the DAC code is adjusted until the offset contribution of the error amplifier is minimized. Once the desired operating point is reached, the corresponding ADC output code is stored and used as a reference value for all subsequent trimming operations. This code represents the target condition of the system and is therefore used as the reference for the closed-loop compensation algorithm.

After the initialization procedure, the controller enters the trimming mode, where it is imposed an Offset that emulates a drift across temperature in a normal operation of the device. At each conversion cycle, the current ADC output is compared against the stored target code. If the measured value is lower than the reference, the DAC code is incremented by one Least Significant Bit (LSB). Conversely, if the measured value is higher than the target, the DAC code is decremented by one LSB. Whenever the measured code matches the stored reference, no correction is applied and the DAC value is maintained unchanged. Through this iterative process, the controller continuously forces the system toward the desired operating point, compensating for offset drift and process-induced variations.

As mentioned before, an additional task performed by the digital controller concerns the management of the ADC output format. The selected SAR ADC provides its conversion result through an 18-bit output bus, denoted as DOUT<17:0>. However, only a subset of these bits is useful for the compensation algorithm. In particular, the relevant information is contained within bits DOUT[15:3].

Since the correction path employs an 11-bit R-2R DAC, a one-bit resolution mismatch exists between the measurement and correction stages. For

this reason, bit `DOUT[3]` is intentionally discarded before the trimming process. The effective information used by the controller is therefore extracted from bits `DOUT[15:4]`, while the management of the quantization difference between ADC and DAC is handled internally by the trimming logic. The same digital block is also responsible for the correct routing of the ADC output bits to the corresponding DAC input lines according to the adopted coding scheme.

Another important aspect of the proposed Verilog concerns the dynamic interaction between the digital trimming loop and the analog control loop. Due to the intrinsic latency of the feedback network and the compensation circuitry, the analog loop exhibits a significantly slower response compared to the digital trimming algorithm.

If the digital controller were allowed to update the DAC code at every available clock cycle, the compensation process would react much faster than the analog system itself. As a consequence, the digital loop could start applying corrections before the analog loop has fully settled, potentially leading to unnecessary oscillations and an incorrect interpretation of the measured feedback voltage, as shown in Figure 5.5.

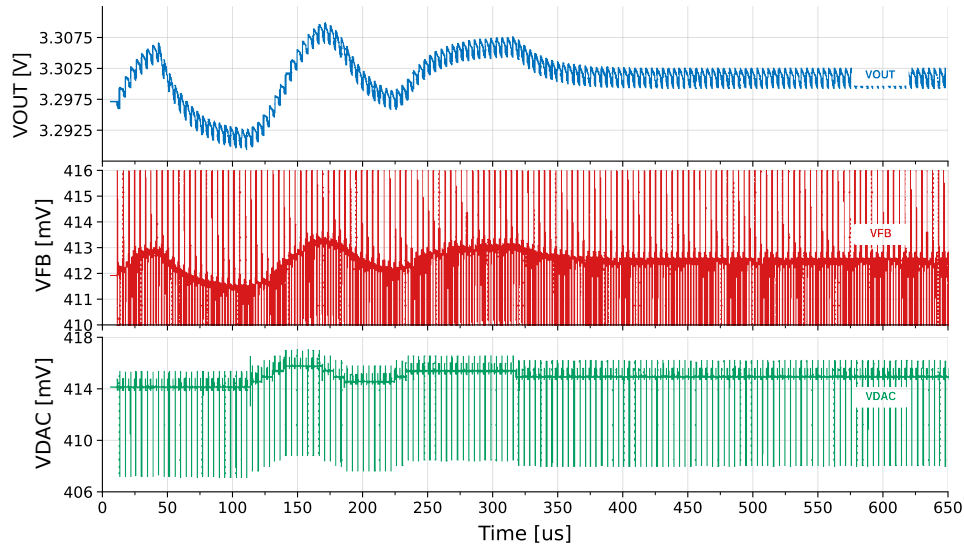


Figure 5.5: Local system solution transient response with trimming at each clock cycle. [blue: V_{OUT} , red: V_{FB} , green: V_{DAC}]

To address this issue, the trimming frequency was intentionally reduced, limiting the update rate of the controller to one operation every four clock cycles. This approach allows the analog loop sufficient time to respond to each DAC correction before a new trimming decision is taken. As a result, the effective reaction speed of the digital loop becomes comparable to that of the analog loop, improving the stability and robustness of the overall

compensation process.

Therefore, the adopted solution can be interpreted as a simple synchronization mechanism between the analog and digital domains, ensuring that each correction step is applied only after the system has adequately settled to its new operating condition.

The implemented algorithm can also be interpreted as a simple digital servo loop. By continuously comparing the measured value with the stored target and updating the DAC code by one LSB at each iteration, the system progressively converges toward the desired operating condition while maintaining a low implementation complexity and a robust behaviour over process and temperature variations.

5.5 R2R DAC Implementation

An R-2R Digital-to-Analog Converter (DAC) [3] is a widely adopted architecture used to convert a digital code into a proportional analog voltage. Its operation relies on a resistor ladder composed exclusively of two resistance values, namely R and $2R$, which simplifies the implementation and guarantees good matching properties. The digital input bits control a network of switches that selectively connect the ladder nodes to the reference voltage or ground, generating an analog output proportional to the applied digital code.

One of the main advantages of the R-2R architecture is its scalability, since the same resistor network can be extended to higher resolutions without requiring additional resistor values. Furthermore, its relatively compact area and straightforward integration make it particularly suitable for digitally-assisted analog systems.

In the proposed compensation loop, the R-2R DAC is used to generate the correction voltage required to compensate for the offset and temperature-induced variations of the error amplifier. The DAC output is continuously updated by the digital trimming controller according to the information provided by the SAR ADC, forming a closed-loop calibration system.

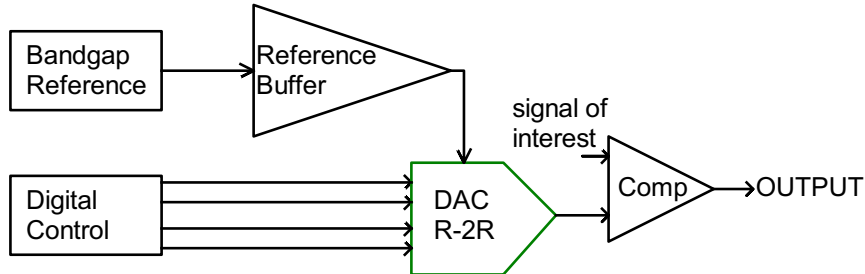


Figure 5.6: DAC R-2R architecture.

The implementation [Figure 5.6] of the R-2R DAC was considerably simpler compared to the SAR ADC integration. According to the integration guide, the DAC requires only a limited number of control and interface signals, making its insertion into the proposed architecture relatively straightforward. Once the reference voltage and the digital input code were properly connected, the block immediately provided the desired analog correction voltage without requiring complex configuration procedures, startup sequences, or calibration mechanisms.

As a consequence, the implementation effort associated with the DAC was mainly focused on defining the correct digital code mapping and on selecting the most suitable resolution for the trimming loop. In contrast to the ADC, no additional configuration or control logic was required, allowing a rapid and robust integration within the overall compensation architecture.

5.6 System Solution Operation

Now that the system-level solution has been fully integrated, the correct operation of the implementation must be verified. For a target output voltage of 3.3 V, the system is expected to converge to a feedback voltage V_{FB} of 412.5 mV.

It should be noted that the achievable accuracy is limited by the intrinsic quantization error introduced by the finite resolution of the R-2R DAC. As a result, the ideal value of 412.5 mV cannot be generated exactly. The closest available DAC code is 683, corresponding to a V_{DAC} of 416.8 mV, which translates into a V_{FB} of approximately 412.7 mV due to the 4 mV offset introduced. The adjacent lower DAC code would instead produce a V_{FB} of around 412.2 mV, resulting in a larger absolute error.

With a DAC code of 683, the regulated output voltage converges to 3.3018 V Figure 5.7. This corresponds to a feedback voltage error of approximately 225 μ V with respect to the ideal target, corresponding to 0.0545% accuracy, which falls within the theoretical quantization limit of $\pm\text{LSB}/2$. Therefore, the obtained result is fully consistent with the expected accuracy of the digital trimming system.

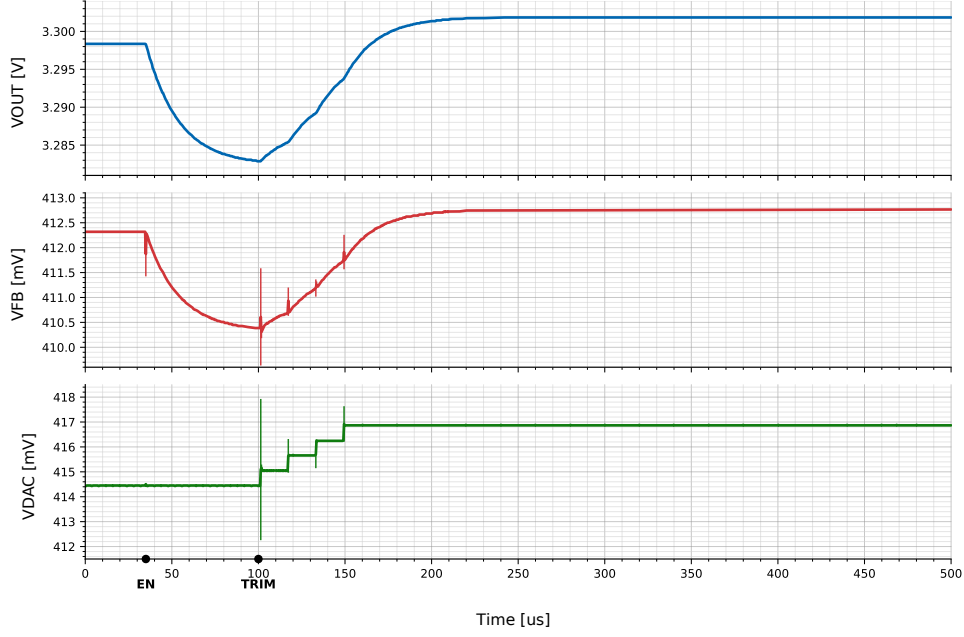


Figure 5.7: Local system solution transient without kickback noise. [blue: V_{OUT} , red: V_{FB} , green: V_{DAC}]

In addition, to improve the readability of the waveforms, the kickback effect introduced by the ADC on the feedback node was intentionally removed by inserting an ideal unity-gain voltage-controlled voltage source (VCVS). In this analysis, the objective is not to provide a realistic implementation of such a buffer, but rather to isolate the behavior of the regulation system and obtain cleaner waveforms for visualization purposes. Therefore, the adopted VCVS should be regarded only as an ideal observation buffer used to enhance the clarity of the reported results.

5.7 Conclusions

In conclusion, the system-level offset compensation approach based on a 13-bit SAR ADC and an 11-bit R-2R DAC proved to be an effective solution for mitigating the error amplifier offset without modifying the original analog cell.

The implemented trimming loop achieved an ideal trimming accuracy of approximately $\pm \text{LSB}/2 = 305 \text{ uV}$, which is comparable to the accuracy obtained through the device-level optimization of the error amplifier. The main advantage of this approach is that the gain stage characteristics remain unchanged, preserving the bandwidth, phase margin, and slew rate of the original design. This allows the offset correction to be decoupled from the analog optimization process and provides greater design flexibility. Really

important note is the non-dependence on the Bandgap drift in temperature. The Bandgap tension is commonly distributed at every block of the system, so a movement of it is seen in every point of the loop, such that the correction is not affected by this additional error.

The main drawback is the additional silicon area required by the ADC, DAC, and digital control logic.

Therefore, while the analog optimization approach offers a more compact implementation, the digitally-assisted solution provides a highly effective and scalable method for offset reduction, making it particularly attractive when preserving the original amplifier performance is a primary design objective.

Chapter 6

Top-Level Validation

After validating the proposed compensation technique at block level, the complete system solution is integrated into the ARM architecture in order to perform top-level simulations and verify its correct operation under realistic working conditions.

The servo loop employed during the validation phase is intentionally removed, as it was only used to emulate the trimming operations performed during testing. Consequently, the following simulations aim to verify whether the proposed compensation strategy can operate autonomously within the complete ARM architecture and maintain the desired converter performance during normal operation.

The test methodology remains unchanged with respect to the previous analyses. An additional offset is intentionally introduced into the system, and the ability of the compensation technique to reject the temperature drift and preserve the target output voltage of 3.3 V is evaluated. These simulations therefore provide a final validation of the proposed approach at the full system level.

6.1 Top-Level Architecture

As a first step, a dedicated symbol containing the entire drift compensation chain is created. This block includes the 13-bit SAR ADC, the digital control logic implemented in Verilog, and the 11-bit R-2R DAC together with the decoder required to manage the most significant bits.

Once completed, the symbol ['TRIMMING BLOCK'] is integrated within the Control Front End architecture Figure 6.1.

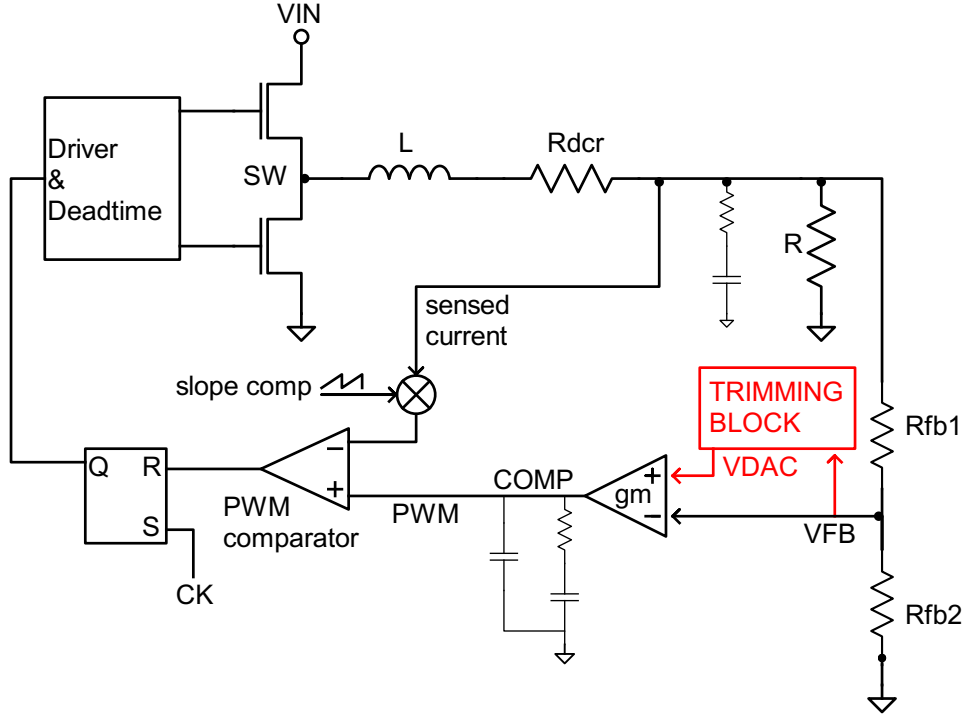


Figure 6.1: Top-level system solution implementation

More specifically, it is inserted in the signal path between the voltage generated by the resistive feedback divider and the reference voltage used by the error amplifier. In this way, the compensation system can dynamically adjust the effective reference seen by the amplifier, counteracting the displacement of the output voltage caused by the temperature-dependent offset drift of the error amplifier.

The resulting architecture allows the proposed digital compensation technique to operate transparently within the regulation loop, providing an automatic correction mechanism capable of preserving the desired output voltage despite variations induced by temperature, without requiring any modification to the main analog control loop.

6.2 Simulation Setup

The top-level simulation setup requires a careful definition of every parameter involved in the system startup sequence. Particular attention has been dedicated to the sizing of passive components, such as the output capacitor, and to the timing ramps applied to the various control signals. These choices are necessary to guarantee a correct power-up sequence and to avoid undesired behaviors caused by transient conditions, invalid measurements, or internal nodes that have not yet reached their nominal operating point.

Special attention has also been devoted to the implementation of the OTP initialization mechanism. During the previous validation phase, the DAC code was directly imposed through the test mode available in the Verilog model. In the final top-level implementation, however, the same information is provided through an OTP memory, thus reproducing as closely as possible the behavior of the actual ARM device and ensuring a realistic validation environment for the proposed compensation technique.

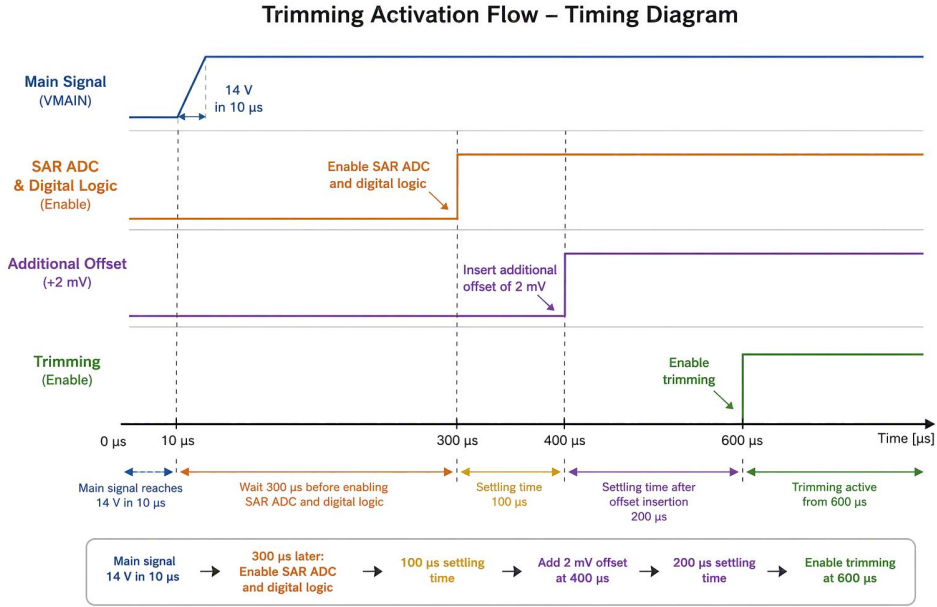


Figure 6.2: Timing flowchart of the top level trimming process.

The startup sequence has been carefully designed to guarantee stable operation of both the analog and digital sections. As shown in Figure 6.2 The main enable signal ramps to 14 V within 10 us. After 300 us from the global power-up event, the digital compensation loop is enabled by activating the SAR ADC and the remaining digital control chain. An additional settling interval of 100 us is then introduced to allow all the blocks to reach their nominal operating conditions. During this phase, the compensation loop remains open and the DAC output is forced to the OTP-stored code, therefore maintaining the system in the ideal trimmed condition.

At 400 us an additional offset (2 mV) is intentionally injected into the error amplifier in order to emulate the effects of the offset temperature drift. The system is then allowed to settle for a further 200 us, ensuring that the perturbation has fully propagated throughout the regulation loop. Finally, at 600 us the trimming operation is enabled and the digital compensation loop is closed. At this point, the OTP code is no longer used and the

correction mechanism begins operating autonomously. The loop compares the measured output condition against the target value previously stored during the initialization phase and continuously updates the DAC code in order to compensate for the generated offset error.

The overall transient simulation duration is set to 5 ms. It should be noted that the SAR ADC normally requires an initial calibration phase lasting approximately 100 ms. Simulating the entire calibration interval would significantly increase the computational cost without providing additional information relevant to the present analysis. For this reason, the calibration procedure has been intentionally bypassed through a dedicated configuration of the ADC block, allowing the simulations to focus exclusively on the steady-state behavior of the compensation system.

6.3 Nominal Results

As expected, the behavior of the overall architecture changes slightly once the trimming system is integrated into the top-level design.

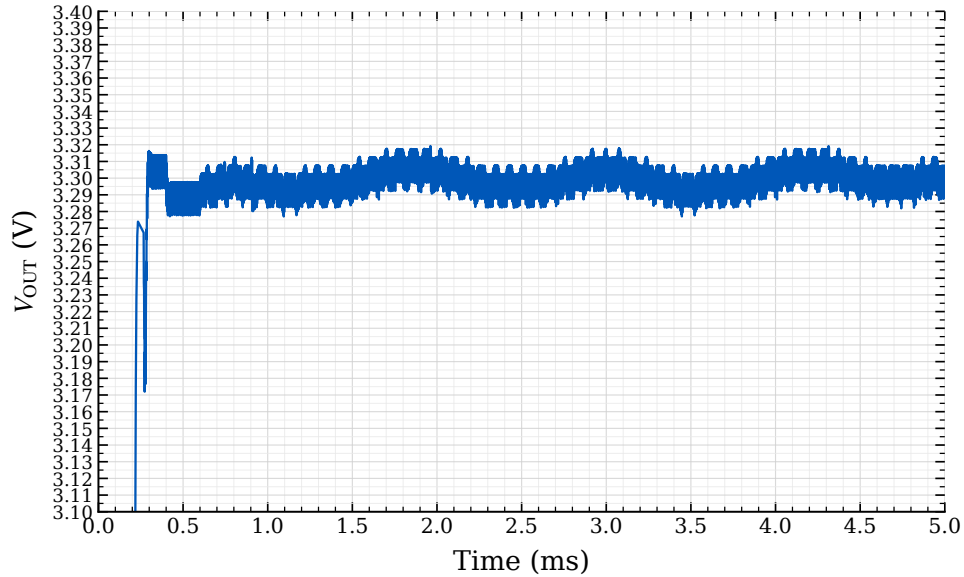


Figure 6.3: Top-level final implementation V_{OUT} transient.

The obtained plot Figure 6.3, where the error introduced at 400 us and the enabling of the trimming algorithm at 600 us can be clearly observed, presents V_{OUT} with a steady-state average of 3.302 V, which is very close to the value observed in the local-level simulations (Figure 5.7). The resulting deviation with respect to the scaled target value is 250 uV, corresponding to an error of 0.0606% with respect to the desired 3.3 V. This result is fully

comparable to the 0.057% variation achieved through the optimization of the gm-stage cell [Table 4.1].

The small oscillation of V_{OUT} around the target voltage can be observed, precisely the oscillation is ± 3 LSB around the desired value. This behavior is mainly related to the trimming update rate and can be further mitigated by reducing the trimming clock frequency, which is currently set to one quarter of the SAR ADC clock frequency.

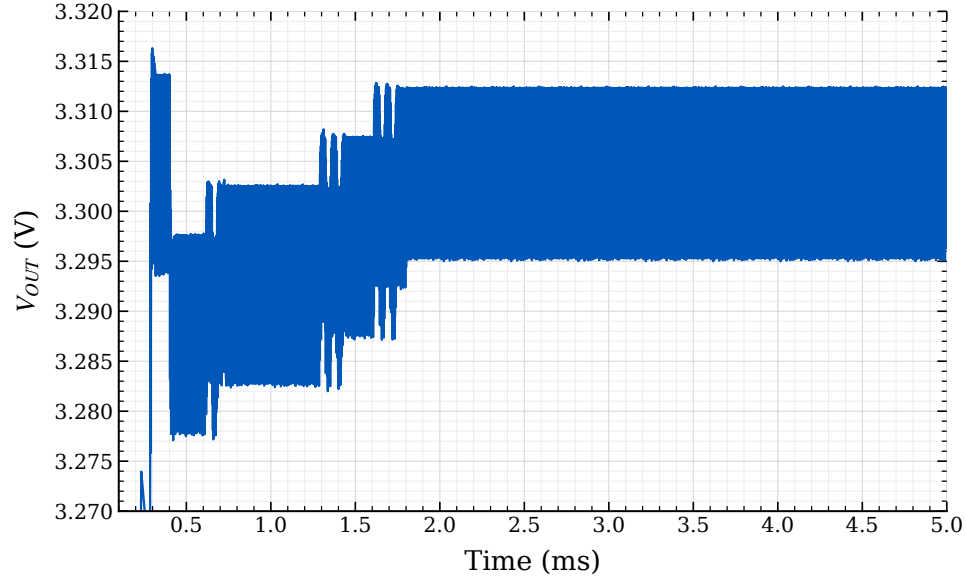


Figure 6.4: Top-level final implementation zoomed-in V_{OUT} transient.

As shown in Figure 6.4, where the Verilog code implemented a trimming over sixteen SAR ADC clocks, the oscillation is reduced and the steady-state value of V_{OUT} corresponds to the expected one.

Chapter 7

Conclusions

7.1 Summary

This thesis investigated the problem of offset voltage and thermal drift in the voltage loop of a precision current-mode buck converter. An initial system-level analysis identified the error amplifier as the dominant contributor to output voltage drift over temperature, while the contributions of the resistive divider and reference buffer were found to be negligible. The work was then divided into two complementary approaches: transistor-level optimization of the existing amplifier architecture and digitally-assisted offset compensation through an ADC-DAC calibration loop.

7.2 Performed Work

The first part of this work was the identification of the main transistor-level sources of offset temperature drift through mismatch contribution analysis and mirror idealization techniques. The analysis demonstrated that the high-compliance mirror and the cascode/output mirror represented the most critical contributors to the thermal behavior of the amplifier.

Based on these observations, a sizing optimization procedure was developed. The final implementation reduced the offset temperature coefficient from approximately 0.145% to 0.057% while preserving acceptable bandwidth and stability characteristics. Considering the total output-voltage accuracy window of $\pm 0.8\%$, the error-amplifier thermal drift initially consumed about 9.1% $((0.145\%/2)/0.8)$ of the available accuracy budget. Following the proposed optimization, its contribution was reduced to approximately 3.6% $((0.057\%/2)/0.8)$, demonstrating a significant improvement in thermal stability.

The second part was the development of a digitally-assisted compensation architecture based on a SAR ADC, an R-2R DAC, and dedicated trimming logic. This solution enabled automatic estimation and correction

of the residual offset at system level, with an accuracy of 0.06%, without modifying the original amplifier topology and without affecting the overall voltage-loop dynamics. In this case the budget consumption was reduced to 3.75% $((0.06\%/2)/0.8)$ of the total $\pm 0.8\%$ budget.

Although the original converter was already compliant with the specified $\pm 0.8\%$ output-voltage accuracy requirement, the proposed optimization significantly reduced the contribution of the error amplifier to the overall error budget. More specifically, the thermal-drift induced output-voltage error was reduced from 0.145% to 0.057%, corresponding to a reduction of approximately 60.7%. Considering the total accuracy window of 1.6%, the fraction of the budget consumed by the error amplifier decreased from approximately 9.1% to 3.6%. This result provides additional margin for the remaining error sources while preserving the original converter architecture and avoiding the use of more complex offset-cancellation techniques such as chopper stabilization or auto-zeroing.

Assuming a worst-case scenario in which the converter operates exactly at the $\pm 0.8\%$ specification limit, the achieved reduction would correspond to an equivalent accuracy improvement from approximately $\pm 0.8\%$ to $\pm 0.71\%$. Since the original design already satisfied the requirement with some residual margin, the actual achievable accuracy is expected to be even better, potentially falling below the $\pm 0.7\%$ level.

This result highlights the effectiveness of the proposed approach in pushing the converter performance beyond the original product target while maintaining a limited implementation overhead, without using complex offset-cancellation techniques. Finally, it is worth noting again that an output-voltage accuracy of $\pm 0.8\%$ is currently representative of the performance level targeted by several state-of-the-art automotive buck converters, as mentioned in the Thesis Objectives chapter.

In some of the state-of-the-art automotive buck converters, such as the Texas Instruments TPS6288x-Q1 family, achieve an output-voltage accuracy as low as $\pm 0.5\%$ [17]. However, these devices are intended for low-input-voltage point-to-load applications, with an operating input range limited to approximately 2.7 V to 6 V. In contrast, the converter investigated in this work supports input voltages up to 36 V, enabling direct connection to automotive power nets without requiring additional pre-regulation stages. Therefore, the achieved accuracy improvement is particularly significant considering the wider operating range and the associated design challenges.

7.3 Solutions Comparison

Aspect	Analog Optimization	Digital Compensation
Thermal drift reduction	Excellent	Excellent
Silicon area	Excellent	Moderate
Impact on existing OTA	Limited	None
Impact on control loop bandwidth	Limited	None
Verification effort	Medium	High
Design complexity	Medium	High
Flexibility after silicon	Limited	Excellent

Table 7.1: Solutions comparison

As shown in Table. 7.1, the analog solution provides a low-cost and low-overhead improvement that can be integrated directly into an existing design. On the other hand, the digital calibration loop achieves a significantly higher compensation capability because it acts on the final system error rather than on a single internal error source. The price to pay is the increased implementation complexity and the requirement for additional mixed-signal circuitry.

7.4 Future Developments

Several extensions of the proposed work can be investigated in future developments.

- **Full silicon implementation of the ADC-DAC trimming loop**
- **Higher-resolution DAC architectures**
- **Comparison with chopper-stabilized and auto-zero techniques**

7.5 Conclusions

Overall, the results demonstrate that both transistor-level optimization and digitally-assisted calibration represent excellent solutions for improving the accuracy in temperature of precision error amplifiers. While the first approach offers a simple and area-efficient improvement, the second provides a more powerful compensation mechanism capable of correcting the residual error of the entire feedback path. Moreover, unlike chopper stabilization and

auto-zeroing techniques, which modify the signal path of the error amplifier and therefore affect the converter loop dynamics, the proposed system solution operates as a low-bandwidth background calibration loop. The trimming algorithm only adjusts the offset compensation code through a DAC, while leaving the error amplifier architecture, compensation network, gain and bandwidth unchanged. As a result, the main regulation loop is not impacted and no redesign of the converter compensation is required.

The methodologies presented in this thesis provide practical design guidelines for future high-precision analog and mixed-signal integrated circuits, where increasing accuracy requirements must be achieved while maintaining compatibility with existing architectures and design constraints.

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