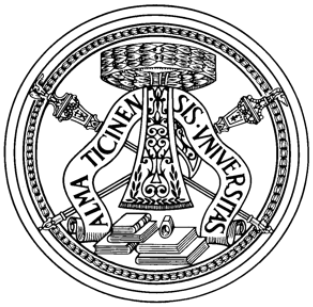


UNIVERSITÀ DEGLI STUDI DI PAVIA

FACULTY OF ENGINEERING

Department of Electrical, Computer and Biomedical Engineering

Master's degree in Electronic Engineering

Design and Implementation of an Analog Normalization System for Real-Time Monitoring and Adaptive Control of DC-DC Buck Converters Using Neural Networks

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Progettazione e implementazione di un sistema di normalizzazione analogico per il monitoraggio in tempo reale e il controllo adattivo di un convertitore DC-DC Buck mediante reti neurali

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Abstract

Sommario-Italiano

Nell'elettronica di potenza moderna, garantire l'affidabilità e l'efficienza dei convertitori DC-DC è cruciale, particolarmente nelle applicazioni che richiedono stabilità a lungo termine e manutenzione predittiva. Questa ricerca presenta la progettazione e l'implementazione di un normalizzatore analogico per l'acquisizione di dati in tempo reale in un sistema convertitore buck. Il normalizzatore elabora parametri elettrici chiave come tensione e corrente di uscita prima della loro conversione in forma digitale per ulteriori analisi, mappando efficacemente variazioni minime del segnale (anche di soli 4mV picco-picco) in un intervallo adatto all'elaborazione digitale senza richiedere convertitori analogico-digitali ad alta risoluzione.

Un sistema diagnostico basato su rete neurale viene quindi impiegato per stimare parametri critici legati all'invecchiamento, inclusi la resistenza serie equivalente (ESR), la resistenza di accensione del MOSFET (RDSON), il degrado del condensatore e le variazioni dell'induttore. Sfruttando i dati dei sensori in tempo reale, il sistema fornisce previsioni precise riguardo l'invecchiamento dei componenti e potenziali guasti. Inoltre, è integrato un sistema di flag diagnostici per indicare anomalie e necessità di manutenzione.

Il framework proposto combina normalizzazione analogica basata su hardware, attraverso approcci sia semplici a tre stadi che avanzati HPF+LPF, elaborazione digitale e analisi guidata dall'intelligenza artificiale, fornendo una strategia completa di monitoraggio in tempo reale e auto-ottimizzazione per i convertitori DC-DC. Questo consente significative riduzioni dell'area di silicio mantenendo un'elevata precisione per le applicazioni di AI edge nell'elettronica di potenza.

Abstract-English

In modern power electronics, ensuring the reliability and efficiency of DC-DC converters is crucial, particularly in applications requiring long-term stability and predictive maintenance. This research presents the design and implementation of an analog normalizer for real-time data acquisition in a buck converter system. The normalizer processes key electrical parameters such as output voltage and current before their conversion into digital form for further analysis, effectively mapping minute signal variations (as small as 4mV peak-to-peak) to a suitable range for digital processing without requiring high-resolution ADCs.

A neural network-based diagnostic system is then employed to estimate critical aging-related parameters, including equivalent series resistance (ESR), MOSFET on-resistance (RDSON), capacitor degradation, and inductor variations. By leveraging real-time sensor data, the system provides precise predictions regarding component aging and potential failures. Additionally, a diagnostic flag system is integrated to indicate anomalies and maintenance needs.

The proposed framework combines hardware-based analog normalization through both simple three-stage and advanced HPF+LPF approaches, digital processing, and AI-driven analysis, providing a comprehensive real-time monitoring and self-optimization strategy for DC-DC converters. This enables significant reductions in silicon area while maintaining high accuracy for edge AI applications in power electronics

INTRODUCTION

Power converters are fundamental components in modern electronics, playing a crucial role in efficient power management, voltage conversion, and regulation across a wide range of edge applications. There is no doubt that their performance directly influences the overall system's efficiency, lifespan, and safety, making reliability a critical aspect of their design. This is especially true in safety-critical applications, such as autonomous vehicles, where power converters must operate with the highest levels of dependability to ensure uninterrupted functionality. For instance, in driverless automobiles, a failure in power conversion can compromise the entire control system, making robust and precise power regulation indispensable.

In this context, a system based on a quantized fully connected tiny neural network has been studied as a potential approach to improving power converter reliability. However, this thesis does not focus on the implementation details of the neural network itself. Instead, the emphasis is placed on designing an *analog normalizer*, which enables continuous normalization of data in the analog domain before conversion to digital, eliminating the need for digital preprocessing.

Two key constraints associated with the tiny neural network motivate this approach:

1. **Cost and Size Limitations:** Since the neural network is designed to operate with a low bit-width, implementing data normalization digitally would require high-resolution analog-to-digital converters (ADCs) to capture minute signal variations. The issue is not with the digital processing elements themselves, which occupy negligible silicon area, but rather with the substantial area requirements of the high-resolution ADCs and the corresponding high-bit-width input layers needed in the neural network to process such fine-grained data. This contradicts the lightweight nature required for our implementation.

2. **Accuracy Constraints in Low-Bit Digital Systems:** A major drawback of performing normalization in the digital domain is the introduction of *quantization errors*, which become particularly significant when working with low-bit representations. In our specific case, the dataset and system under study require processing the output ripple voltage of a buck converter with a precision as fine as *4 millivolts peak-to-peak* on top of a 5-volt DC level.

To illustrate the magnitude of this challenge quantitatively, consider the following analysis: With a 10-bit ADC and 2V full scale voltage, the quantization step becomes $\frac{2V}{2^{10}}$ =1.953 mV, which would allow only about 2 steps to represent 4 mV signal, yielding up to 50% quantization error. Such large error is unacceptable for reliable system characterization and would severely compromise the neural network's ability to detect subtle changes in converter performance.

Given such stringent accuracy requirements, even minor quantization errors can lead to substantial deviations in system performance, making digital normalization unsuitable for this application.

Without an analog normalizer, differentiating input analog data with variations as minimal as 4 mV peak-to-peak would necessitate an analog-to-digital converter (ADC) with at least *16-bit resolution*. Such high-resolution ADCs impose substantial silicon area requirements compared to the total system, which becomes particularly problematic when considering that our neural network implementation cannot exceed *10-bit precision* while maintaining reasonable area occupation. The elegant solution to this dilemma lies in analog normalization, which effectively utilizes the *full-scale range* of the ADC input. Instead of resolving minute 4 mV peak-to-peak variations directly, the analog normalizer maps these small variations to a *2-volt peak-to-peak range*, thereby significantly enhancing the effective resolution of subsequent digital processing stages.

To overcome these challenges, we propose a fully analog normalizer, which continuously adjusts the data in real time without introducing quantization errors before the data enters the digital domain for further processing by the neural network.

This thesis is organized into several chapters, each addressing specific aspects of the analog normalization system for DC-DC buck converters. Following this introduction, Chapter 1 explores the foundations of neural networks and their application in diagnostic systems for power converters, establishing the architectural framework and system requirements. Chapter 2 delves into hardware-based analog normalization techniques, examining various approaches including min-max normalization and the novel HPF+LPF solution, with detailed mathematical formulations and circuit implementations. Chapter 3 presents the comprehensive system board development, describing the practical realization of the proposed normalization approaches through discrete component implementation and detailed circuit design. Finally, the thesis concludes with a summary of findings and outlines directions for future research, with immediate next steps focused on utilizing the developed testing board for experimental validation and performance measurements. Following successful validation, subsequent work will explore silicon implementation considerations and potential optimizations for the proposed normalization techniques.

By leveraging analog signal processing techniques, this approach ensures high precision and affordable size of the total system, ultimately leading to a more efficient and reliable power management system.

CHAPTER 1

Neural Networks

The human brain comprises approximately 100 billion interconnected neurons, which function as the fundamental cellular units responsible for information processing and transmission. These specialized cells communicate with one another through electrochemical signaling mechanisms, creating intricate neural networks that enable complex cognitive functions.

Artificial Neural Networks (ANNs) were conceptualized based on the principles inspired by the human brain's information processing capabilities. This revolutionary computational paradigm was initially introduced to the scientific community in 1943 by Warren McCulloch and Walter Pitts, who proposed a mathematical model of neural networks that would form the foundation for future developments in this field. Their pioneering work established a framework that continues to influence contemporary neural network architectures.

In the decades following this initial conceptualization, ANNs have experienced widespread adoption across virtually every scientific discipline as powerful tool for addressing complex computational challenges. The versatility and efficacy of these systems have facilitated their integration into numerous domains where traditional algorithmic approaches proved insufficient.

Williams made significant contributions to this field by demonstrating the remarkable efficiency of machine learning algorithms. Through rigorous analysis and empirical validation, Williams established compelling evidence regarding the broad applicability of these computational techniques across diverse domains.

The evolutionary trajectory from biological inspiration to computational implementation represents a significant advancement in artificial intelligence, enabling increasingly sophisticated pattern recognition and decision-making capabilities that continue to transform numerous fields of human endeavor [1].

Having established the historical foundations and biological inspirations of neural networks, we now turn to examining their technical architecture and mathematical formulation in greater detail.

Neural Networks constitute an essential element of modern artificial intelligence systems. It is unequivocally established that neural networks are sophisticated computational structures comprising interconnected processing units, referred to as neurons, which are systematically organized into multiple layers. Each neuron operates by receiving input signals, processing this information through a designated activation function, and subsequently generating an output signal. Through the methodical process of training on diverse datasets, neural networks develop the capability to recognize and learn complex patterns and relationships within data. This acquired knowledge enables them to accurately forecast outcomes, efficiently categorize information, and execute a comprehensive range of significant computational tasks with remarkable precision.

The foundational component of a neural network exists as a Perceptron, which represents a rudimentary, single-layer computational structure specifically engineered to address problems that exhibit linear separability. This Perceptron functions by computing a weighted sum of its inputs and subsequently applying a threshold-based activation function to produce a binary output, as formulated in Eq. (1.1), effectively creating a decision boundary in the input space.

The mathematical formulation of a perceptron can be expressed as follows:

$$y = f\left(\sum_{i=1}^{n} w_i x_i + b\right) \tag{1.1}$$

Where:

- x_i represents the input vector elements $(x_1, x_2, \ldots, x_n)$

- w_i represents the corresponding weight vector elements $(w_1, w_2, \dots, w_n)$
- b is the bias term (sometimes denoted as w_0 with a corresponding input $x_0 = 1$)
- $\sum_{i=1}^{n} w_i x_i + b$ calculates the weighted sum of inputs plus bias
- f is the activation function that determines the output

For the classical perceptron model, the activation function is typically a step function which can be defined as:

$$\text{Step function (z)} = \begin{cases} 1, & if \ \ z \geq \theta \\ 0, & if \ \ z < \theta \end{cases} \tag{1.2}$$

Where θ is the threshold value. The Eq. (1.2) effectively compares the weighted summation against a threshold value to determine whether the perceptron "fires" (activates) or not, thereby implementing the decision boundary in the input space that characterizes the perceptron's operation in classification tasks.

It is worth noting that when these elementary perceptrons are methodically arranged into hierarchical multilayer configurations with the strategic integration of nonlinear activation functions such as sigmoid, hyperbolic tangent (tanh), or Rectified Linear Unit (ReLU), the resultant multilayer neural network architectures acquire substantial computational capabilities. The incorporation of these nonlinear elements is crucial, as they introduce the mathematical capacity to approximate arbitrary functions through composition, a property formalized in the Universal Approximation Theorem.

Indeed, these sophisticated structures demonstrate remarkable proficiency in executing intricate computational tasks and effectively discerning nonlinear patterns embedded within the data they process. The hierarchical nature of information processing enables the extraction of increasingly abstract representations across successive layers—lower layers typically detect basic features (e.g., edges or textures in image processing), while deeper layers combine these elementary features to represent more complex concepts.

The transformation from simple perceptrons to complex multilayer networks fundamentally enhances the analytical capacity and functional versatility of these computational systems, enabling them to address progressively more challenging problems in various domains of application. This evolutionary progression in network architecture has been accompanied by corresponding advancements in training

methodologies, notably the backpropagation algorithm, which facilitates efficient parameter optimization through gradient-based techniques, thereby allowing these networks to learn from extensive datasets with millions of parameters [2] [3] [4].

1.1 Neural Network-Based Diagnostic System

Neural networks have demonstrated remarkable versatility and efficacy across a diverse spectrum of application domains. In the field of computer vision, these computational structures excel at image recognition tasks, enabling automated identification of objects, faces, and patterns with unprecedented accuracy. Similarly, in audio processing, neural networks have revolutionized speech recognition systems, facilitating more natural human-computer interactions. The domain of natural language processing has been transformed through neural network implementations that comprehend, generate, and translate human language with increasing sophistication.

In healthcare, neural networks contribute significantly to the medical diagnostics by analyzing complex clinical data and identifying patterns indicative of various pathologies, thereby augmenting the diagnostic capabilities of healthcare professionals. The transportation sector has witnessed substantial advancements through the integration of neural networks in autonomous vehicle systems, where these networks process and interpret vast amounts of sensor data to navigate complex environments safely and efficiently.

Financial institutions increasingly rely on neural networks for predictive analytics and forecasting, leveraging these systems to identify market trends, assess investment opportunities, and mitigate risks with greater precision.

In the field of electronics, particularly in power management systems, neural networks have emerged as powerful tools for enhancing the performance and reliability of DC-DC converters. These converters, fundamental components in numerous electronic devices, benefit significantly from neural network integration for predictive maintenance and adaptive control [7] [8]. A sophisticated implementation involves training neural networks with operational data from DC-DC converters to accurately predict component aging phenomena, such as capacitor degradation and switching element wear. By analyzing subtle changes in converter parameters—including output ripple characteristics, switching transients, and thermal signatures—these networks can

forecast impending failures before conventional detection methods identify anomalies. Furthermore, neural networks enable dynamic adjustment of PID (Proportional-Integral-Derivative) controller coefficients in response to both aging-related parameter drift and varying load conditions [9]. This adaptive control methodology substantially enhances conversion efficiency across the operational lifespan of the device, resulting in reduced power losses, extended component longevity, and improved overall system reliability.

The exceptional capacity of neural networks to extract meaningful patterns from extensive datasets, coupled with their ability to generalize these learned patterns to novel scenarios, renders them extraordinarily powerful computational tools for addressing multifaceted problems that have historically resisted conventional algorithmic solutions.

Indeed, neural networks represent a transformative technological paradigm that continues to expand the boundaries of computational problem-solving across scientific, industrial, and commercial domains [2] [5] [6].

The Neural network model discussed in this context represents a fully connected neural network architecture, characterized by its comprehensive interconnections between neurons across adjacent layers. This particular network paradigm operates fundamentally on the principles of supervised learning methodologies. Within the supervised learning framework, the training process is conducted using a dataset comprised of explicitly defined examples. These examples are meticulously structured to demonstrate the precise correspondence between input patterns and their associated correct output responses.

In this supervised learning approach, the neural network undergoes an iterative training procedure wherein it processes input data, generates predictions, and subsequently adjusts its internal parameters based on the discrepancy between its predicted outputs and the ground truth values provided in the training examples.

The fully connected architecture ensures that each neuron in a given layer maintains connections with every neuron in the subsequent layer, facilitating comprehensive information flow and pattern recognition capabilities. This interconnected structure enables the network to learn complex, hierarchical representations of the input data across its multiple layers. Through this process, the network progressively develops the

capacity to generalize from training examples to accurately process previously unseen inputs, thereby demonstrating its ability to extract and apply learned patterns to novel situations within its domain of application [4].

1.2 ARCHITECTURE

Neural networks are comprised of a series of interconnected computational units, formally designated as neurons, which perform the essential function of data processing. The organizational framework of a neural network, technically referred to as its Architecture, delineates the systematic arrangement of these neurons into distinct functional layers. The architectural design of neural networks fundamentally determines their information processing capabilities and operational characteristics.

The structural configuration of a neural network typically consists of multiple layers, each serving specific computational purposes within the overall system. These layers generally include an input layer that receives initial data, one or more intermediate hidden layers where complex pattern recognition and feature extraction processes occur, and an output layer that generates the final computational results. The precise number of layers, their respective sizes, and the specific connectivity patterns between neurons collectively define the network's architectural topology.

This architectural framework establishes the computational pathways through which information propagates during both the training phase and subsequent operational deployment. The topological design significantly influences crucial network properties, including its learning capacity, generalization capabilities, and computational efficiency. Modern neural network architectures exhibit considerable diversity, ranging from relatively simple feedforward configurations to highly sophisticated recurrent and convolutional structures, each optimized for specific classes of computational problems and application domains.

The systematic design of neural network architectures represents a critical aspect of their implementation, as it directly impacts their ability to effectively address complex pattern recognition tasks across various fields of application [2] [3].

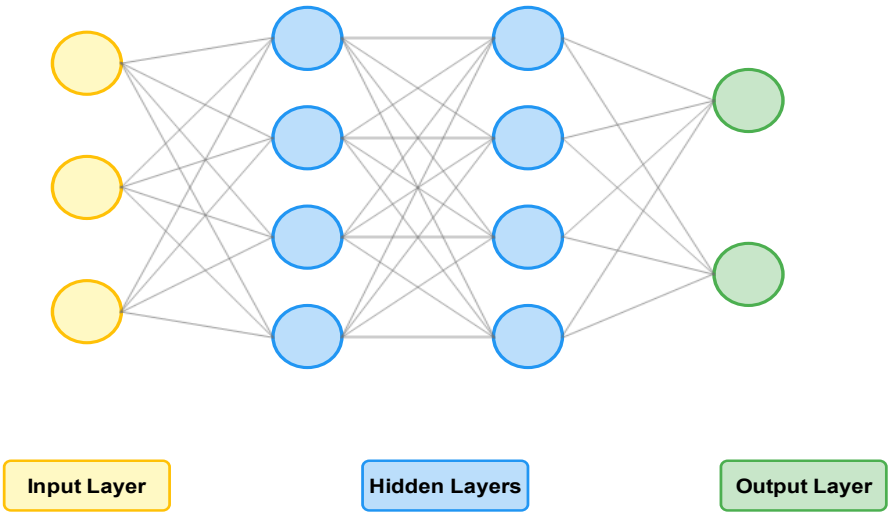


Fig. 1. Architecture of a Neural Network comprising an input layer, hidden layer, and an output layer, represented in orange, blue and green respectively.

The architecture of a neural network typically comprises a single input layer, followed by one or more hidden layers, and culminating in an output layer, as illustrated in Fig.1.

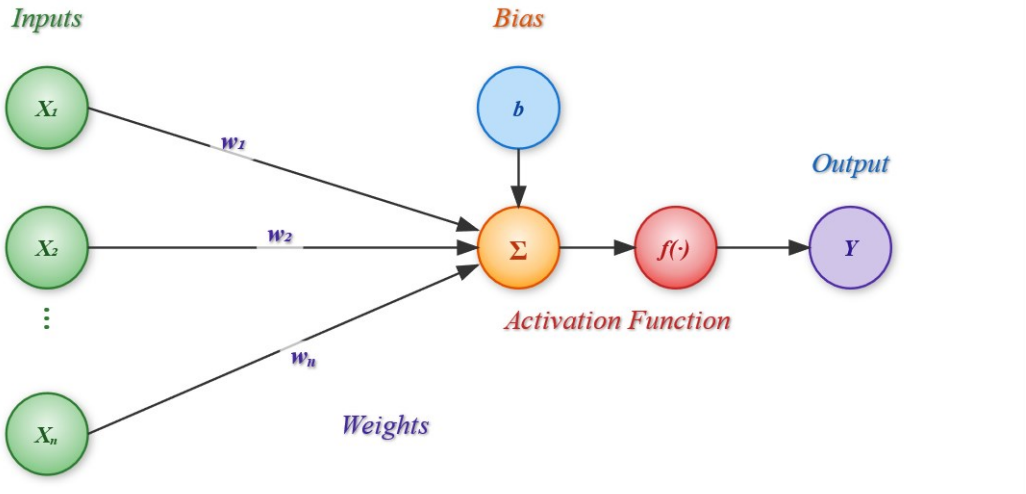


Fig. 2. Single Neuron

Fig. 2. provides a comprehensive mathematical representation of the operations occurring within an individual neuron situated in the hidden layer. It is indisputable that

neural networks are fundamentally built upon these computational units. In this representation, the variables $x_1, x_2, \ldots, x_n$ denote the input signals, while $w_1, w_2, \ldots, w_n$ correspond to the respective synaptic weights associated with each input signal, and the parameter b represents the bias value. Each neuron performs a computation wherein it evaluates the weighted summation of its inputs—a process that entails multiplying each input signal by its corresponding weight coefficient and subsequently incorporating the bias term. The resultant sum is then processed through an activation function, denoted as f(.), which generates an output Y.

This output subsequently serves as an input signal for neurons in the succeeding layer. The mathematical expression governing the output of a neuron can be formally articulated as:

$$f(x) = w_1 \cdot x_1 + w_2 x_2 + \cdots + w_n \cdot x_n + b = y \tag{1.3}$$

The Eq. (1.3), encapsulates the fundamental computational mechanism underlying neural information processing. The activation function introduces non-linearity into the system, which is essential for the network to learn complex patterns and representations from the input data [2].

Having established the fundamental architecture and operational principles of neural networks, the focus now shifts to the specific implementation developed for this research. This work employs a quantized neural network approach to achieve an optimal balance between computational capability and hardware efficiency. While traditional neural networks often utilize floating-point arithmetic that demands substantial computational resources, the implementation presented herein leverages integer-based quantization techniques to dramatically reduce the silicon footprint while maintaining acceptable levels of performance. This strategic optimization is particularly critical for edge computing applications where power constraints and silicon area limitations present significant design challenges. The following section details the architectural specifications and quantization methodology employed in this implementation.

1.2.1 Hardware-Optimized Neural Network Design

While traditional neural networks often utilize floating-point arithmetic (typically 32-bit or 64-bit precision), such implementations require substantial computational resources and silicon area. Floating-point operations necessitate complex hardware units for managing sign bits, exponents, and mantissas, along with specialized circuitry for normalization and rounding operations. The implementation of floating-point arithmetic in silicon demands significantly larger die area, consumes more power, and introduces greater computational latency compared to fixed-point or integer-based alternatives. Furthermore, the precision offered by floating-point arithmetic often exceeds what is practically necessary for many neural network applications, where studies have demonstrated that reduced numerical precision can maintain comparable inference accuracy while dramatically improving hardware efficiency. This observation forms the foundation for the quantized approach adopted in the present research [10] [11].

Neural Network Coded in QKeras® QAT deep learning framework, the required topology consisted of 8 inputs, a first and a second hidden layer with 20 neurons each and 5 output neurons. Compared to the previous study [9], the neural network was defined to target a tiny hardware digital implementation, by quantization of inputs, internal nodes, weights, bias and by representation of numeric values as signed integers instead of float32, which would make the silicon implementation too expensive. As described in Fig. 3., all hidden layers were defined by the QDense layer with 20 neurons. Weights and bias were coded as 8-bits signed vectors. The AF blocks represented activation layers, defined by the QActivation layer as ReLU and quantized to 16-bit vectors to include enough information from the accumulation of products in each neuron.

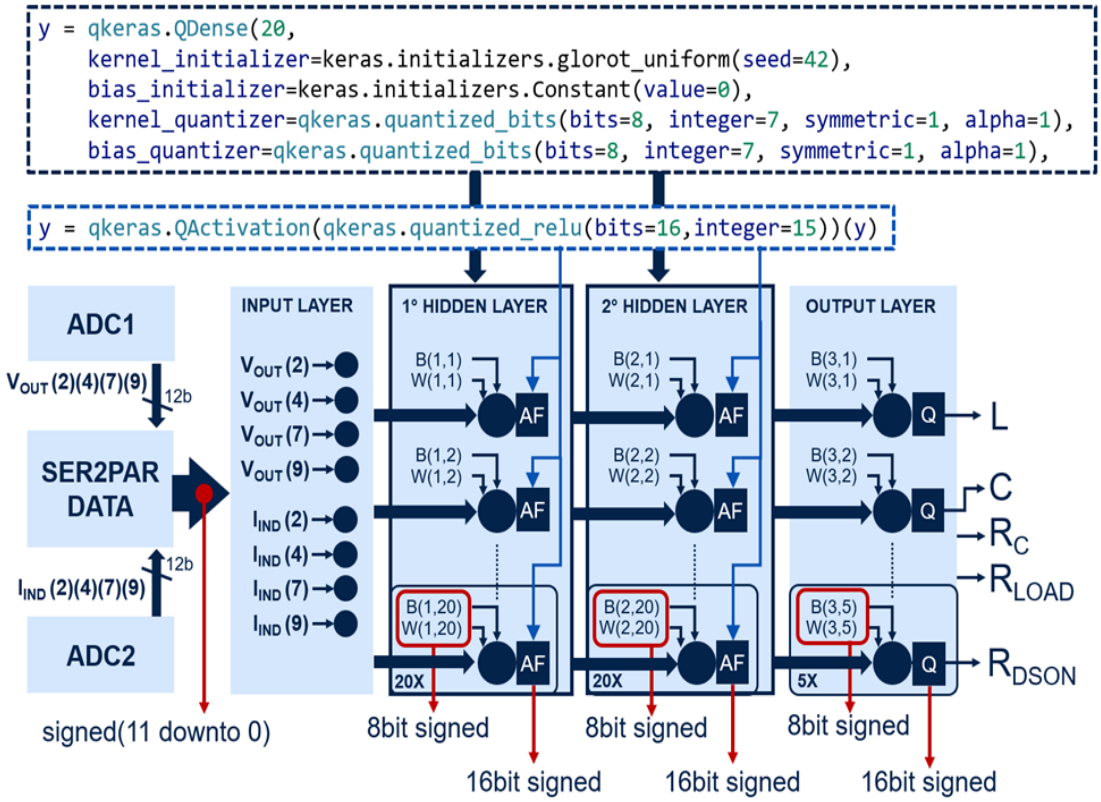


Fig. 3. Neural network topology description.

The Q blocks performed a simple quantization to 16-bit of the output using a pure linear activation function. The choices of ReLU and linear activation function were to achieve a hardware friendly implementation with an ad-hoc hardware digital circuit. The Eq. (1.4) defines the mean square error (MSE) between the training parameters K_1-K_n and target parameters K_1^I-K_n^I and represents the loss function of the neural network, used to evaluate the differences between ground truth and estimated data output. During the training operations, parameters K_1-K_n were defined as a function of the 4 samples of V_{OUT} and I_{IND} accordingly to weights *w* and bias *b* values.

$$\mathrm{MSE} = \frac{1}{n}\sum_{i=0}^{n}\ \sum_{j=0}^{m}(K_{ij} - K_{ij}^{I})^2 \qquad (1.4)$$

The gradient descent algorithm tried, for a desired number of epochs, to recursively identify the minimum of the loss function by updating *w* and *b*, until the loss function

reached an acceptable threshold. This behavior is described by the losses plot related to validation and training operations, shown in Fig. 4.

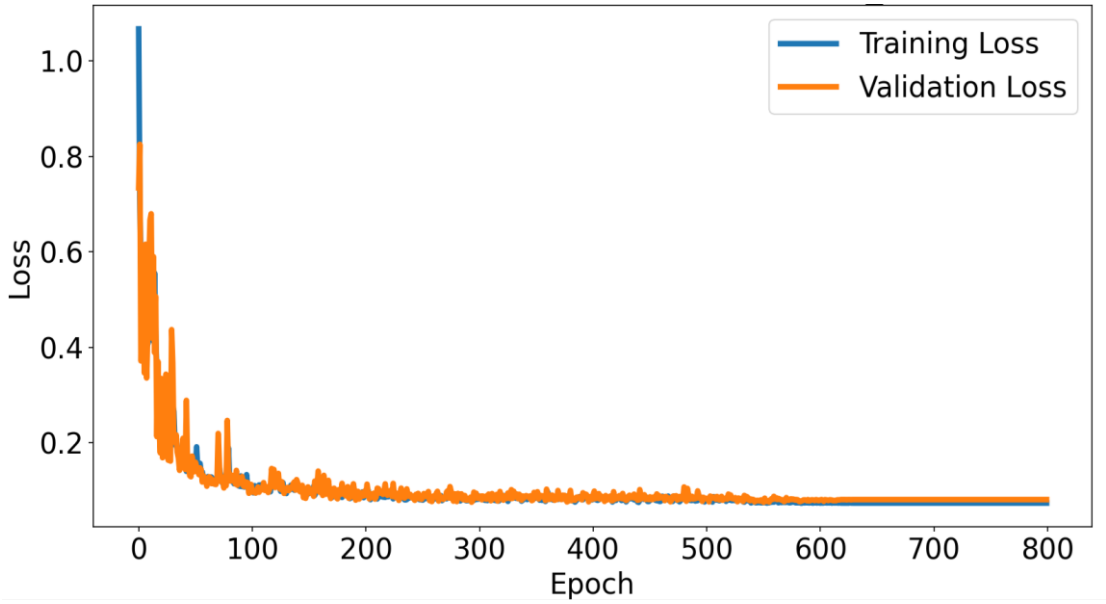


Fig. 4. Training and validation loss plots.

1.3 TARGET SYSTEM

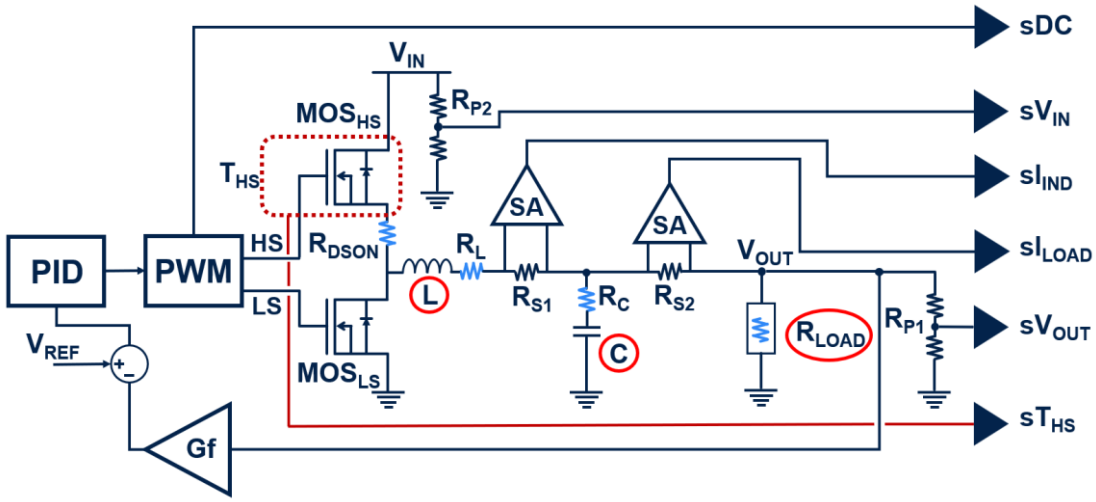


Fig. 5. DC-DC buck converter schematic and sensed signals.

This work considered a cheap DC-DC synchronous buck converter whose schematic is shown in Fig. 5. The output voltage regulation is implemented by a control loop that consists of a PID (Proportional, Integral, Derivative controller) that evaluates the error as the difference V_{OUT} - V_{REF} and properly tunes the duty cycle of the pulse width modulation signals, HS and LS, which complementary drive the gate of the high side and the low side power MOS (Metal Oxide Semiconductor) transistor. The conversion efficiency between input and output voltages, the control feedback loop stability, the output current and voltage stability, heavily depend on the highlighted red parameters in the circuit of Fig. 5. i.e., the main values of inductor L, capacitor C and resistive load R_{LOAD}. Non-optimal working points can occur when these values diverge from the nominal ones due to manufacturing tolerances, components aging, parasitic introduced by the PCB, degradation with temperature and operating time [1] [2] [3]. A real and physical estimation of these parameters makes it possible to tune the regulation feedback loop, recover previously mentioned undesired effects, preserve nominal performances and extend the life of the system. Indirect estimation of the blue elements of Fig. 5., i.e., the parasitic resistors of the capacitor R_C, inductor R_L and the R_{HDSON} of the MOS, can be used to evaluate the degradation of the components, make aware of some issues and prevent complete system failure [12]. For example, when an anomalous increase of R_{DSON} is detected, the system can accordingly decrease the voltage level V_{GS} of the signals HS and LS, managing to recover the variation, to extend components life and improve power efficiency. Since the coefficients of the PID controller, depends on L, C and RLOAD, estimation of the physical value of these components allows updating the coefficients and recovering power conversion efficiency and output stability over the time.

1.4 SYSTEM REQUIREMENTS

To achieve the previously described target and exploit related benefits in a silicon device, a multimeter function block shall be designed with specifications related to integration and accuracy. To limit manufacturing costs, the power stage and the multimeter supervisor shall be integrated on the same silicon device using the same BCD technology. Unfortunately, this technology is not advantageous for integrating complex digital circuits. To be area-efficient, the supervisor design shall be as simple

and compact as possible, without exceeding half of the power stage silicon area. In a commercial DC-DC buck converter with a maximum output current of 1A, a V_{IN} up to 30V, and a switching frequency of 1MHz, the area of the power stage can reach 1mm², and the area of the supervisor should not exceed 0.5/0.6 mm². About precision, considering the nominal value and range of each target parameter described in TABLE 1, 5% error can be accepted to evaluate components aging and efficiently implement auto-tune algorithms.

TABLE 1. Target parameters

NAME	NOMINAL	RANGE
R_C	0.045 Ω	0.01 Ω to 0.1 Ω
R_L	0.045 Ω	0.01 Ω to 0.1 Ω
R_{DSON}	0.3 Ω	0.1 Ω to 0.5 Ω
L	15 µH	12 µH to 18 µH
C	47 µF	37 µF to 56 µF
R_{LOAD}	50 Ω	5 Ω to 100 Ω

1.5 EXISTING APPROACHES

Different solutions are available to estimate single components directly [13] [14] [15] [16] [17], but these approaches require additional circuitry, and their analysis is typically limited to only one parameter. Other solutions estimated multiple components: [18] solved the state equation but only evaluated capacitance and inductor. To consider parasitic components in the analysis, a time-domain model and a virtual replica of the converter were defined in [19][20][21]. The resulting complexity made the silicon implementation of a compact digital supervisor unfeasible, in the same technology used for the power converter. [22] [23] exploited a neural network and the relationships between spectral components of voltage/current and electrical parameters. However, high clock sampling frequency and complex digital processing

were required, making digital implementation difficult when area and timing requirements are limited.

1.6 PROPOSED APPROACH

This work defined a system based on neural network, which indirectly estimated all required parameters with enough precision, that can be integrated together with the power converter in a tiny silicon device. The design of a PCB board, which will be used to verify and study this approach, is also described. As shown in Fig. 5., the approach consisted of evaluating some electrical parameters of the circuit, such as voltages and currents that are easy to sense: current flowing in the inductor and current load are respectively measured by R_{S1} and R_{S2} connected to a sensing amplifier, while output and input voltages were respectively sensed by resistive partitions R_{P1} and R_{P2}. Additional information was provided by the temperature T_{HS} of the high side MOS and the duty cycle DC set by the PID. The first step of the study was to identify which of these sensed values (sDC, sV_{IN}, sI_{IND}, sI_{LOAD}, sV_{OUT}, sT_{HS}) were the optimal inputs for the neural network, to estimate the target parameters listed in TABLE 1, within a 5% error allowed. In TABLE 2, possible neural network inputs, nominal values and related variation ranges are listed.

TABLE *2*. Input parameters

NAME	NOMINAL	RANGE
sV_{IN}	12V	11.76 V to 12.24 V
sDC	50%	40 % to 60 %
sI_{IND}	/	-0.1 A to 1.2 A
sI_{LOAD}	/	0.04 A to 1.1 A
sV_{OUT}	5	4.9 V to 5.1 V
sT_{HS}	25°C	0 °C to 80 °C

This work is an enhancement of a previous study [9] and it overcomes some related limitations. Following chapters describe in detail each step of the system definition and board implementation: analysis of the inputs, development of the power converter

model, data set extraction, design of the sensing analog circuit and design of the validation board.

1.7 INPUTS IDENTIFICATION

To identify the optimal inputs set two approaches were used:

- Analysis of the state space equations related to a synchronous DC-DC buck converter.
- MATLAB® simulation of a DC-DC converter model Simscape® and analysis of current and voltage waveforms according to output parameters changes.

To obtain a nonlinear relationship between all considered parameters, all resistive paths in the schematic in Fig. 5. shall be described in their parallel or serial configuration, Eq. (1.5), (1.6), (1.7) and (1.8) considered in the state space equations Eq. (1.9), in which D represents the high (D=1) or low (D=0) state of the HS signal.

$$\alpha = (R_C + R_{LOAD}) / (R_C \times R_{LOAD}) \tag{1.5}$$

$$\beta = (R_{LOAD}) / (R_C \times R_{LOAD}) \tag{1.6}$$

$$\gamma = R_L + D \times R_{DSON} \tag{1.7}$$

$$\delta = R_C + R_{LOAD} \tag{1.8}$$

$$\begin{bmatrix} \frac{diL}{dt} \\ \frac{dvC}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{\gamma+\alpha}{L} & -\frac{\beta}{L} \\ \frac{\beta}{C} & -\frac{1}{C\times\delta} \end{bmatrix} \times \begin{bmatrix} iL \\ vC \end{bmatrix} + \begin{bmatrix} V_{IN} \\ 0 \end{bmatrix} \times \frac{D}{L} \tag{1.9}$$

Eq. (1.9) suggested that target parameters C, L, R_{LOAD}, and R_C were strongly related to sI_{IND} and sV_{OUT}. Unfortunately, the only term in Eq. (1.9) that describes R_L and R_{DSON} is γ, which is divided by L, accordingly to the schematic shown in Fig. 5. and to the series connection of these three components. This divide operator makes the

relationship of R_L and R_{DSON} weak and not useful. Since the purpose of this work was the supervision of such a system, integrated into a silicon device and in terms of aging or loop optimization, the R_L parameter was neglected and the R_{DSON} evaluation was based only on aging variation. Values assumed by R_{DSON} were selected based on data provided by reliability tests and silicon characterization. To verify this hypothesis, a Simscape® model of the synchronous DC-DC buck converter, shown in Fig. 6. has been developed and simulated in MATLAB®.

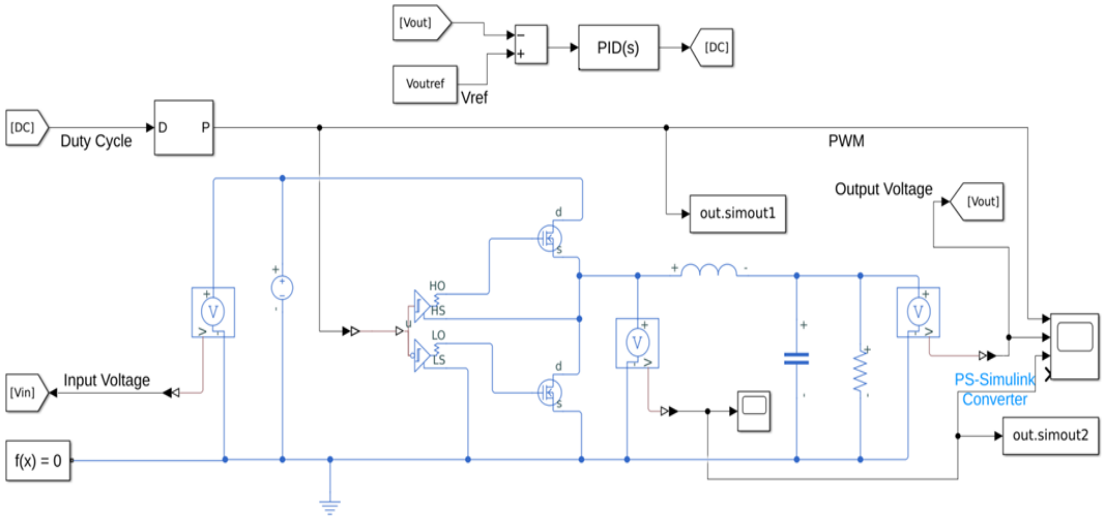
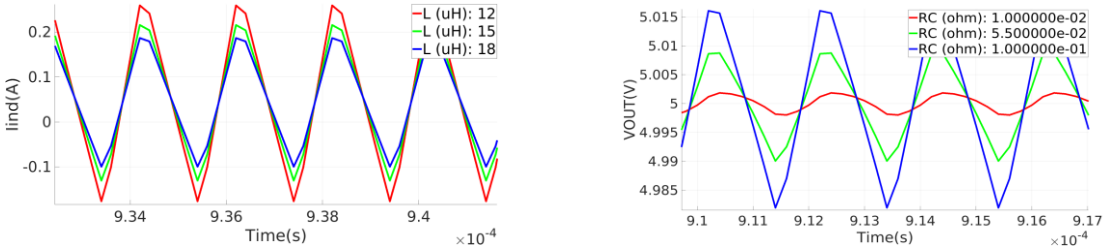


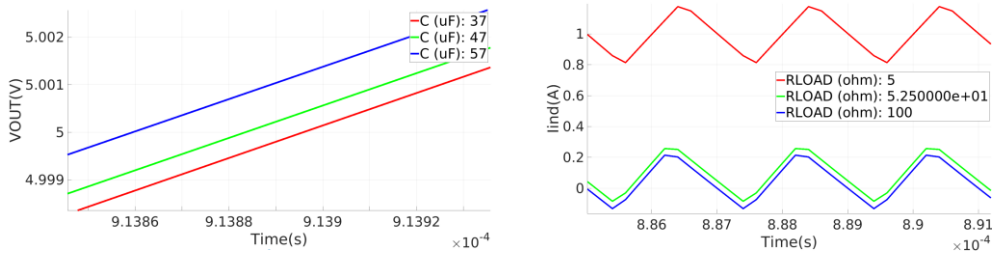
Fig. 6. DC-DC buck converter Simscape model.

The temperature parameter has been neglected in this evaluation and will be considered in the evolution of the activity, when the system will be verified at the physical level, implemented on a development board. From simulations, significant variations in output voltage and inductor current ripples were observed, when changing target parameters: for example, when C and L change by +/-20% from their nominal values or when R_C and R_{LOAD} assumed the maximum and minimum of their ranges, V_{OUT} and I_{IND} waveforms were subject to shapes variations as shown in Fig. 7. as function of R_C and L and Fig. 8. Variation of VOUT (a) and IIND (b) as function of C and RLOAD



(a) (b)

Fig. 7. Variation of V_{OUT} (a) and I_{IND} (b) as function of R_C and L



(a) (b)

Fig. 8. Variation of V_{OUT} (a) and I_{IND} (b) as function of C and R_{LOAD}

1.8 DATA SET EXTRACTION

The proposed approach consisted of sampling these two waveforms and analyzed the time variations of the related shapes. By the results extracted from simulations, it was important to provide the neural network with information about signals changes over one PWM period T_{SW}. This was accomplished by providing data samples with a batched structure input, which allowed passing time-dependent changes of parameters to the neural network more efficiently, instead of providing derivative values dV_{OUT}/dt and dI_{IND}/dt computed on a finite number of samples [9]. Each batch consisted of N samples of sI_{IND} and sV_{OUT} belonging to one PWM period of the HS signal when the PID was steadily regulating the V_{OUT}, as shown in Fig. 9. The system used 2 samples on the rising edge and 2 samples on the falling edge of the input signals, far from their maximum and minimum values. To verify the proposed approach, a data set was extracted from the MATLAB® model and a tiny neural network was devised, trained and tested using QKeras® QAT policy. Respect the previous study [9], where the number of simulations was 10 and the training data set poor, the MATLAB® script run

1,000 simulations of the developed model. For each run, all output parameters and V_{IN} assumed randomly one of the 50 discretized values in the defined range. In each simulation 10 values of sI_{IND} and sV_{OUT} were sampled in 100 PWM periods and only samples with index V2, V4, V7 and V9 were saved and averaged on each period. A data set table was created so that first 8 columns consisted of sV_{OUT} and sI_{IND} batched samples, that were used as input to the neural network, and next 6 columns contained related parameters R_C, R_L, R_{DSON}, C, L, R_{LOAD} representing the output. Acquired data were passed to python script that removed outliers, normalized the columns values between [-1, 1] and split table as: 70% of the total rows number of data set was used to train the neural network, 15% was used for validation and 15% to test the results.

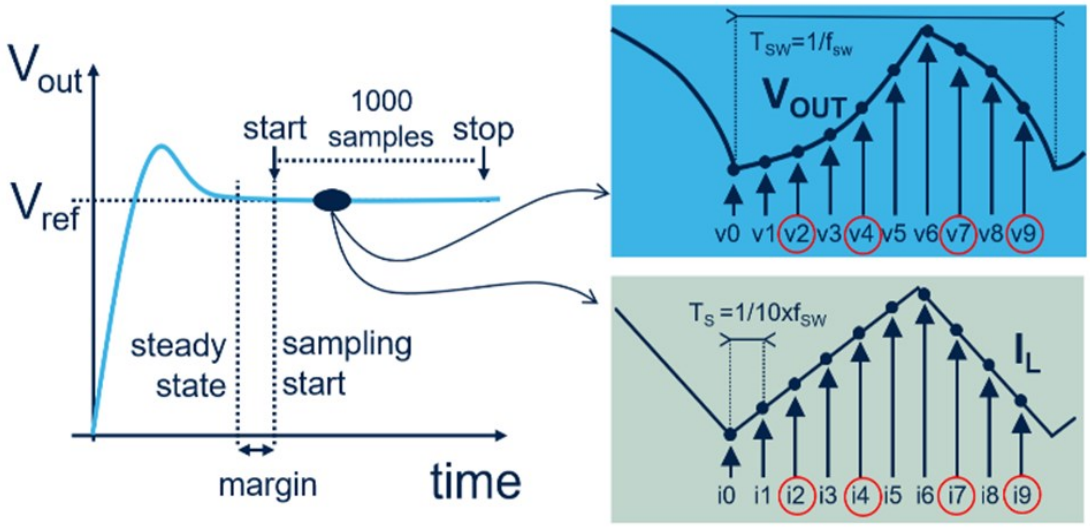


Fig. 9. Data set samples acquisition.

CHAPTER 2

hardware-based analog normalization

Data normalization constitutes a fundamental pre-processing methodology wherein data undergoes scaling or transformation to ensure each feature contributes equitably to the analytical process. Compelling evidence suggests that normalization plays a critical role in preparing datasets for subsequent processing stages. The efficacy of machine learning algorithms is inherently contingent upon data quality, which directly influences the development of a generalized predictive model capable of addressing the classification problem with optimal accuracy.

The normalization process fundamentally alters the distribution of features within a dataset, typically converting them to a common scale without distorting the underlying relationships or differences in value ranges. This transformation is particularly crucial when dealing with features that exhibit substantial variance in their magnitude scales.

The implementation of effective normalization techniques substantially enhances the convergence rate during model training and mitigates the risk of certain features dominating the learning process solely due to their larger numerical scale rather than their intrinsic predictive significance [24].

Datasets containing attributes with disparate value ranges present significant operational challenges. Attributes possessing substantially smaller numerical values often experience diminished influence or complete dysfunction when compared to attributes with larger magnitudes. This imbalance in attribute contribution necessitates data transformation through normalization techniques.

The normalization process is fundamentally essential for equalizing the range of values across all attributes according to a predetermined scale, thereby producing well-normalized data that enables equitable contribution from each feature. It is widely acknowledged that normalization serves as a critical preprocessing step for ensuring algorithmic fairness in feature evaluation.

Several methodological approaches exist for implementing data transformation through normalization:

- Min-Max normalization transforms the data linearly to a specified range, typically [0,1].
- Z-Score normalization standardizes values based on the mean and standard deviation of the attribute.
- Decimal Scaling normalization adjusts values by dividing by an appropriate power of 10:

$$X_{-normalized} = \frac{x}{10^j} \tag{2.1}$$

where j is the smallest integer

The strategic selection of an appropriate normalization technique depends significantly on the specific characteristics of the dataset and the requirements of the machine learning algorithm being employed. Proper normalization substantially enhances model performance by ensuring that all attributes contribute proportionally to the decision-making process based on their intrinsic predictive value rather than their numerical scale.

Decimal Scaling normalization formulated by Eq. (2.1), demonstrates utility in applications requiring intuitive interpretation of normalized values, particularly in financial modeling and business intelligence systems. This approach maintains the relative decimal position of values, making it advantageous for scenarios where human

interpretability of the transformed data remains critical, such as in financial ratio analysis or economic indicators.

The choice should be guided by the specific requirements of the application domain, the characteristics of the dataset, and the underlying assumptions of the machine learning algorithm being employed [24] [25] [26] [27].

In this work, two normalization methods were only discussed, namely Min-Max and Z-Score. The focus is on Min_Max normalization due to its simpler implementation in analog circuitry.

2.1 NORMALIZATION BASICS

The pre-processing involves several distinct techniques:

- Data discretization (converting continuous values to discrete categories)
- Removing outliers and noise
- Integrating data from different sources
- Handling missing or incomplete data
- Transforming data to comparable ranges (normalization)

Normalization is particularly important because machine learning algorithms can be heavily biased when features have wildly different scales. For example, if one feature ranges from 0-1 while another ranges from 0-10,000, the second feature would dominate the model's learning process not because it is more important but simply because of its larger numerical values.

The core principle here is creating fairness in how features influence model decisions. When we do not know which features matter most, normalization ensures they all start with equal opportunity to contribute to the learning process.

As large datasets became important research resources, the need for rigorous data preparation became evident. Raw data typically has many quality issues—

incompleteness, inconsistencies, inaccuracies, duplications, and noise. These problems directly lead to unstable algorithms and unreliable systems.

Data collection is often done with minimal controls, resulting in numerous data quality issues. Analyzing data without addressing these problems first leads to misleading results. While pre-processing can be time-consuming, it is essential for reliable outcomes.

In essence, no matter how sophisticated the algorithms are, they can only perform as well as the quality of data we feed them. Proper pre-processing is not just helpful—it is fundamental to the entire machine learning process.

The pre-processing of data represents a vital procedural step for attaining optimal classification performance prior to the evaluation of data through machine learning algorithms. This process encompasses data discretization, elimination of outliers and noise, integration of data from diverse sources, management of incomplete data, and transformation of data to comparable dynamic ranges (specifically normalization). Data normalization, in particular, constitutes a crucial pre-processing step involving the transformation of features into a common range, thereby preventing features with larger numerical values from overwhelming those with smaller numerical values. The primary objective is to reduce the bias associated with features whose numerical contribution disproportionately influences the discrimination of pattern classes. In scenarios where the relative significance of features remains undetermined, equalization of feature importance becomes necessary for accurate prediction of output classes for unknown instances. This approach proves especially beneficial for statistical learning methodologies, as it ensures equitable contribution from all features throughout the learning process [24].

Over recent decades, datasets, which constitute substantial data collections, have emerged as significant resources for research communities. These datasets serve as benchmarks for developing predictive models applicable to classification, clustering, forecasting, and related analytical tasks. Consequently, data mining and machine learning methodologies have been formulated to autonomously extract valuable information from these extensive data repositories through various data processing procedures. The acquired data necessitates processing due to frequent quality deficiencies stemming from incompleteness, inconsistency, inaccuracy, data

redundancy, and elevated noise levels. These deficiencies engender instability in machine learning algorithms, culminating in unreliable systems and diminished reproducibility of decision-making processes [28].

Data pre-processing constitutes a critical phase in the data mining process. Data collection methodologies are frequently subject to minimal control, resulting in outliers, implausible data combinations, and absent values, among other issues. The analysis of data that has not been meticulously filtered for such anomalies may yield misleading outcomes. Consequently, data representation and quality assume paramount importance prior to conducting any analytical procedures. Several factors, including quality, reliability, and availability, significantly influence the successful interpretation of data by neural networks. The presence of irrelevant information or noisy, unreliable data renders knowledge discovery particularly challenging during the training process. While data preparation and filtering procedures may require substantial processing time, the completion of pre-processing operations yields more dependable data and robust analytical results [29].

2.1.1 Min-Max Normalization

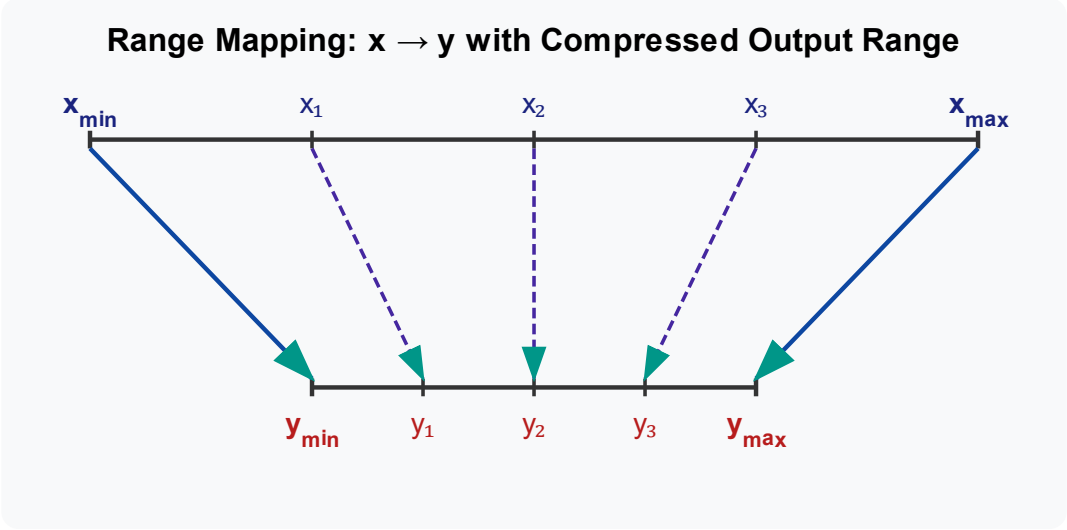


Fig. 10. Min-Max Normalization.

In mathematical terms, the most common normalization technique, min-max normalization, can be expressed as:

$$X_{-normalized} = \frac{(x - x_{min})}{x_{man} - x_{min}} \quad (2.2)$$

where x represents the original feature value, x_{min} and x_{max} denote the minimum and maximum values of that feature respectively, and X_normalized represents the scaled value within the range [0,1].

There is another version of min-max normalization, as shown in Fig. 10. allowing data to be scaled to any arbitrary range [y_{min} , y_{max}] instead of the default [0,1]. This is particularly useful when custom output ranges are required.

$$Y_normalized = (y_{max} - y_{min}) \times \frac{(x - x_{min})}{(x_{max} - x_{min})} + y_{min} \quad (2.3)$$

Min-Max normalization is particularly suitable for applications where a bounded range is required, such as neural network inputs or image processing. This technique preserves the relationships between the original data values while constraining them to a specific range, typically [0,1]. It finds extensive application in computer vision algorithms, recommendation systems, and scenarios where feature scaling is essential but the original distribution shape must be maintained.

2.1.2 Z-score

$$X_{-normalized} = \frac{(x - \mu)}{\sigma} \quad (2.4)$$

Z-Score normalization proves invaluable for applications involving statistical analysis and algorithms that assume normally distributed data. The evidence conclusively demonstrates that Z-Score normalization excels in outlier detection frameworks, clustering algorithms, and principal component analysis. This technique is especially effective when the actual minimum and maximum values of attributes are unknown or when the dataset contains significant outliers that would distort Min-Max scaling.

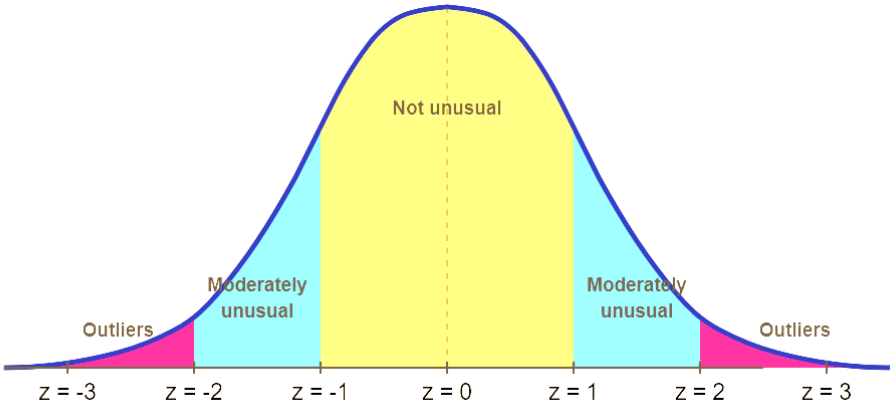


Fig. 11. Detecting Outliers with Z-Scores

TABLE *3*. **Min-Max Normalization vs Z-Score Standardization:**

Aspect	**Min-Max Normalization**	**Z-Score Standardization**
Output Range	Bounded [ymin, ymax], typically [0,1]	Unbounded, though approximately [-3,3] contains ~99.7% of values in normal distributions
Central Tendency	Preserves relative positions	Centers around mean (0)
Scale	Based on range (xmax-xmin)	Based on standard deviation
Zero-Centered	No (unless $y_{min} = -y_{max}$)	Yes (mean becomes 0)

2.1.3 Outliers

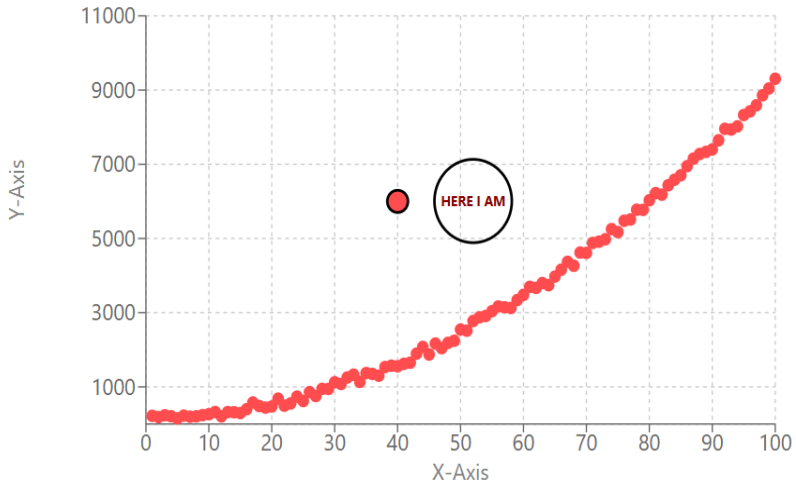


Fig. 12. Outlier

Outliers, as illustrated in Fig. 12. in neural network data represent extreme values that significantly deviate from the majority of observations in a dataset. These anomalous data points can substantially impact the training and performance of neural networks due to their disproportionate influence on learning algorithms.

Neural networks are particularly susceptible to outliers because of their ability to fit complex patterns. As demonstrated consistently across studies neural networks are powerful function approximators capable of modeling intricate relationships in data; however, this same flexibility makes them vulnerable to overemphasizing outlier points during training. When outliers exist in training data, networks may allocate excessive weight to these unusual observations, potentially leading to overfitting and diminished generalization performance on new data.

Several mechanisms can generate outliers in neural network contexts, including measurement errors, data corruption, natural variability within the phenomenon being studied, or instances from rare subpopulations. The impact of outliers varies depending on the specific neural network architecture and learning algorithm employed.

Common approaches to addressing outliers include:

1. Detection and removal techniques using statistical methods such as Z-scores, the Interquartile Range (IQR), or more sophisticated algorithms like Isolation Forests and Local Outlier Factor.

2. Robust training methodologies that employ loss functions less sensitive to extreme values, such as Huber loss or quantile regression, which can mitigate the influence of outliers without explicit removal.

3. Data transformation procedures, including normalization, or applying non-linear transformations that compress the range of extreme values.

4. Ensemble methods that combine multiple models to reduce the impact of outliers on the final prediction.

The appropriate strategy for handling outliers depends on the specific application domain, the underlying data generation process, and whether outliers represent noise or valuable but rare information that should be preserved in the model [30].

A set of voltage measurements is considered for analysis, with values given as follows: 1.2V, 2.5V, 3.7V, 4.1V, and 5.0V. These measurements will be utilized as a case study in this section.

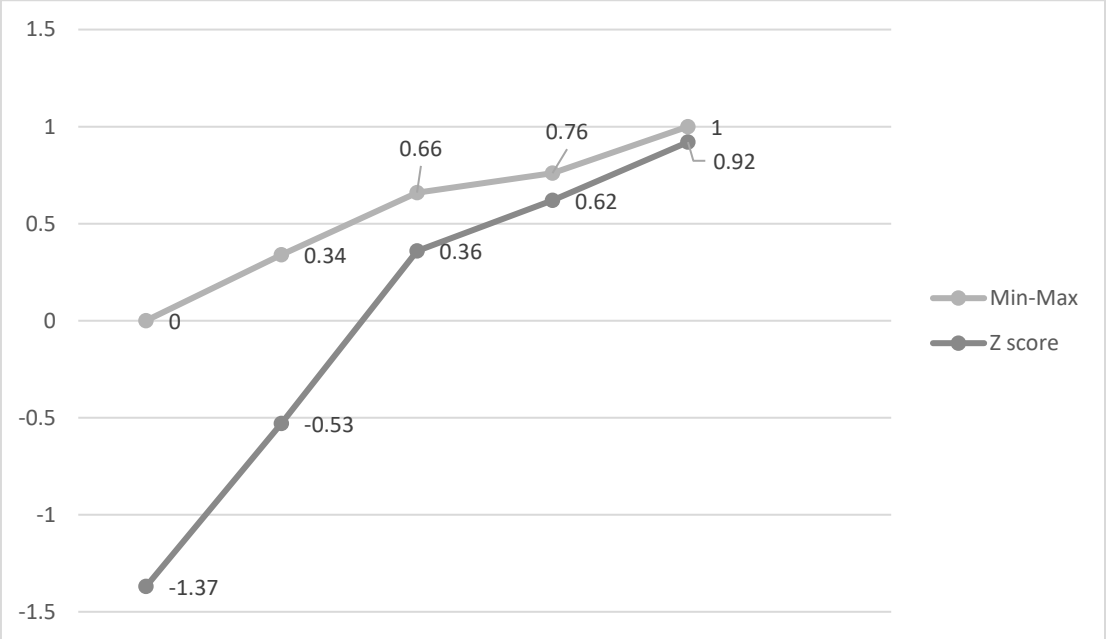


Fig. 13. The normalized value for both Min-Max and Z-score normalization

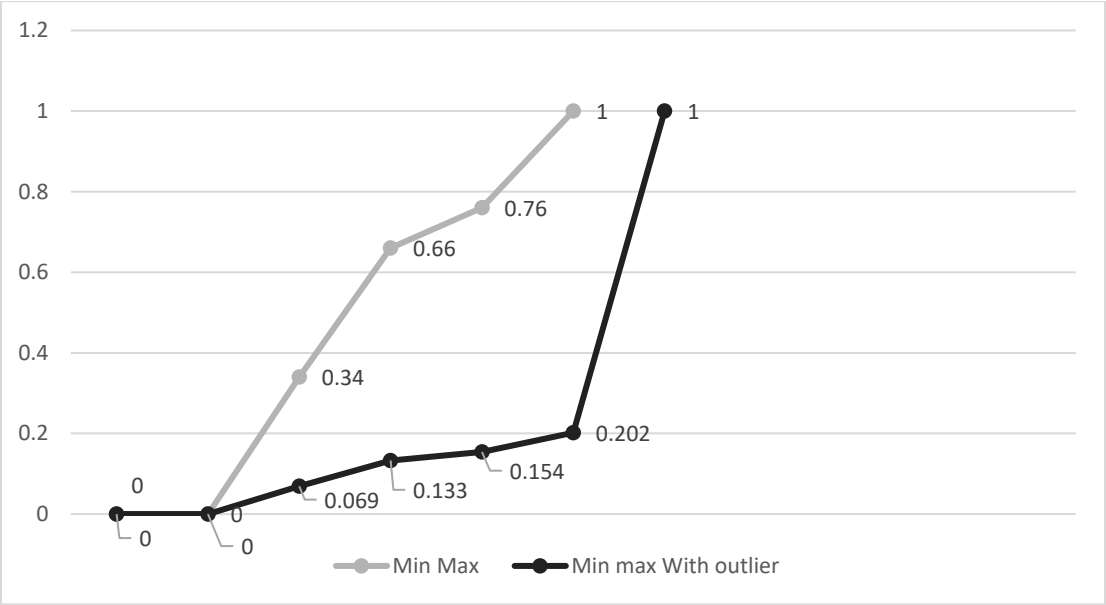


Fig. 14. In Presence of the Outlier, Min-Max Normalization

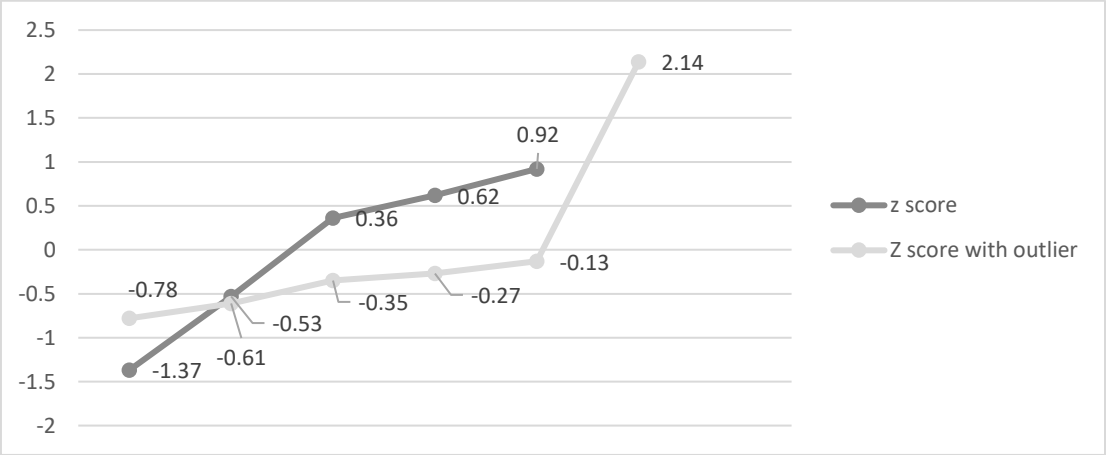


Fig. 15. In Presence of the Outlier, Z-Score Normalization

Upon inspection of the waveforms presented in Figures 13, 14, and 15, it becomes evident that:

- For min-max scaling, an outlier would compress the rest of the data into a smaller portion of the range.

- For z-score normalization, an outlier would shift the mean and increase the standard deviation, affecting all normalized values, but potentially less drastically than min-max scaling.

2.2 LIMITATIONS OF DIGITAL NORMALIZATION TECHNIQUES

Several fundamental constraints render digital domain normalization suboptimal for this specific application context. The implementation of normalization algorithms in the digital domain presents notable limitations as enumerated below:

- Digital normalization necessitates analog-to-digital conversion prior to the normalization process, which inherently introduces quantization noise into the signal path. This quantization effect can significantly compromise signal integrity, particularly in applications requiring high precision or when processing signals with substantial dynamic range. Consequently, implementing normalization procedures within the analog domain prior to analog-to-digital conversion results in diminished precision and compromised measurement accuracy in the final digital representation.

- The silicon area required to implement high-performance ADCs and digital processing blocks represents another significant limitation. The substantial footprint of these components can restrict integration capabilities and increase manufacturing costs, particularly in applications where miniaturization is a critical design objective. It is imperative for practical silicon implementation that the circuit design maintain dimensional efficiency, occupying a justifiable area footprint that aligns with manufacturing and economic constraints.

2.3 SIMPLE ANALOG NORMALIZER

The implementation of signal normalization in the analog domain prior to analog-to-digital conversion represents a critical architectural decision in the mixed-signal system

design. As illustrated in Fig. 16. the normalization process fundamentally transforms an input signal with voltage ripple into a standardized signal bounded within a precisely defined range (±1V). The voltage range between +4.9V and +5.1V depicted in Fig. 16. serves merely as an illustrative example to elucidate the normalization concept; in practical implementations, the signal characteristics may vary significantly.

Fig. 16. demonstrates the conceptual flow: a voltage signal exhibiting ripple characteristics is processed through the normalizer block, which effectively maps the original signal's dynamic range to a well-defined normalized voltage span suitable for subsequent analog-to-digital conversion.

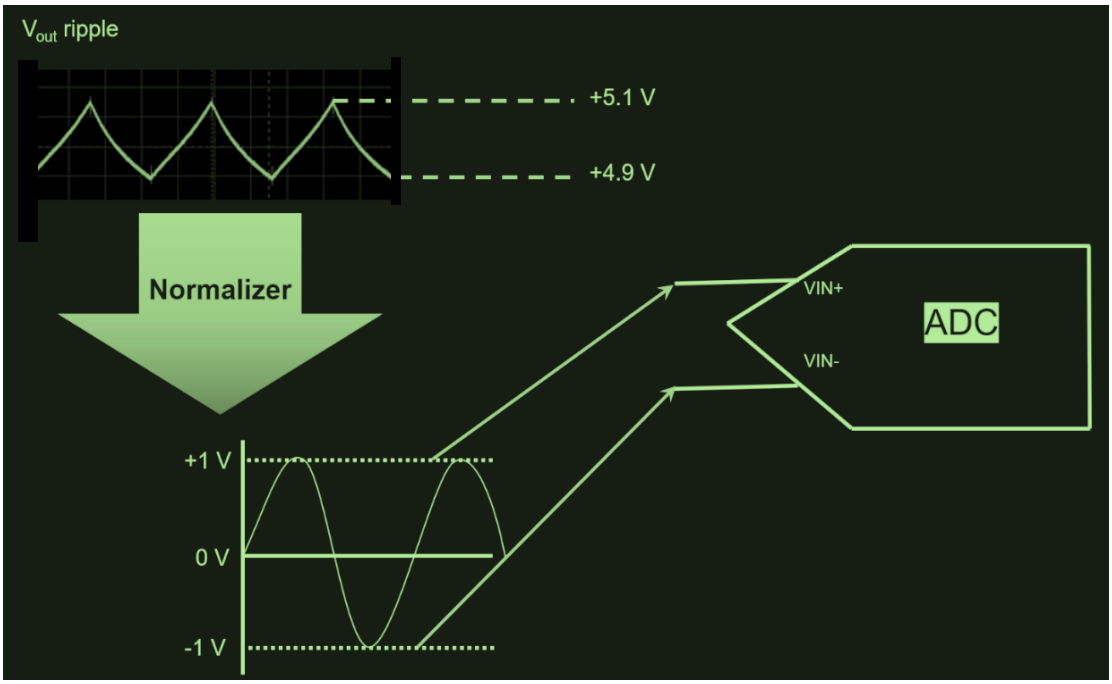


Fig. 16. Normalization Process

Fig. 17. quantitatively demonstrates the relationship between the original output voltage (displayed in green, corresponding to the right y-axis scale) and its normalized counterpart (shown in blue, corresponding to the left y-axis scale).

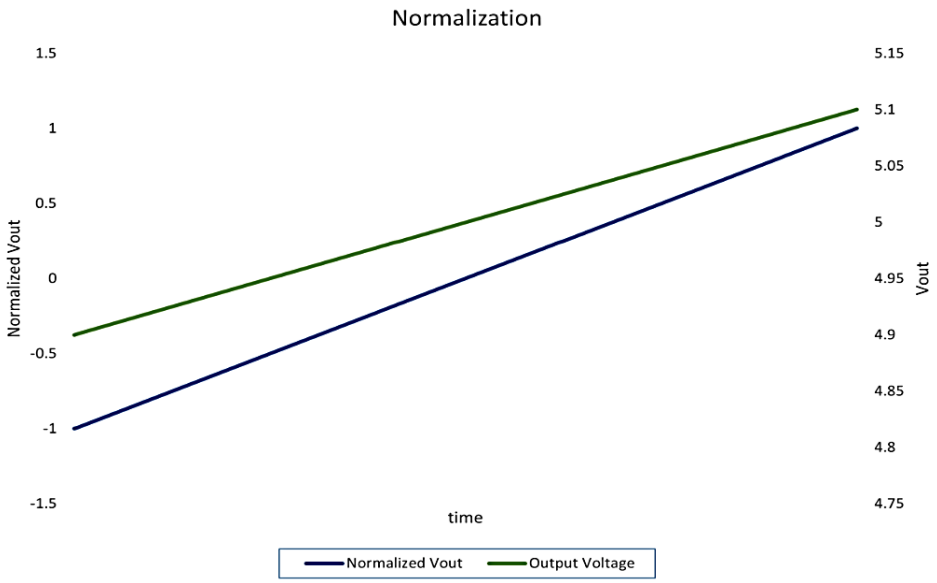


Fig. 17. Ranges of Interest

Fig. 18. and 19 further emphasize the technical necessity for analog normalization by highlighting the extremely constrained voltage ranges encountered in this application context. The simulation results reveal that the signal variations are remarkably minute—less than 5 millivolts in certain operational scenarios (as evidenced in Fig. 18.) and not exceeding 40 millivolts in maximal excursion cases (as presented in Fig. 19.). These exceptionally narrow voltage ranges would present significant challenges for direct digital conversion due to quantization limitations and resolution constraints inherent in analog-to-digital converter architectures.

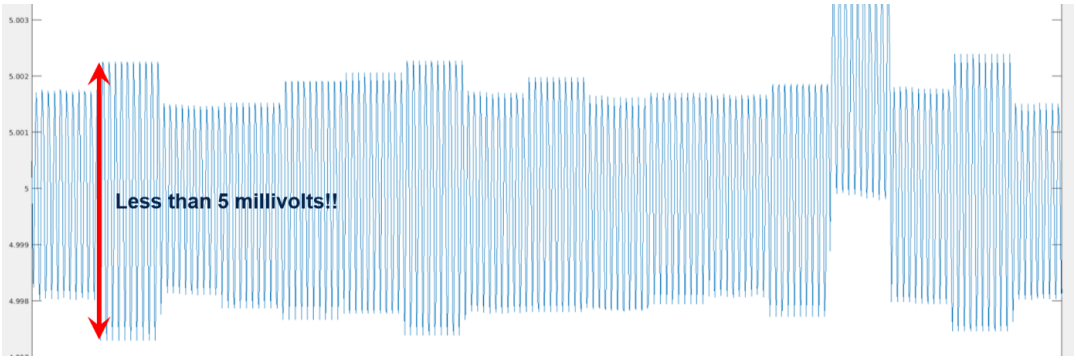


Fig. 18. Dynamic Range Limitation

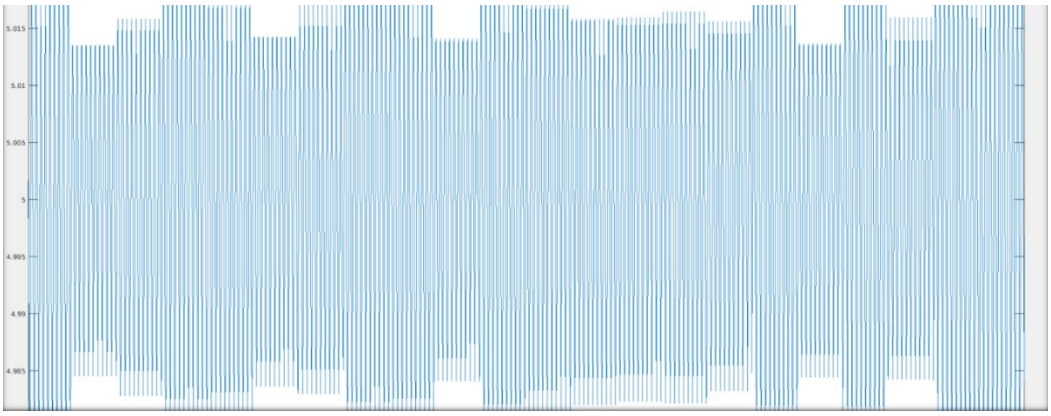


Fig. 19. The Maximum Range

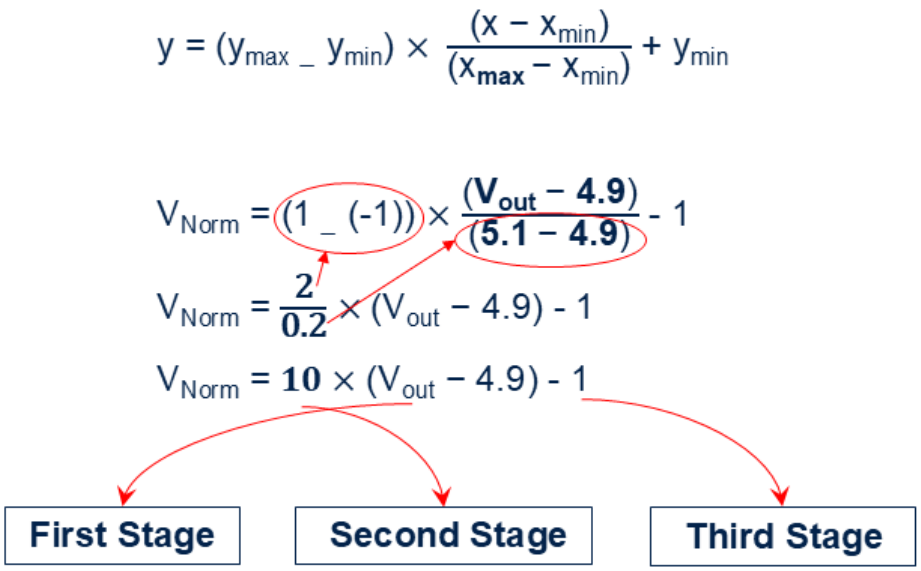


Fig. 20. Systematic Approach

The normalization process can be mathematically formulated and implemented through a systematic approach, as illustrated in Fig. 20. the fundamental principle of min-max normalization is expressed by the generalized equation at the top of the figure, where the input variable x is mapped to output y within specified boundaries.

For practical implementation, it is essential to recognize that the extrema of the signal (denoted as X_{min} and X_{max}) are predetermined through extensive simulation analyses. In silicon implementations, these parameters would be empirically determined via peak detector circuitry. The specific values of 4.9V and 5.1V utilized in these equations are

presented solely for illustrative purposes; in actual applications, these values would be determined by the particular signal characteristics of the system under consideration.

Similarly, the desired output range parameters (y_{min} and y_{max}) are established a priori as they correspond to the maximum peak-to-peak voltage range acceptable at the analog-to-digital converter input.

The normalization procedure is decomposed into three distinct computational stages for analytical clarity and implementation efficiency:

1. In the first stage, the input signal is referenced to zero by subtracting the minimum value (V_{out} - 4.9), effectively creating a zero-based dynamic range.
2. The second stage applies a gain factor G, mathematically expressed as:

$$G = \frac{(ymax - ymin)}{(x_{max} - x_{min})} = 10$$

3. The third stage introduces an offset by adding y_{min}, thereby establishing the complete min-max normalization expression as shown in the final equation:

$$V_{Norm} = 10 \times (V_{out} - 4.9) - 1$$

This segmented implementation facilitates not only the mathematical understanding of the normalization process but also provides a framework for efficient circuit realization.

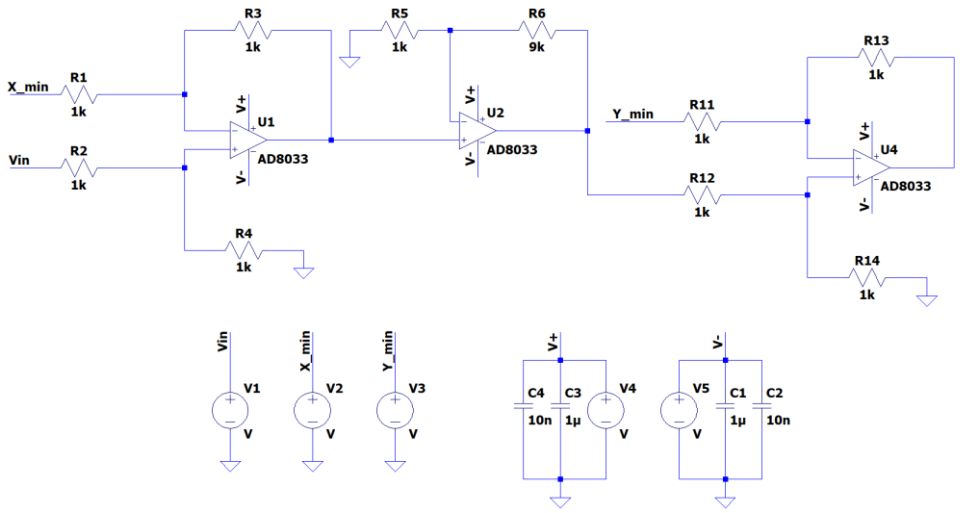


Fig. 21. Practical Circuit Implementation

Fig. 21. presents a practical circuit implementation of the previously described normalization process using operational amplifiers in LTspice simulation environment. This circuit architecture directly corresponds to the three-stage normalization procedure discussed earlier.

The implementation employs three AD8033 operational amplifiers configured to perform the sequential operations required for min-max normalization.

- The first operational amplifier (U1) functions as a unity-gain subtractor that performs the initial stage of normalization by subtracting the minimum value (X_min, represented as 4.9V in this illustrative example) from the input signal (Vin). This effectively shifts the signal to begin from zero.
- The second operational amplifier (U2) is configured as a non-inverting amplifier with a gain of 10, achieved through the resistor ratio of R6 (9kΩ) and R5 (1kΩ). This implements the second stage of the normalization process, applying the calculated gain factor G = 10 to the shifted signal.
- The third operational amplifier (U4) performs the final stage by subtracting Y_{min} (represented as 1V in this example) from the amplified signal, thus completing the min-max normalization as expressed in the mathematical formulation.

The circuit also incorporates power supply voltage sources (V4 and V5) of ±12V to ensure proper operational amplifier functionality, along with appropriate decoupling capacitors (C1-C4) for stability. The voltage sources V1, V2, and V3 model the input signal and reference voltages required for the normalization operation.

This circuit topology demonstrates how the theoretical normalization formula Eq. (2.3) can be effectively translated into a practical analog implementation using standard components, validating the feasibility of the proposed signal conditioning approach.

Despite the implementation of analog normalization presented in Fig. 21. several notable limitations must be acknowledged. While this approach circumvents the substantial silicon area requirements of high-resolution ADCs needed for digital normalization, it introduces its own set of constraints.

The analog implementation, though more area-efficient than a high-precision ADC solution, still demands significant silicon real estate due to the three operational amplifiers and their associated passive components. However, this area overhead is

generally an order of magnitude smaller than what would be required for a high-resolution ADC capable of directly digitizing the small-amplitude signals depicted in Fig. 18. and 19.

The cascaded operational amplifier topology introduces cumulative noise and offset errors at each stage, potentially compromising the precision of the normalization process. Additionally, the accuracy of the normalization is heavily dependent on resistor matching, which presents substantial challenges in integrated circuit implementations due to process variations, thermal gradients, and aging effects.

Furthermore, the circuit exhibits bandwidth and slew rate limitations imposed by the operational amplifiers, restricting performance for high-frequency input signals. The requirement for stable and accurate reference voltages introduces another source of potential error, as any drift in these references directly affects normalization accuracy.

The power consumption remains a concern due to the three active operational amplifiers drawing quiescent current from the supply rails, though this is still generally lower than what would be required by a high-resolution ADC with its associated digital processing circuitry.

These considerations highlight the inherent trade-offs between analog and digital normalization approaches. While the analog implementation significantly reduces silicon area compared to digital alternatives, it introduces performance limitations that must be carefully evaluated within the context of the specific application requirements.

2.3.1 DC Offset Compensation Challenges in Analog Signal Normalization

The implementation of analog normalization circuits presents significant challenges when confronted with DC offset variations. In the previously analyzed min-max normalization architecture, the first stage was specifically dedicated to removing the baseline voltage (X_{min}) from the input signal according to the Eq. (2.3). This critical operation establishes a zero-referenced signal for subsequent scaling operations. However, this approach inherently creates several implementation challenges of considerable magnitude.

The primary difficulty arises from the circuit's extreme sensitivity to reference voltage accuracy. The subtraction operation requires a precise voltage reference that exactly matches the minimum value of the input signal. Any deviation between the actual signal minimum and the reference voltage introduces a systematic error that propagates through subsequent normalization stages. It is fundamentally clear that this sensitivity to reference precision constitutes a fundamental limitation in practical implementations.

The consequences of imprecise DC offset removal are particularly severe in min-max normalization because the gain factor in the second stage is inversely proportional to the input signal range (x_{max} - x_{min}) according to the Eq. (2.3). For signals with narrow dynamic range, as illustrated in our previous analysis of signals with variations of merely 5-40 millivolts, the gain factor becomes substantially large. Consequently, even minor errors in the reference voltage are amplified considerably, potentially causing output saturation or significant normalization inaccuracy.

Several approaches may be employed to address these DC offset challenges:

1. Adaptive reference tracking circuits might be implemented to continuously monitor and adjust the reference voltage according to the actual signal minimum. However, such circuits introduce additional complexity, area overhead, and potential stability issues.
2. Differential signaling architectures could mitigate common-mode voltage variations by processing the difference between two signal paths rather than absolute voltage levels. This approach, while effective, necessitates fully differential operational amplifiers and matched signal paths.
3. AC-coupling through high-pass filtering might be considered for applications where the signal information resides primarily in higher frequencies. Nevertheless, this technique inherently eliminates low-frequency content which may contain valuable information depending on the application context.
4. Calibration procedures could be employed during system initialization to measure and compensate for DC offsets. However, this approach cannot account for temporal drift or dynamic changes in operating conditions.

Each of these potential solutions presents its own set of trade-offs regarding circuit complexity, silicon area, power consumption, and performance reliability. The

selection of an appropriate DC offset compensation strategy must be carefully evaluated within the specific constraints of the target application [31].

2.3.2 Limitations of Voltage Divider Approach for DC Offset Compensation

The implementation of a voltage divider configuration represents a potential solution for addressing DC offset in analog normalization circuits. This approach utilizes a resistive network to attenuate the input signal, effectively reducing the large DC component to a more manageable level.

The fundamental principle of this method lies in the proportional attenuation characteristic of voltage dividers. When an input signal passes through a voltage divider, both its DC offset and dynamic range are reduced by the same factor. This mathematical relationship creates an inherent trade-off that significantly constrains the effectiveness of this approach.

As the voltage divider is configured to achieve greater DC suppression by increasing the resistance ratio, the signal's dynamic range undergoes proportional attenuation. This diminishment of dynamic range presents a substantial challenge, particularly for signals with already narrow voltage spans. In practical terms, when the DC component is sufficiently suppressed to meet design requirements, the signal's information-carrying variations may be reduced to mere microvolts, approaching the noise floor of typical analog circuitry.

While subsequent amplification can theoretically recover the attenuated dynamic range, this compensation strategy encounters practical limitations in real-world implementations. The amplification stage, typically implemented with operational amplifiers, faces fundamental constraints related to supply voltage headroom, noise multiplication, bandwidth limitations, and slew rate restrictions. As amplification factors increase to compensate for greater attenuation, these limitations become increasingly pronounced.

Moreover, the extreme resistance values required for significant DC suppression introduce additional complications, including increased sensitivity to parasitic

capacitances, vulnerability to electromagnetic interference, and potential loading effects on preceding circuit stages.

The analysis reveals that while voltage dividers offer an appealing simplicity for DC management, they ultimately fail to provide a comprehensive solution for normalization circuits without additional compensation mechanisms [32]. A more holistic approach involving adaptive reference tracking, differential architectures, or specialized DC cancellation techniques would be required to overcome these inherent limitations.

2.4 USING ANALOG MULTIPLIER

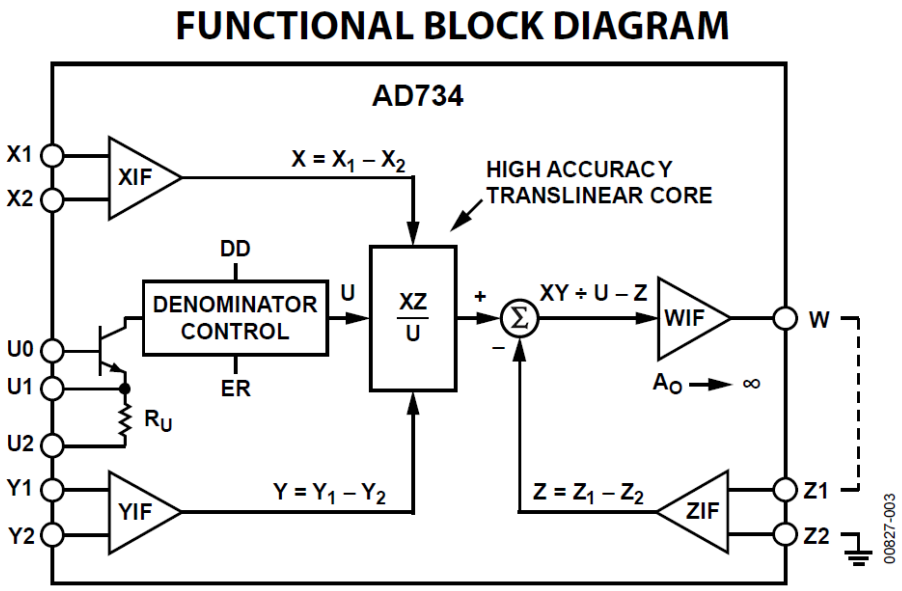


Fig. 22. Block Diagram of AD734 From Analog Devices [37].

The utilization of analog multipliers presents an alternative approach to address scaling challenges in normalization circuits. As illustrated in the provided documentation [37], specialized integrated circuits such as the AD734 from Analog Devices offer comprehensive signal processing capabilities through four-quadrant multiplication and division functions.

The AD734 operates as a high-precision analog computation engine, implementing transfer functions that can be configured for normalization operations. Its functional

block diagram reveals a sophisticated architecture with differential inputs, denominator control, and a translinear core that enables accurate multiplication and division operations. The multiplier processes the input signal according to the transfer function:

$$w = \left(\frac{(x_1 - x_2)(y_1 - y_2)}{U}\right) + z_2 \tag{2.5}$$

This mathematical relationship allows for simultaneous scaling and offset compensation, effectively performing the normalization function in a single integrated circuit. The output signal can be further conditioned using an operational amplifier (AD712) to achieve the desired signal characteristics.

Advantages:

1. **Direct implementation of the normalization equation**: The analog multiplier inherently performs the mathematical operations Eq. (2.5) required for normalization without the multi-stage approach necessary in simpler circuits.
2. **High precision**: The AD734 offers typical error rates of 0.1%, providing accurate signal processing capabilities critical for preserving signal integrity during normalization.
3. **Superior dynamic performance**: With a 10 MHz full power bandwidth and 450 V/μs slew rate, these devices can process high-frequency signals while maintaining normalization accuracy.
4. **Low distortion and noise characteristics**: The specified -80 dBc distortion and high signal-to-noise ratio (94 dB at lower frequencies) ensure minimal degradation of the normalized signal.
5. **Compact solution**: Using a dedicated integrated circuit reduces the component count compared to discrete implementations, potentially saving board space.

Disadvantages:

1. **Cost implications**: These specialized analog computing components command premium pricing (€44.48 per unit or €177.92 for four units), representing a significant cost factor in production designs.
2. **Supply voltage requirements**: These devices often necessitate dual supply voltages with relatively high rails to accommodate their internal architecture and maintain linearity across the operating range.
3. **Limited availability**: Specialized analog computing ICs may face supply chain challenges or eventual obsolescence compared to more common analog components.

Nevertheless, this solution is not without significant limitations. The cost implications of utilizing specialized analog computing components are substantial, with unit pricing that exceeds conventional operational amplifiers by an order of magnitude. This prohibitive cost factor is precisely why we have opted not to employ this approach in our testing board implementation. However, the underlying multiplicative principle represents an ideal solution for our custom silicon design. When implemented directly in an integrated circuit, the analog multiplier core can be incorporated without the substantial price premium associated with discrete components, while retaining all the technical advantages of the approach.

The analog multiplier approach represents a technically elegant solution for normalization requirements where signal fidelity and mathematical accuracy are paramount considerations. While economic constraints render this approach impractical for our prototype and testing phases using commercial components, we intend to adopt and optimize this conceptual framework in our final silicon implementation to achieve the desired normalization performance with significantly improved cost efficiency, contingent upon satisfactory results from our current testing board measurements.

2.4.1 Gilbert Cell Architecture for Precision Analog Multiplication

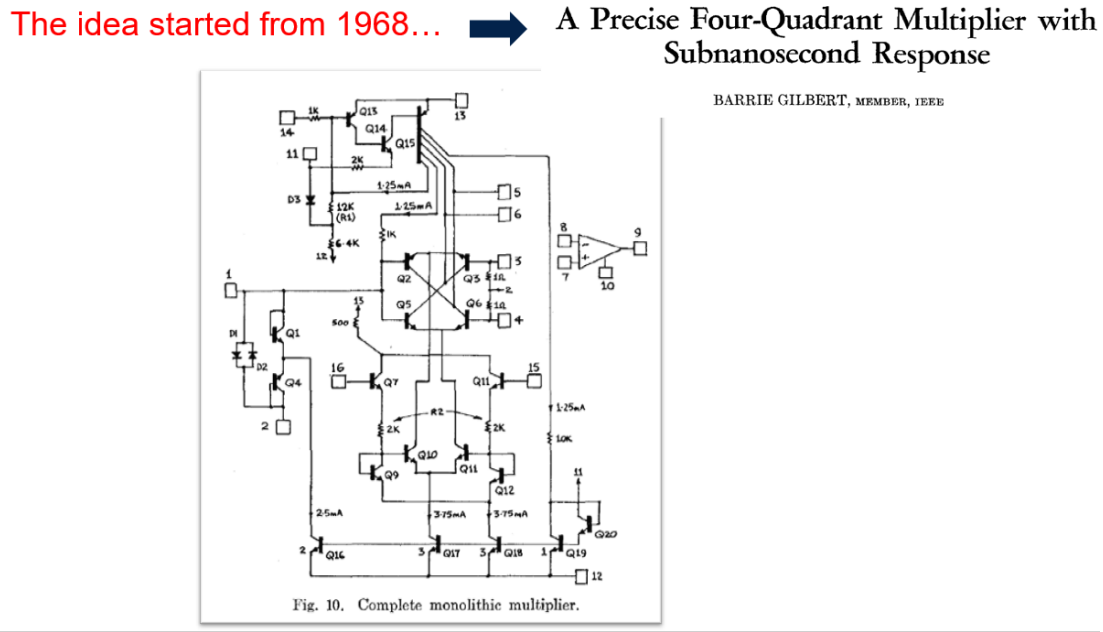


Fig. 23. A Precise Four-Quadrant Multiplier [33].

The development of precision analog multiplication circuits represents a significant milestone in integrated circuit design. The Gilbert cell, named after its inventor Barrie Gilbert, stands as one of the most influential circuit topologies in analog signal processing, with applications spanning from RF mixers to analog computation systems. The fundamental architecture of this circuit was initially conceptualized in 1968, as illustrated in Fig. 23., which depicts the complete monolithic multiplier designed by Gilbert. Contemporary understanding firmly establishes that this innovation established a new paradigm for four-quadrant multiplication in integrated circuit form.

The Gilbert cell's elegance lies in its differential topology, which enables four-quadrant multiplication—a capability that allows both input signals to swing positive and negative while maintaining precisely controlled output characteristics. The core of the architecture consists of cross-coupled transistor pairs arranged to form a current-steering mechanism, where the differential input voltages modulate the division of current between output branches. This configuration inherently provides excellent common-mode rejection and temperature stability, two critical parameters for precision analog computation.



Fig. 24. AD534, Four-Quadrant Precision Multiplier [34].

The commercial significance of Gilbert's innovation became evident eight years after its initial conception, when Analog Devices introduced the AD534 in 1976—the first widely available integrated circuit implementation of the Gilbert multiplier. This component, shown in Fig. 24. ultimately achieved such technological importance that specimens are now preserved in the Computer History Museum, highlighting its historical significance in the evolution of analog integrated circuits.

The robust performance characteristics of the Gilbert cell, including its subnanosecond response time as noted in Gilbert's original publication [33], established it as the predominant architecture for high-frequency multiplication and mixing applications.

Despite the elegance and functionality of Gilbert cell-based analog multipliers, their widespread adoption has been constrained by several significant factors. The semiconductor industry's investment priorities have been predominantly directed toward digital technologies, influenced by the exponential improvements predicted and realized through Moore's Law [35]. While digital computation elements have benefited from dramatic reductions in size, cost, and power consumption with each process node advancement, analog multipliers have not experienced comparable scaling benefits. The fundamental physics underlying analog circuit operation imposes certain constraints that resist straightforward dimensional scaling.

Furthermore, the inherent susceptibility of analog signals to noise, interference, and process variations presents persistent challenges for precision multiplication applications. These limitations are particularly pronounced in deep submicron technologies where reduced supply voltages further constrain analog signal headroom. The industry's perception that "digital is better" has also influenced both engineering

decisions and market preferences, often directing research and development resources away from analog computation solutions even in applications where they might offer performance or efficiency advantages [36].

The complexity of designing, simulating, and modifying analog multiplier circuits remains substantially higher than for their digital counterparts, requiring specialized expertise that has become increasingly scarce in the semiconductor ecosystem. This combination of economic, technical, and perceptual factors explains why analog multipliers such as those based on the Gilbert cell topology continue to command premium pricing in the component market, despite their long-established design heritage. These considerations have directly informed our approach to implementing normalization circuitry, where we must carefully balance performance requirements against practical constraints of cost and complexity.

2.5 THE USAGE OF HIGH PASS FILTER

The fundamental challenge in implementing min-max normalization for signals with significant DC offset, as previously established, lies in the precision required for DC reference subtraction. The conventional approach necessitates exact knowledge of X_{min} and its accurate reproduction as a reference voltage, which presents considerable design challenges. A more elegant solution to this constraint involves the application of high-pass filtering techniques to inherently remove the DC component without requiring precise reference generation.

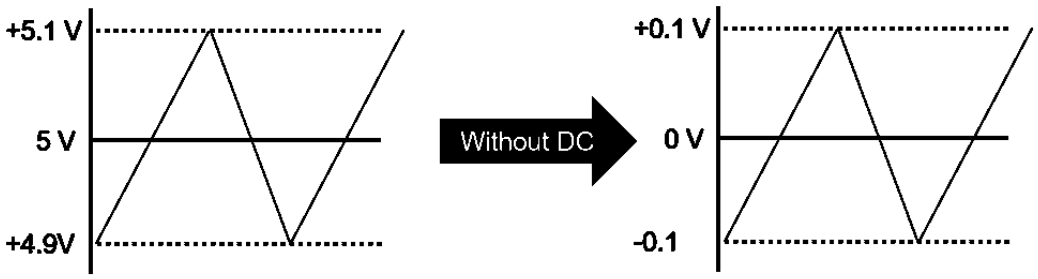


Fig. 25. High-Pass Filter operation

As illustrated in Fig. 25. the high-pass filtering approach fundamentally transforms the normalization problem. The input signal, which oscillates between +4.9V and +5.1V with a substantial DC component of 5V, is processed through a high-pass filter that inherently blocks the DC content, resulting in a signal centered at 0V and varying between -0.1V and +0.1V. This transformation effectively eliminates the need for precise X_{min} subtraction in the normalization equation Eq. (2.3).

By removing the DC component, the normalization equation can be simplified, as the term X_{min} becomes effectively zero:

$$Y_normalized = (y_{max} - y_{min}) \times \frac{(x)}{(X_{max})} + y_{min} \qquad (2.6)$$

There is no doubt that this approach substantially reduces the sensitivity to reference voltage accuracy that plagued earlier implementations.

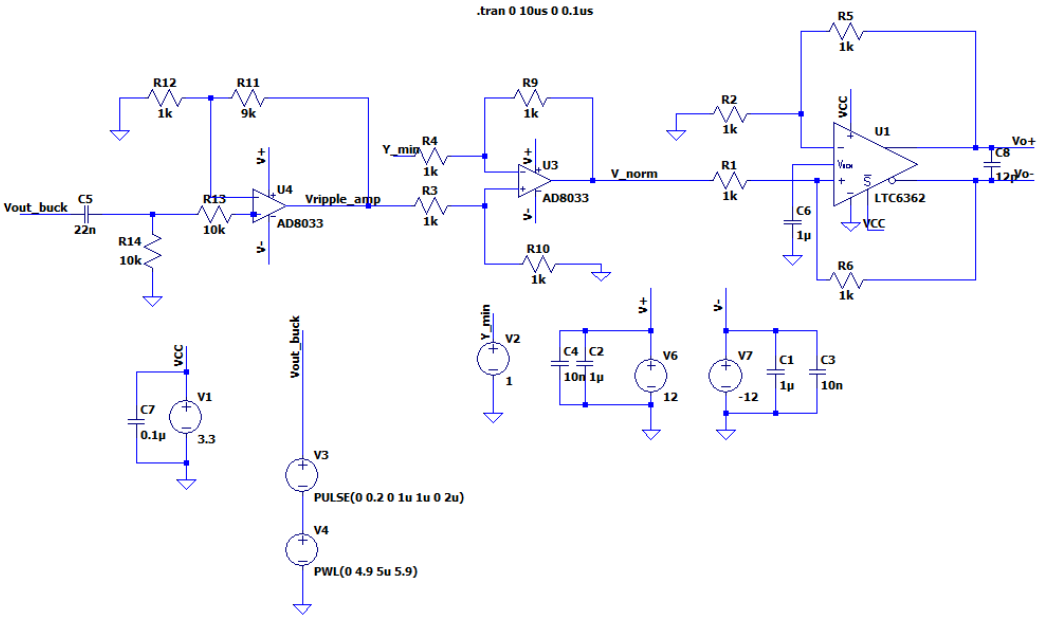


Fig. 26. Practical Implementation of Eq. (2.6).

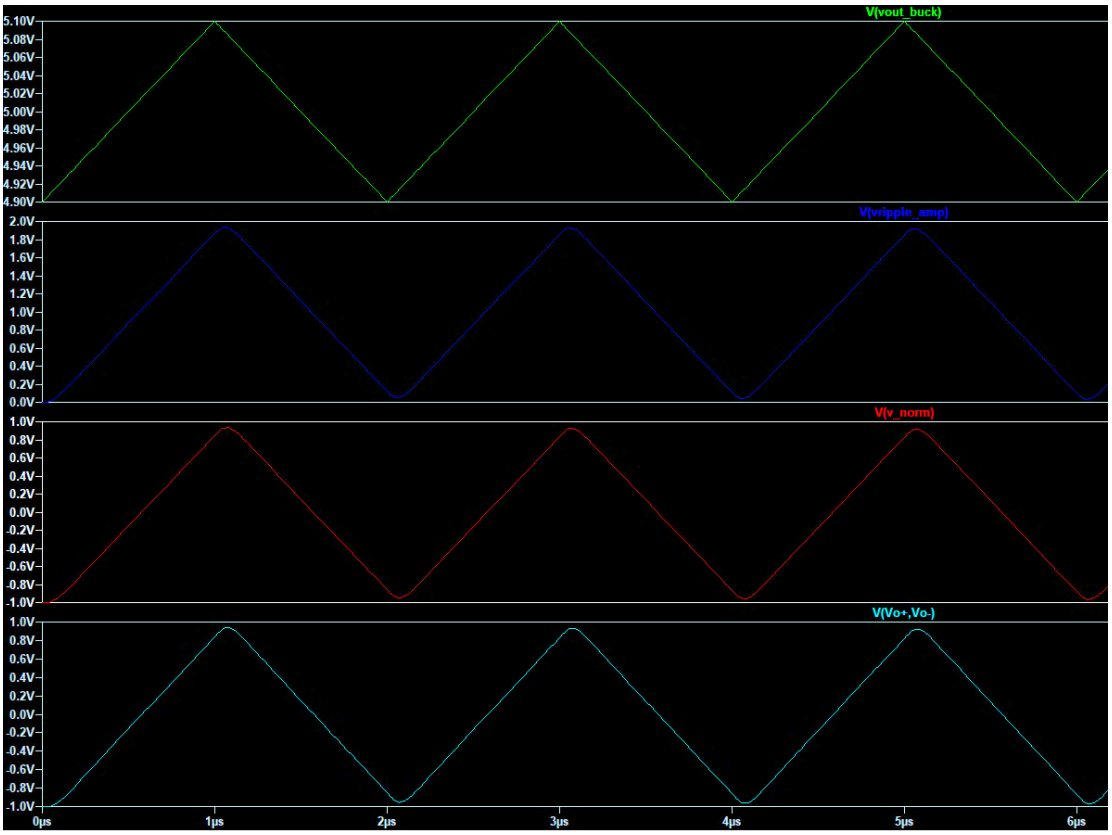


Fig. 27. Simulation results from LTspice

The practical implementation of this concept is demonstrated in Fig. 26. which depicts a complete normalization circuit incorporating high-pass filtering at the input stage. The HPF is formed by capacitor C5 (22nF) and resistor R14 (10kΩ), creating a first-order high-pass filter with a cutoff frequency:

$$f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 10k \times 22n} \approx 723\ Hz$$

This cutoff frequency is strategically selected to be below the frequency components of interest in the signal while effectively eliminating the DC component. The filtered signal is then amplified by operational amplifier U4 (AD8033) configured with a gain determined by resistors R11 and R12.

The subsequent stages implement the remaining normalization operations, with U3 providing the appropriate offset and U1 (LTC6362) performing the final conditioning to achieve the desired differential output range. This architecture eliminates the need for precise tracking of Xmin.

The simulation results obtained from LTspice for the high-pass filter implementation of the normalizer are presented in Fig. 27. the multi-plot display illustrates the signal transformation through various stages of the normalization process. The top waveform (green) represents V(vout_buck), showing the output voltage from the buck converter with a triangular ripple ranging from 4.90V to 5.10V. This signal serves as the input to our normalization circuit. The second waveform (blue) depicts V(ripple_amp), which represents the output after the initial high-pass filtering stage, effectively removing the DC component and rescaling the signal to a range of 0V to 2V. The third plot (red) shows V(v_norm), the normalized output signal with a symmetrical range of -1V to 1V, demonstrating successful bipolar normalization as required for subsequent analog-to-digital conversion. The bottom waveform (cyan) illustrates V (Vo^+ - Vo^-), representing the differential output of the fully differential amplifier. These results validate the efficacy of the high-pass filter approach in our normalizer design, demonstrating its capability to extract the dynamic components from the input signal while properly scaling the output to the desired voltage range.

2.5.1 Pros and Cons

The high-pass filter approach offers several significant advantages over conventional DC subtraction methods:

1. **Reduced Sensitivity to Reference Accuracy**: By eliminating the need for a precise X_{min} reference, the circuit becomes inherently more robust against reference drift and inaccuracies.
2. **Simplified Circuit Architecture**: The implementation requires fewer precision components and calibration mechanisms, potentially reducing area and power consumption.
3. **Improved Noise Performance**: Without the need for a high-gain differential amplifier to subtract X_{min} , the noise contribution from the first stage can be significantly reduced.

- Limitations of the High-Pass Filter Approach:

While the high-pass filter technique offers significant advantages for DC offset removal in normalization circuits, it suffers from a fundamental limitation that must be carefully considered in practical applications. The inherent characteristic of high-pass filters to block DC components creates vulnerability to gradual DC level variations in the input signal.

As depicted in Fig. 28. this limitation becomes evident when examining the response to slowly varying DC components. The upper trace (green) shows the input signal exhibiting a gradual DC level shift, while maintaining high-frequency oscillations of consistent amplitude. This represents a realistic scenario where thermal drift, component aging, or external conditions might cause the DC operating point to shift over time.

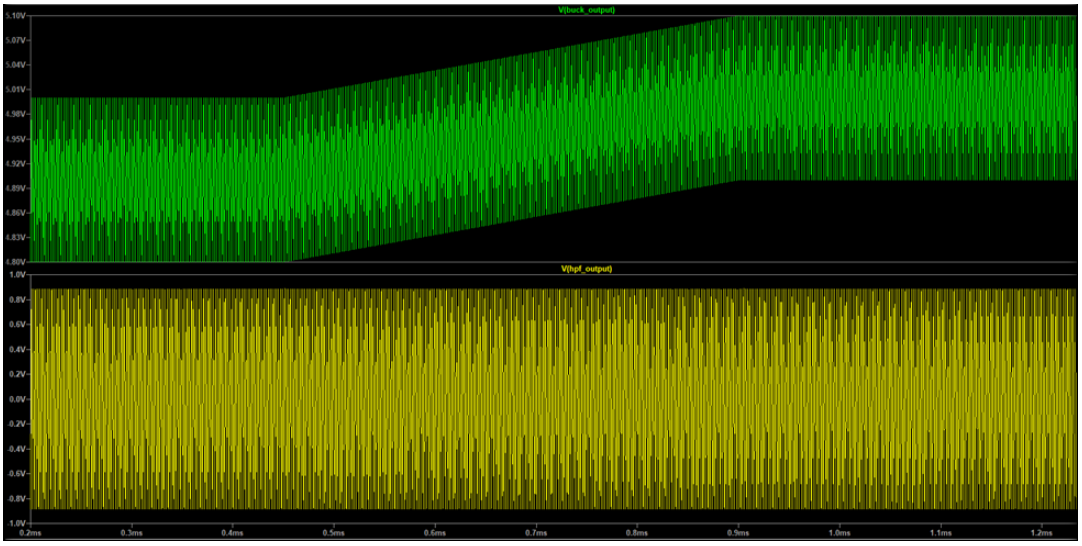


Fig. 28. Simulation results from LTspice

The lower trace (yellow) illustrates the high-pass filtered output, which maintains a consistent amplitude and position despite the DC level shift in the input signal. This response demonstrates the key limitation: the high-pass filter effectively removes both the initial DC level and its subsequent variation, rendering the circuit incapable of detecting or responding to these changes.

This behavior can be mathematically explained by examining the transfer function of a first-order high-pass filter:

$$H(s) = \frac{s}{s + \omega_c} \tag{2.7}$$

Where ω_c is the cutoff frequency. For frequencies significantly below ω_c, the magnitude of Eq. (2.7) approximates $\frac{\omega}{\omega_c}$, which becomes vanishingly small as ω approaches zero. This results in substantial attenuation of both static DC offsets and slow variations that have frequency components well below the cutoff.

The simulation results in Fig. 28. clearly illustrate this fundamental limitation—while the HPF approach simplifies the circuit architecture by eliminating the need for precise DC reference tracking, it simultaneously introduces insensitivity to meaningful DC level changes that might require compensation in certain applications.

For systems where the input signal's DC component carries significant information, or where maintaining calibration against absolute voltage references is essential, alternative approaches that combine high-pass filtering with periodic DC level measurement or adaptive reference adjustment may be necessary to achieve robust normalization performance.

This trade-off between implementation simplicity and complete signal fidelity represents a critical design consideration that must be evaluated within the specific context of each application's requirements.

2.6 New Solution: HPF + LPF

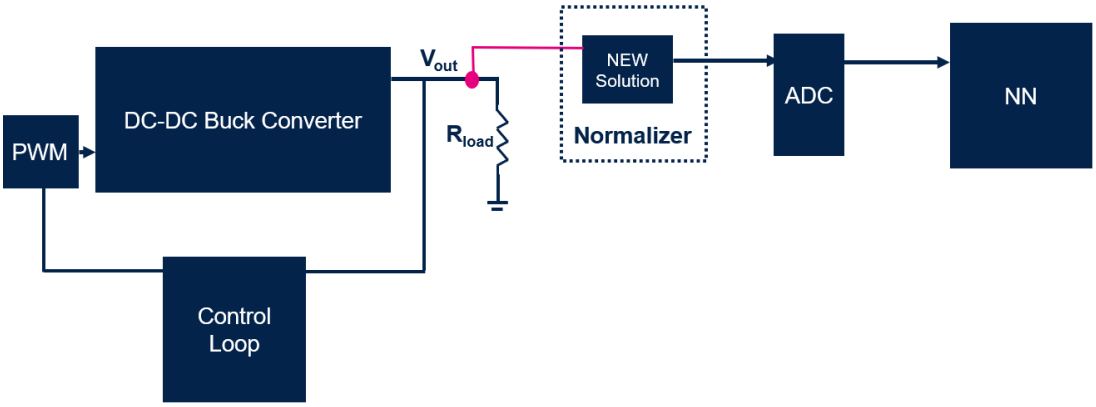


Fig. 29. HPF + LPF

The preceding discussions have illuminated several critical challenges in signal normalization, particularly regarding the preservation of DC information which is essential for accurate system monitoring. It is incontrovertible that conventional approaches often sacrifice valuable DC content during the normalization process. To address these limitations comprehensively, we propose a novel solution that strategically combines high-pass filtering (HPF) and low-pass filtering (LPF) techniques within our normalization architecture.

As illustrated in Fig. 29. our proposed solution integrates a specialized normalization block between the DC-DC buck converter output and the analog-to-digital converter (ADC) that feeds the neural network (NN). This normalization block implements a sophisticated dual-filtering approach that preserves both the dynamic AC components and the slowly varying DC levels that characterize aging-related phenomena.

The fundamental principle underlying this approach is the complementary nature of HPF and LPF responses. By employing these filters in a carefully orchestrated configuration, we can effectively separate the signal into its constituent components while maintaining the critical DC information that previous normalization methods typically eliminate. This approach is particularly crucial for monitoring gradual parametric shifts in power conversion systems, where subtle changes in DC levels provide essential diagnostic information about system degradation and aging effects.

The HPF component isolates the high-frequency transient behavior necessary for operational analysis, while the LPF component tracks the slow DC variations that offer insights into long-term reliability trends. Through this complementary filtering strategy, our normalizer preserves the complete signal information spectrum required for comprehensive system health assessment while still providing appropriately conditioned signals for the subsequent digital processing stages.

This innovative approach directly addresses the limitations of conventional normalization techniques discussed previously, ensuring that critical DC information is retained throughout the signal conditioning chain while still achieving the dynamic range adaptation necessary for effective neural network processing.

It is worth noting that this solution has been recognized for its innovation and practical utility, and has been submitted for **patent** filing by **STMicroelectronics**.

2.6.1 DC Tracking Capability of Low-Pass Filters

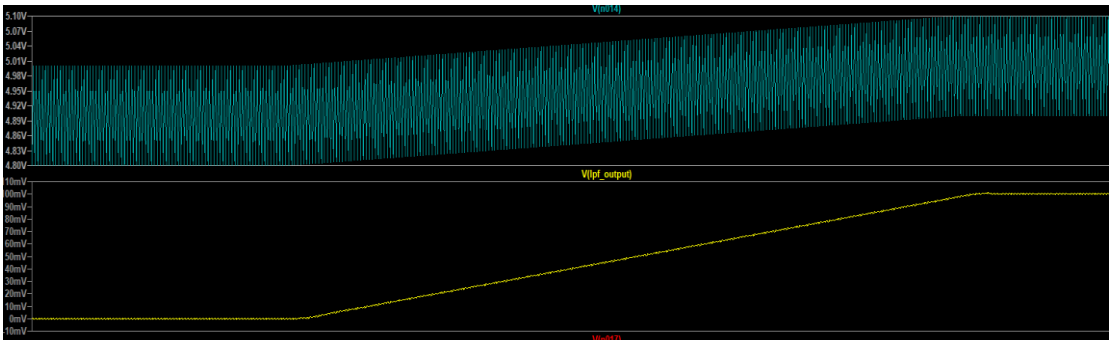


Fig. 30. LPF follows the DC change

The low-pass filter's inherent ability to track slowly varying DC components while attenuating higher frequency signals represents a significant advantage for monitoring gradual parametric shifts in electronic systems. As evidenced in the Fig. 30. the LPF effectively follows the DC trajectory (depicted in the yellow trace) while simultaneously filtering out the high-frequency components visible in the upper waveform. This characteristic is particularly valuable in aging monitoring applications where temporal drift manifests as incremental DC level variations.

The fundamental mechanism behind this behavior relates to the transfer function of the LPF, which can be expressed as:

$$H(s) = \frac{1}{1 + s\tau} \tag{2.8}$$

Where τ represents the filter time constant. For frequencies significantly below the cutoff frequency ($f \ll \frac{1}{2\pi\tau}$), the Eq. (2.8), approaches unity gain, allowing the DC and near-DC components to pass with minimal attenuation. Consequently, slow variations in the DC level—precisely the type associated with aging phenomena in semiconductor devices—propagate through the filter with high fidelity.

This capability is particularly crucial in reliability engineering, where monitoring gradual parametric shifts requires precision tracking of subtle voltage or current variations over extended time periods. The LPF effectively establishes a temporal

baseline by filtering out transient fluctuations, thereby isolating the underlying drift pattern attributable to aging mechanisms.

In practical implementations, careful selection of the filter time constant becomes essential to establish the appropriate balance between noise rejection and responsiveness to genuine DC drift. The time constant must be sufficiently large to attenuate unwanted high-frequency components while remaining responsive enough to capture the relevant aging-induced parametric variations.

2.6.2 Mathematical Manipulation

The Eq. (2.3) can be modified, or reformulated, in view of its circuit implementation.

In particular, it is first exemplarily assumed that

$y_{max} = K$ and

$y_{\min} = -K$ (where K can be, for example, equal to 1),

so that: $(y_{max} - y_{\min}) = 2K$.

The Eq. (2.3) may then be rewritten as:

$$y = 2K \cdot \frac{(x - x_{\min})}{x_{max} - x_{\min}} - K = \frac{2Kx - 2Kx_{\min} - Kx_{\max} + Kx_{\min}}{x_{max} - x_{\min}} =$$

$$= \frac{2Kx - Kx_{\min} - Kx_{\max}}{x_{max} - x_{\min}}$$

$$y = \frac{2K[x - x_{\min}/2 - x_{\max}/2]}{x_{max} - x_{\min}} \qquad (2.9)$$

The term $2K/(x_{max} - x_{\min})$ has a constant value, so that it can be considered as a constant amplification or gain factor G.

The Eq. (2.9) can thus be further modified as follows:

$$y = G \cdot [x - x_{\min}/2 - x_{\max}/2]$$

$$y = G \cdot [x - (x_{\min} + x_{\max})/2] \tag{2.10}$$

The term $(x_{\min} + x_{\max})/2$ can be considered, for example in a continuous real time processing, as the average or constant (i.e., DC) value or component of the input signal x, so that the Eq. (2.10) can be further modified as follows:

$$y = G \cdot [x - x_{\mathrm{DC}}] \tag{2.11}$$

wherein the term x_{DC} represents the above referenced DC component of the input signal x.

In particular, the DC component of the input signal x may generally be subject to slow variations or changes over time (these slow varying DC shifts may be particularly significant when the signals to be normalized are used to perform analyses over longer times, when gradual, long-term DC drifts may have an impact on the analysis results).

The input signal can be expressed as:

$$x = x_{\mathrm{DC}} + x_{\mathrm{DC}'} + x_{\mathrm{AC}} \tag{2.12}$$

where $x_{\mathrm{DC}'}$ represents the DC shift component, superimposed on the DC component x_{DC} and x_{AC} the rapidly variable, AC, component of the same input signal x.

This is exemplified in the plot of Fig. 31. which shows, as an example of the input signal x to be normalized, a voltage signal V at the output of a voltage converter, e.g. a Buck voltage converter. This voltage signal V has an AC ripple, at a switching frequency f_s, superimposed on a DC component, having a slow variation over time.

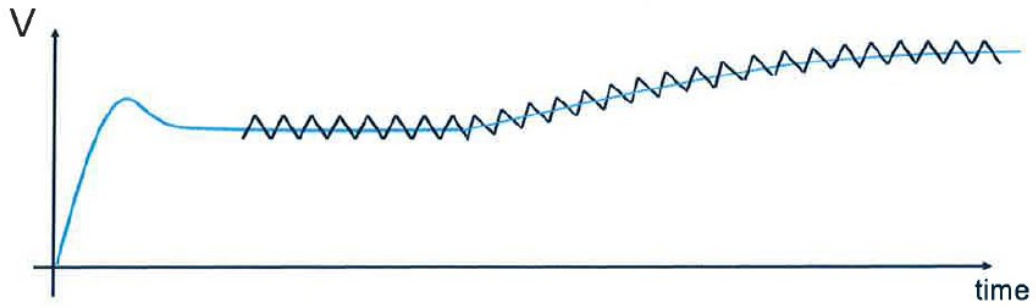


Fig. 31. Shows the Plot of an Exemplary Input Signal to be Normalized.

The Eq. (2.11) therefore can be rewritten as follows:

$$y = G \cdot [x - x_{\mathrm{DC}}] = G \cdot [x_{\mathrm{DC}} + x_{\mathrm{DC}'} + x_{\mathrm{AC}} - x_{\mathrm{DC}}] = G \cdot x_{\mathrm{DC}'} + G \cdot x_{\mathrm{AC}}$$

$$y = G\,(x_{\mathrm{DC}'} + x_{\mathrm{AC}}) \tag{2.13}$$

In other words, the result of the min-max normalization, i.e. the output signal y, can be expressed as the Eq. (2.13) as the sum of a (slow varying) DC shift component and of a (rapidly variable) AC component of the same input signal x, both multiplied by a same gain factor G.

2.6.3 Topology

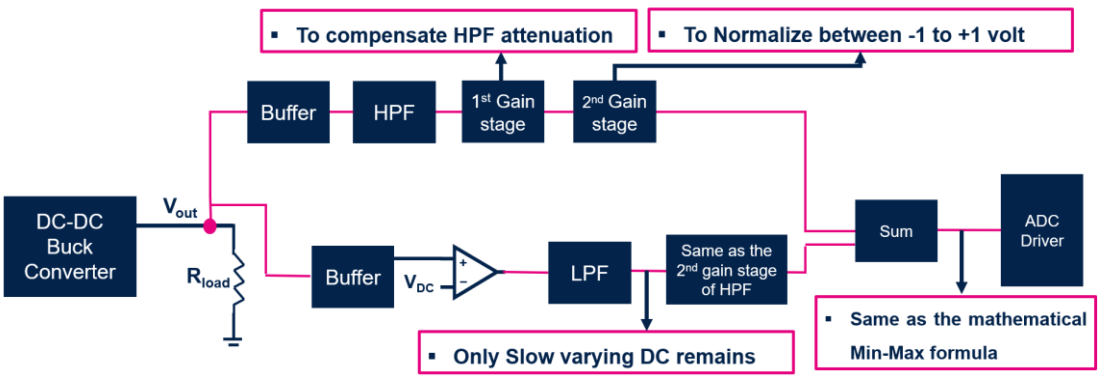


Fig. 32. a Block Diagram of a Normalization Circuit

According to the Eq. (2.13) the normalization circuit applies a common gain factor G to both AC and DC components, ensuring that the summing stage output (representing the normalized signal y) oscillates symmetrically around zero, typically between defined limits -K and K (e.g., between -1 and 1).

In the implementation depicted in Fig. 32. the first circuit path executes high-pass filtering and amplification (by gain factor G) of the input voltage V, generating a first amplified filtered signal $G \cdot V_{\mathrm{AC}}$ (corresponding to $G \cdot x_{\mathrm{AC}}$ in the Eq. (2.13)). Concurrently, the second circuit path performs low-pass filtering and amplification (utilizing the identical gain factor G) of the input voltage, producing a second amplified filtered signal $G \cdot V_{\mathrm{DC}\prime}$ (equivalent to $G \cdot x_{\mathrm{DC}'}$ in the Eq. (2.13)).

The summing stage integrates these amplified filtered signals to produce $G \cdot V_{\mathrm{AC}} + G \cdot V_{\mathrm{DC}\prime}$, which constitutes the normalized output voltage $\overline{\mathrm{V}}$. This normalized signal can subsequently interface with an ADC driver or directly connect to an ADC converter for digital conversion and further processing.

The first circuit path consists of:

- A buffer stage (typically a unity gain amplifier) providing signal isolation.
- A high-pass filter stage that removes DC components and centers the signal around zero.
- A gain stage that amplifies the filtered signal by factor G. The gain stage typically incorporates a compensation sub-stage that mitigates attenuation from filtering operations, followed by an amplification sub-stage implementing the gain factor G. Alternative configurations may omit the compensation sub-stage or distribute amplification across multiple stages.

Importantly, given an input signal frequency fs, the high-pass cut-off frequency exceeds fs/10, preferably higher than fs/5, to ensure proper separation of signal components.

The second circuit path incorporates:

- A buffer stage for signal isolation.

- A subtractor stage that removes the constant DC component $V_{\mathrm{DC}} = (V_{\mathrm{out_min}} + V_{\mathrm{out_max}})/2$, where $V_{\mathrm{out_min}}$ and $V_{\mathrm{out_max}}$ represent the minimum and maximum possible inputs to the normalizer (corresponding to $V_{\mathrm{out_min}} = x_{\mathrm{min}}$ and $V_{\mathrm{out_max}} = x_{\mathrm{max}}$).
- A low-pass filter stage isolating DC-shift components.
- A gain stage applying the factor G (matching the gain of the first circuit path). The low-pass filter output corresponds to the DC shift component $V_{\mathrm{DC}\prime}$, yielding $G \cdot V_{\mathrm{DC}\prime}$ at the second gain stage output.

For optimal performance, given an input signal frequency fs, the low-pass cut-off frequency remains below fs/20, preferably lower than fs/50, and most optimally below fs/100, ensuring effective separation between rapid transients and gradual baseline shifts in the signal.

2.6.4 The Math Behind the New Solution

The proposed normalization architecture can be understood through a systematic mathematical analysis of its constituent stages. Each stage performs a specific mathematical transformation, collectively achieving the complete normalization function. By analyzing these transformations sequentially, we can establish a comprehensive understanding of the signal path and the precise mathematical operations that enable effective normalization across varying input conditions.

1. In the high-pass filter path:

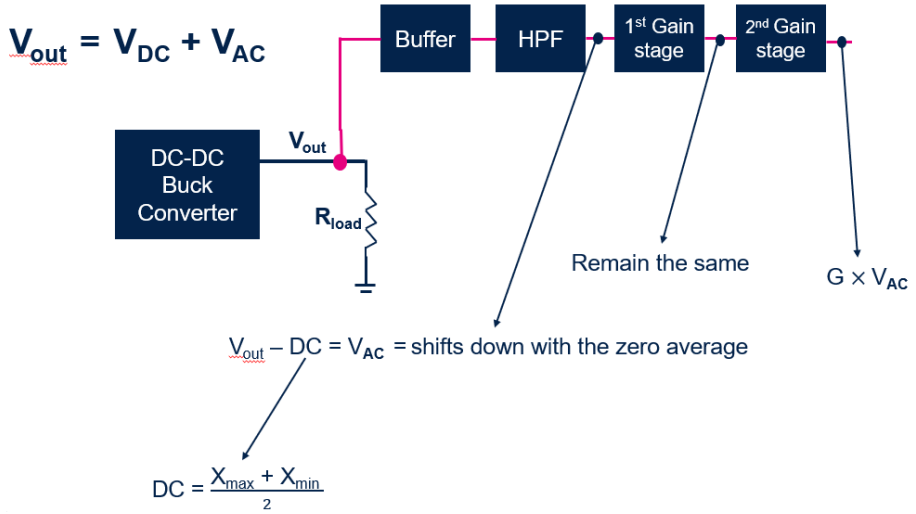


Fig. 33. HPF path

2. In the Low-pass filter path:

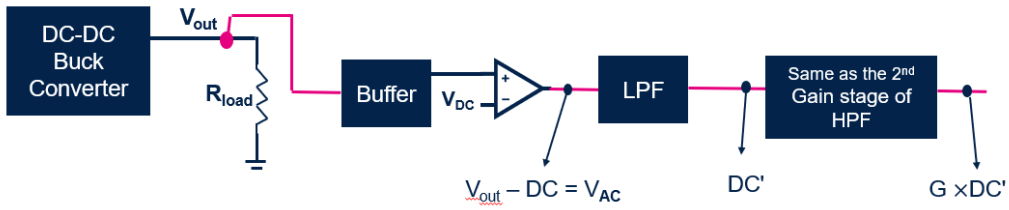


Fig. 34. LPF path

3. Summation:

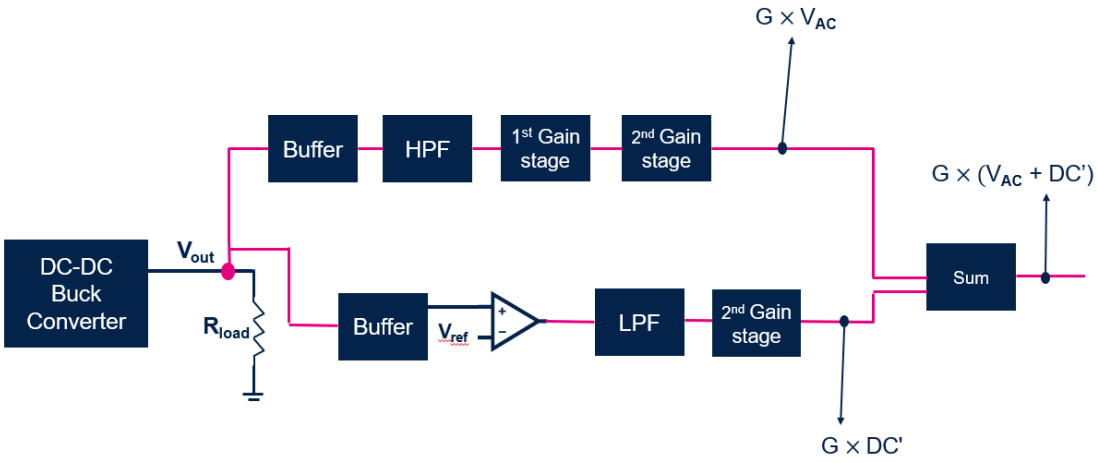
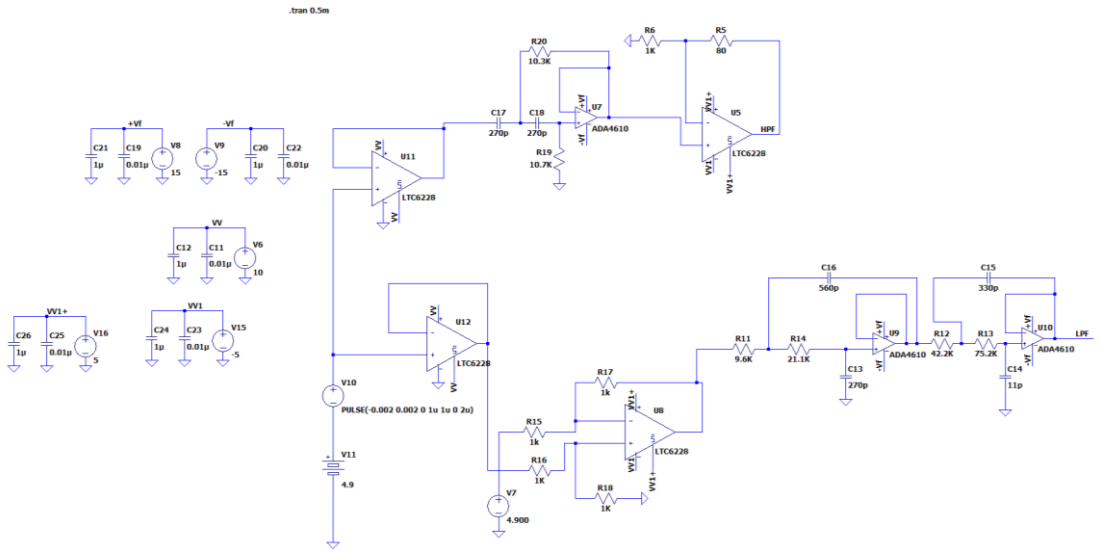
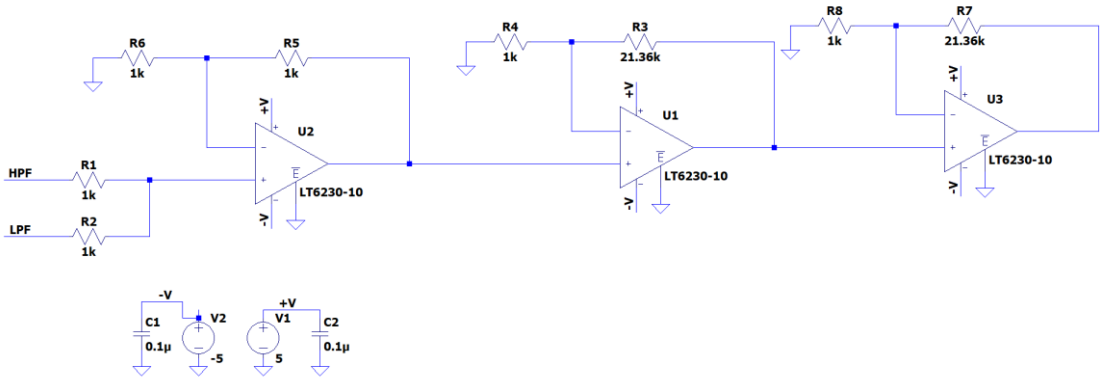


Fig. 35. Summation

2.6.5 Circuit Implementation of the Normalization Circuit



(a)



(b)

Fig. 36. The Full Implementation of the New Solution: a)LPF+HPF b) Summation and Gain Stages

Fig. 36. presents a comprehensive implementation of the novel normalization architecture. In part (a), the schematic illustrates the parallel signal processing paths comprising the low-pass filter (LPF) and high-pass filter (HPF) stages, each designed to isolate specific frequency components of the input signal. Subsequently, as depicted in part (b), these independently processed signals undergo summation through a

precision analog summing circuit, followed by amplification via a carefully calibrated gain stage. This gain factor is meticulously matched to ensure consistent amplification of both signal components, preserving the proportional relationship between low-frequency variations and high-frequency transients. The strategic integration of these complementary filtering techniques with synchronized gain control enables effective normalization while maintaining fidelity across the entire frequency spectrum of interest.

2.6.6 Implementation of Low-Pass Filter for Ripple Attenuation

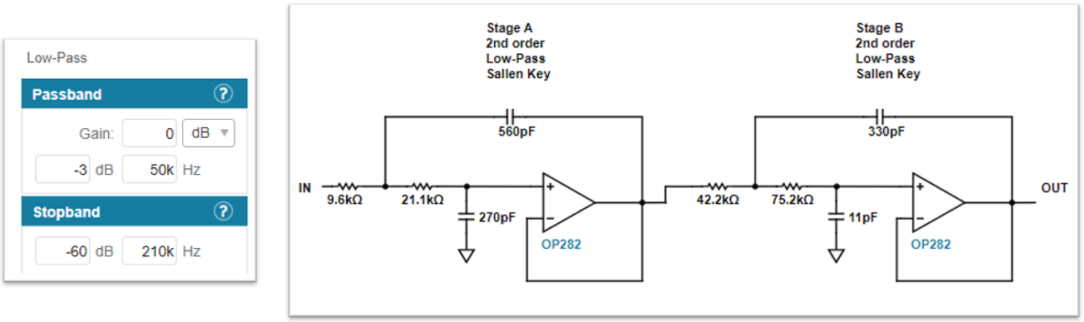


Fig. 37. LPF; 4th Order Chebyshev 0.3dB; 50kHz Passband

Fig. 37. presents a practical implementation of a fourth-order Chebyshev low-pass filter with 0.3 dB passband ripple and a 50 kHz passband cutoff frequency. This filter topology was selected to provide optimal ripple attenuation for this application, where the converter switching frequency of 500 kHz generates output voltage ripple at the same frequency. The filter implementation employs a cascade of two second-order Sallen-Key stages, a configuration that offers an excellent compromise between implementation complexity and filtering performance.

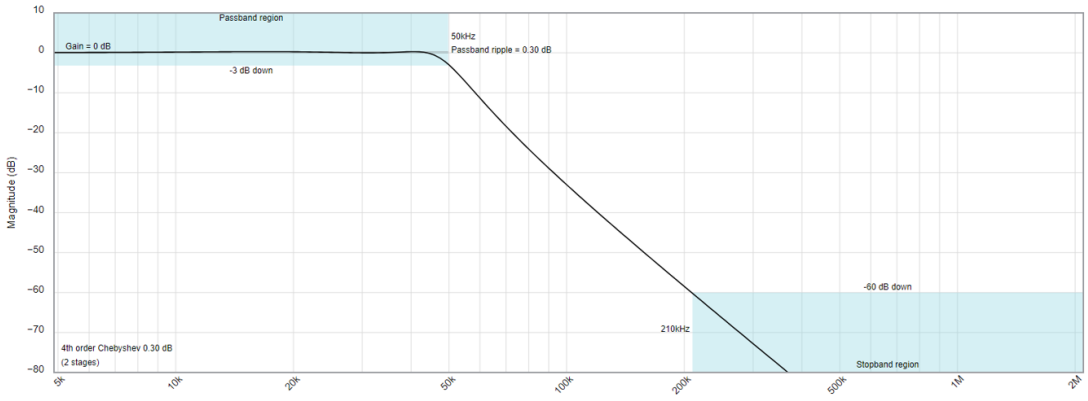


Fig. 38. LPF Specifications

Fig. 38. illustrates the frequency response characteristics of the implemented filter. The magnitude plot clearly demonstrates the filter's performance specifications, with several key parameters explicitly annotated. Within the passband region (below 50 kHz), the response maintains a flat gain of 0 dB with a maximum passband ripple of 0.3 dB, ensuring minimal distortion of low-frequency signal components. At the 50 kHz cutoff frequency, the response exhibits the expected -3 dB attenuation.

The stopband region demonstrates the filter's significant attenuation capabilities, achieving -60 dB rejection at 210 kHz, and maintaining at least -60 dB attenuation across the entire stopband region extending to 2 MHz and beyond. This pronounced attenuation characteristic is particularly important for our application, as it ensures effective suppression of the 500 kHz switching ripple while preserving the low-frequency signal content essential for monitoring aging effects and system performance.

The filter's relatively steep transition from passband to stopband is a characteristic feature of the Chebyshev approximation, which provides superior roll-off compared to other filter types of the same order. This property is particularly advantageous in our application, where maximizing the attenuation at the switching frequency while maintaining a reasonable passband width is paramount for accurate system monitoring and diagnostic capabilities.

2.6.7 High-Pass Filter Implementation for AC Component Extraction

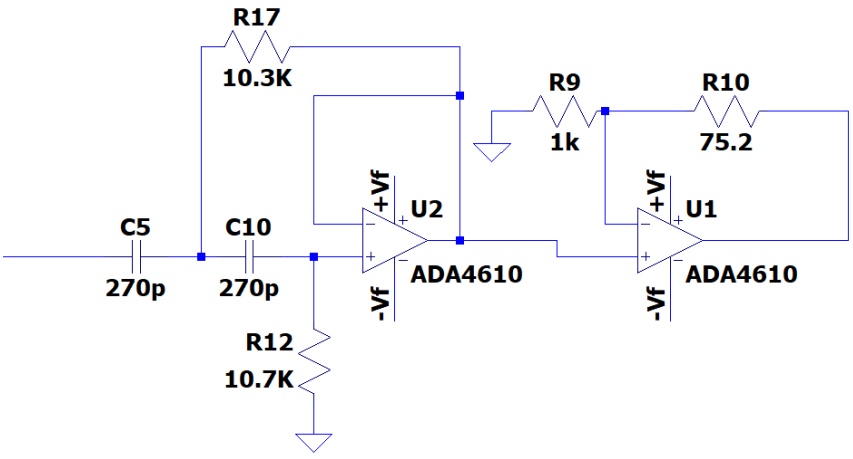


Fig. 39. HPF Implementation

Fig. 39. depicts the implemented high-pass filter (HPF) configuration, which forms a critical component of our dual-filtering approach. The circuit employs a two-stage architecture designed to effectively isolate the AC components of the signal while addressing the inherent attenuation challenges associated with high-pass filtering.

The first stage constitutes the actual high-pass filtering function, effectively blocks DC components while passing the AC signal components above the cutoff frequency.

The second stage, serves as a compensation stage to counteract the attenuation introduced by the high-pass filtering. This stage employs resistors R9 and R10 to establish the gain necessary to restore the amplitude of the passed AC components to appropriate levels for subsequent processing. This gain compensation is particularly important in ensuring that the high-frequency components retain sufficient amplitude for accurate analysis by the neural network after digitization.

The utilization of fine operational amplifiers in both stages is noteworthy, as these devices should offer excellent bandwidth, low noise characteristics, and high slew rates—all critical parameters for processing the high-frequency components of the converter's output signal. The careful design of this HPF stage, working in conjunction with the previously described LPF, enables our normalization approach to separately

process and preserve both the high-frequency AC components needed for operational analysis and the low-frequency DC content essential for aging monitoring.

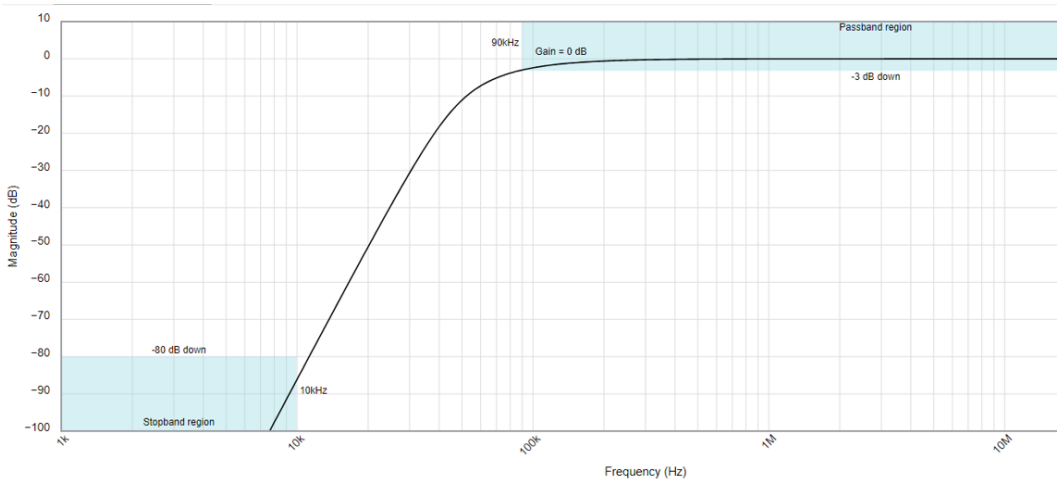


Fig. 40. HPF Specification

Fig. 40. presents the frequency response characteristics of the high-pass filter implementation. Designed to provide optimal phase linearity while achieving the necessary stopband attenuation. This filter topology was selected for its superior transient response characteristics, which are particularly advantageous when analyzing switching waveforms in power conversion systems.

The transition region demonstrates a relatively gradual slope characteristic of Bessel filters, which prioritize constant group delay over steep roll-off. This design choice ensures minimal waveform distortion of the passed high-frequency components, preserving the temporal relationships within the signal that are critical for accurate transient analysis.

At 90 kHz, the response reaches the -3 dB point that defines the filter's cutoff frequency. Beyond this point, the filter enters its passband region where the gain stabilizes at approximately 0 dB, allowing high-frequency components to pass with minimal attenuation. This passband extends well beyond the 500 kHz switching frequency, ensuring that the fundamental and several harmonic components of the switching waveform are preserved for analysis.

The Bessel filter characteristic is particularly important in this application, as it ensures that all frequency components in the passband experience nearly identical time delay,

preserving the waveform shape of complex signals. This property makes the filter especially suitable for temporal analysis of switching transients, which contain critical information about the converter's dynamic performance.

2.6.8 Results and Future Implications

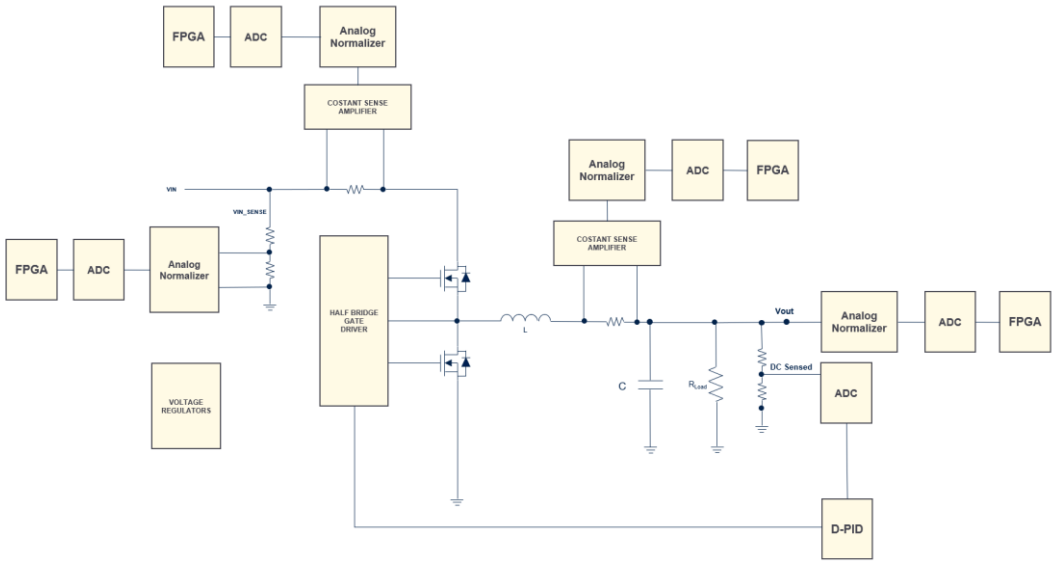


Fig. 41. Testing Board Implementation Block Diagram

The proposed dual-filtering normalization solution presents a highly effective approach for our testing board implementation, particularly for validating the concept of using neural networks for aging prediction in power conversion systems. It is indisputable that this architecture strikes an optimal balance between analog preprocessing complexity and digital processing capabilities. The complementary HPF-LPF configuration effectively preserves both the dynamic AC components and slowly varying DC levels, providing the neural network with the complete spectrum of information necessary for comprehensive aging analysis.

As illustrated in Fig. 41. our testing board implementation features a sophisticated architecture with multiple analog normalizer stages strategically positioned throughout the power conversion system. The board integrates several measurement points where analog normalizers precede ADC and FPGA processing chains, enabling comprehensive data acquisition from various circuit nodes. The half-bridge gate driver forms the core power stage, with current sensing, voltage monitoring, and output

measurements all subjected to appropriate normalization before digital processing. This comprehensive sensing approach, with dedicated normalization for each measurement channel, ensures optimal signal conditioning for all parameters of interest.

The testing board incorporating this normalization architecture offers substantial versatility beyond the initial aging prediction objective. Its ability to simultaneously capture and condition multiple system parameters—including temperature, output voltage and current, as well as input voltage and current—establishes it as a valuable platform for diverse research initiatives. This multi-parameter measurement capability facilitates not only aging studies but also opens avenues for investigating fault detection, efficiency optimization, and thermal management strategies through neural network processing.

When comparing implementation options for future silicon integration, the Gilbert cell multiplier emerges as a particularly promising candidate. Despite the relative complexity of our current discrete implementation with multiple operational amplifier stages, the Gilbert cell offers comparable functionality with significantly reduced silicon area requirements. Its inherent four-quadrant multiplication capability aligns well with the mathematical operations required for normalization, potentially enabling a more compact realization than our current approach.

In comparison to a purely digital normalization solution requiring a high-resolution ADC, our hybrid analog-digital approach demonstrates several advantages. While a high-resolution ADC would occupy substantial silicon area and introduce significant power consumption, our solution distributes the processing burden between optimized analog preprocessing and subsequent digital analysis. The area efficiency advantage becomes particularly pronounced when considering the silicon implementation costs of high-resolution ADCs with sampling rates adequate for capturing the switching transients of interest.

Looking toward future refinements, the potential exists to further miniaturize this solution through custom transistor-level implementations in silicon. Although the precise area requirements and performance characteristics of such an implementation remain to be determined through detailed design and simulation, the fundamental approach appears promising for eventual single-chip integration. The specific optimization strategies and transistor-level architectures represent an intriguing

direction for subsequent research phases, with the current testing board serving as the essential proof-of-concept validation platform.

CHAPTER 3

SYSTEM BOARD DEVELOPMENT

The theoretical frameworks and circuit topologies discussed in preceding chapters necessitate experimental validation through physical implementation. This chapter delineates the development process of a testing platform utilizing discrete components on a printed circuit board (PCB). The experimental verification system serves as a critical bridge between theoretical analysis and practical application, enabling comprehensive characterization of the proposed normalization techniques under realistic operating conditions.

The testing infrastructure has been meticulously designed using Altium Designer, a professional electronic design automation software, to ensure optimal signal integrity, minimal parasitic effects, and reliable measurement capabilities. The schematic design incorporates careful consideration of component selection, signal routing methodologies, and power distribution strategies to faithfully represent the intended circuit behavior while facilitating precise measurements.

This chapter presents the system architecture, detailed circuit schematics, and the underlying design considerations that guided the PCB development process. Particular attention has been paid to the implementation of critical analog signal paths, reference voltage generation, and interface circuits necessary for comprehensive performance evaluation. Furthermore, the design incorporates appropriate test points and measurement interfaces to enable thorough characterization of the normalization circuitry under various operating conditions.

The testing board implementation thus serves dual purposes: validating the fundamental aging prediction methodology while simultaneously establishing a flexible research platform for exploring broader applications of neural network processing in power electronics systems.

3.1 TOPOLOGY

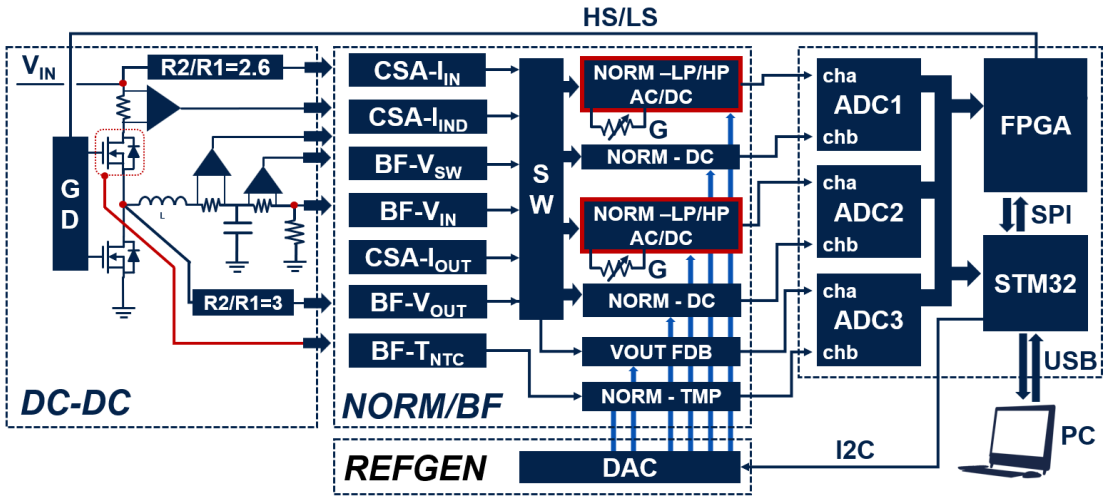


Fig. 42. System Board Topology

The system board topology illustrated in the schematic diagram represents a comprehensive test infrastructure designed for experimental validation of the proposed approach that is a system based on neural network, which indirectly estimated all required parameters with enough precision, that can be integrated together with the power converter in a tiny silicon device. The architecture is strategically partitioned into functional blocks, each dedicated to specific operations within the signal processing chain. The DC-DC unit implements the power supply, the half bridge, the gates driver and sensing of needed parameters.

The voltage signals are properly buffered, and current signals are converted by the CSA (Current Sense Amplifier) blocks. To improve flexibility and to study different solutions, the SW block allows selecting which of the available inputs must be processed by the normalizer block, whose purpose is to scale signals to the input range of the ADC converters. The system provides 4 input channels: two of them, named NORM-DC, are suitable for evaluating constant DC values when high accuracy is not

needed, solely utilize the simple three-stage analog normalizer architecture discussed in previous chapters, without high-pass filtering functionality. The others, named NORM-LP/HP, provide more accuracy in processing the signal and implement the HPF + LPF normalizer configuration, which can process both AC and DC signal components through its high-pass and low-pass filtering capabilities. Each of the two data converters, ADC1 and ADC2, has two input channels with an input range between -1V and 1V, and provides data conversion to the digital domain for the 4 available channels. The first channel of ADC3 is used to acquire V_{OUT}, needed to compute loop error, by subtracting the V_{REF}, as shown in Fig. 5. This error is the input of the digital PID that properly tunes the duty cycle of the HS and LS signals, regulates V_{OUT} and closes the feedback loop. The second channel of ADC3 is dedicated to the temperature sensing, measured by a NTC close to the high side power MOS. All acquired data can be used as input to a neural network designed in VHDL RTL and implemented in the FPGA or programmed into a STM32 MCU. The first solution is enabled by an FMC connector that allows data communication with a Digilent Nexys Video board, shown in Fig. 42. (left side), equipped with an Artix-7 FPGA, used to test digital hardware that can be integrated into a silicon device. The second solution exploits the NUCLEO-H563ZI MCU board shown in Fig. 43. (right side) for verifications, further developments and testing of predictive maintenance algorithms. The STM32 MCU is also required to configure system settings, to set output voltage references in the REFGEN block, to collect and transfer measured data to a computer. Processed data will be used to define a physical data set, which will be employed instead of the data set extracted from model simulations. This will offer a more reliable study of the proposed methodology and, together with the designed board, represents a complete verification platform for different supervisor and monitor algorithms, supporting power converter systems.

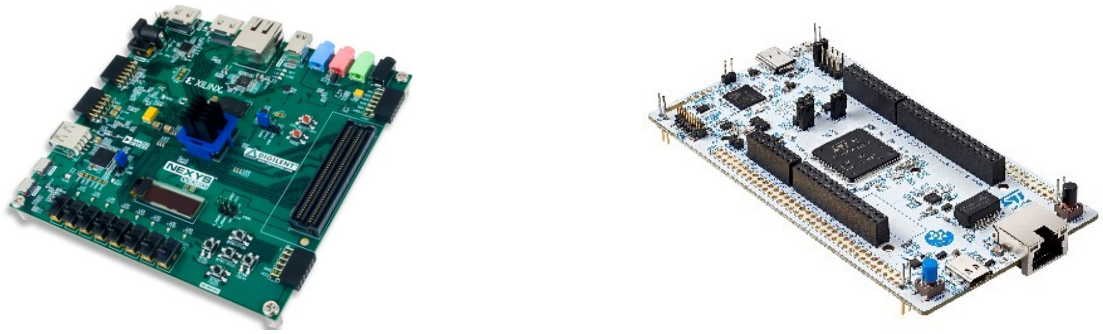


Fig. 43. Digilent Nexis Video and NUCLEO-H563ZI boards.

The most relevant parts of the board development are the sensing circuitry, and the digital design of the neural network. They have a big impact on the accuracy of acquired data and the total area occupation on an integrated silicon device.

In the RTL design, the SER2PAR block of Fig. 42. was used to collect the 8 samples of V_{OUT} and I_{IND} from the ADC. When all needed input values are available into the array, the neural network inference is executed. A synchronization between ADC sampling and the SER2PAR block is required to ensure the desired 4 samples, which in this work have indices 4, 6, 7 and 9 in the PWM period, are correctly kept. Since the regulation of the DC-DC converter is done by a digital PID that tunes the power MOS gate driver, the rising edge of the digital signal HS is useful to properly start the sampling window. The implemented RTL of the overall controller allows choosing up to 16 samples in a PWM period and the index of all samples from the 1^{st} to the 16^{th}. It also provides the possibility to trim the delay of the sampling window with respect to the start reference i.e., the rising edge of HS, and to sample each value either inside the same PWM period or each value in a different PWM period. After samples are acquired, the average of up to 16 samples can be computed and a fine digital gain and offset can be applied to each sample.

3.1.1 Simulated Three-Dimensional Model

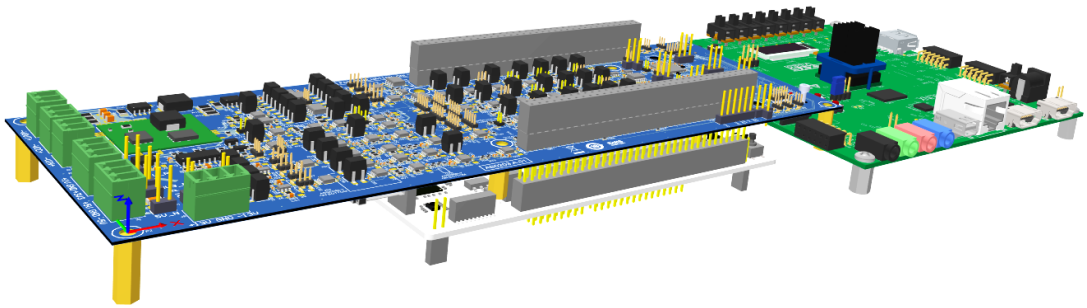


Fig. 44. Isometric View

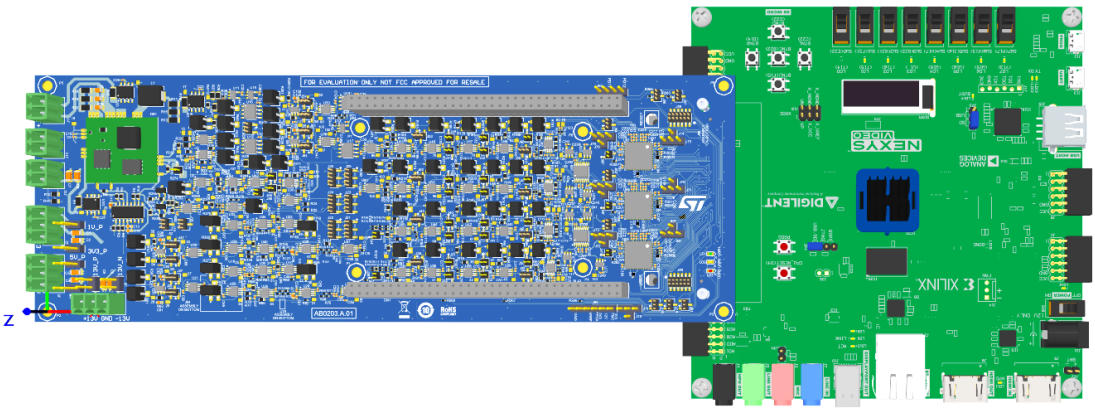


Fig. 45. Top View

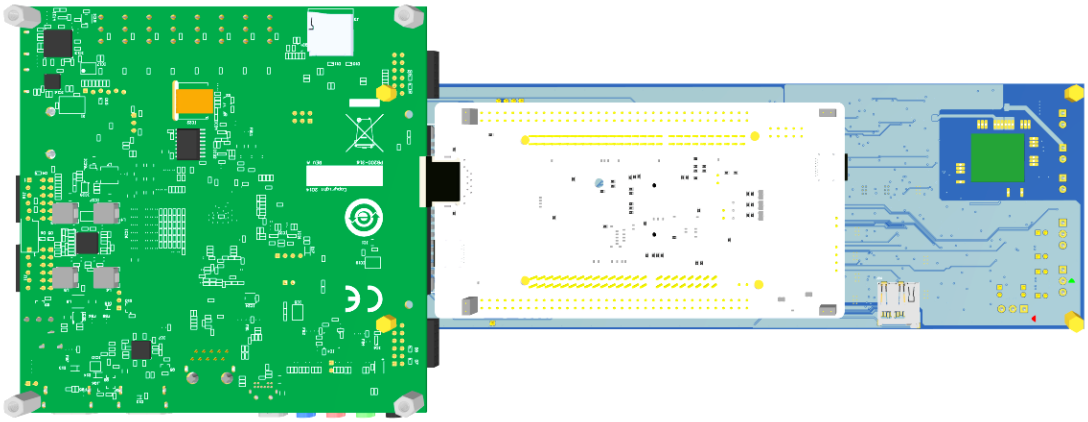


Fig. 46. Bottom View

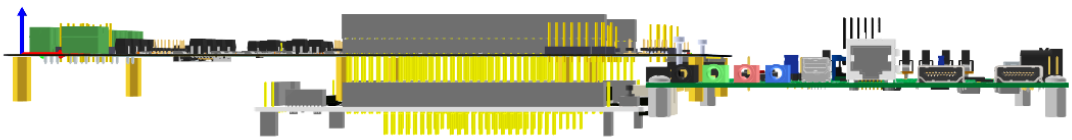


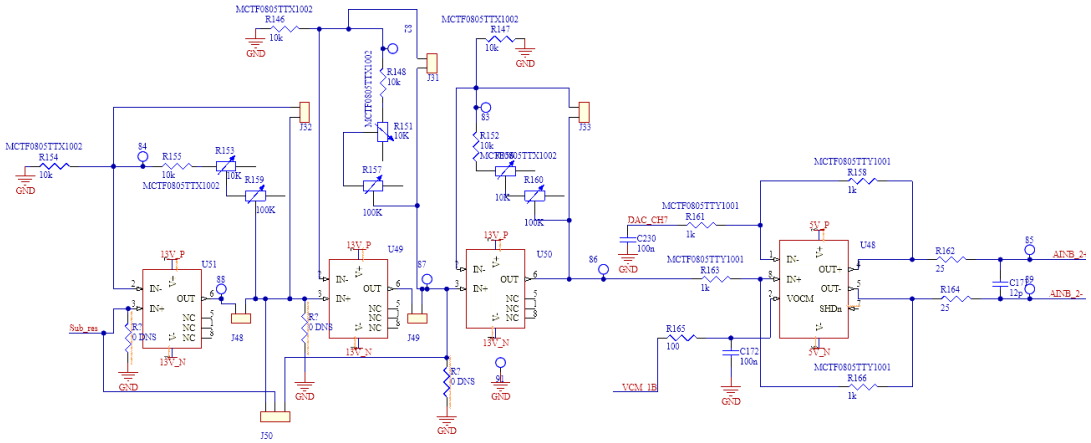
Fig. 47. Front View

The experimental verification platform was designed as a comprehensive testing infrastructure for validating the proposed normalization techniques. Figure 44 presents an isometric visualization of the complete system board, illustrating the three-dimensional arrangement of components and interconnections. Figure 45 provides a top-view perspective of the assembled board, revealing the meticulous component placement and signal routing strategies employed to minimize parasitic effects and electromagnetic interference. Complementing these views, Figure 46 depicts the bottom layer of the printed circuit board, showcasing the ground plane implementation and interconnection technologies utilized for signal integrity preservation. Figure 47 offers a front-view cross-section of the experimental apparatus, highlighting the vertical clearances and mechanical interfaces between the main board and peripheral connectors. This multi-perspective representation demonstrates the comprehensive design approach undertaken to ensure proper functionality of both the normalization circuits and the supporting infrastructure necessary for experimental characterization.

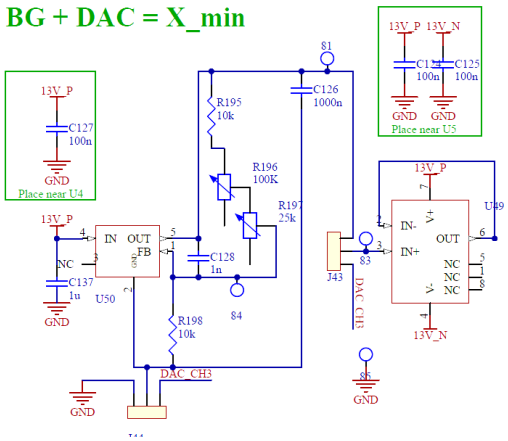
3.2 SIMPLE NORMALIZER

The schematic presented in Fig. 48. illustrates the detailed implementation of the simple normalizer circuit discussed in Chapter 2. This design embodies the multi-stage normalization approach with particular attention to practical considerations for signal integrity and adjustability.

The circuit architecture follows a sequential processing chain comprising several distinct stages. At the input, buffer amplifiers provide critical impedance isolation between the sensing nodes and the normalization circuitry, ensuring that measurement points are not loaded and signal fidelity is maintained. This isolation is essential for accurate signal acquisition from high-impedance sources within the power converter.



(a)



(b)

Fig. 48. Simple Normalizer

As depicted in Fig. 48. Part (b), the first normalization stage, labeled "BG + DAC = X_min," implements the crucial subtraction operation where the input signal X is offset by X_min. This reference generation subsystem merits special attention for its innovative approach to precision reference generation. Rather than using a fixed reference, the circuit incorporates a flexible bandgap reference whose output voltage can be precisely adjusted via potentiometers. This adjustable bandgap is further enhanced by adding a digitally controlled offset voltage from a high-precision 16-bit DAC. This hybrid approach effectively enables the bandgap reference to start from the DAC voltage rather than ground, providing exceptionally fine-grained control over the X_min reference value.

As presented in Fig. 48. Part (b), following the subtraction stage, the signal traverses through three cascaded amplification stages utilizing OPA828 operational amplifiers. These amplifiers were specifically selected for their excellent performance characteristics, particularly their extremely low input bias current in the picoampere range and minimal offset voltage below 300 microvolts. Each stage incorporates adjustable feedback resistors implemented as potentiometers, enabling precise gain calibration. The design utilizes both 10kΩ and 100kΩ potentiometers to provide both fine and coarse adjustment capabilities, offering wide-ranging gain control.

The implementation of three separate gain stages is a deliberate design decision necessitated by the extreme dynamic range requirements of the application. In worst-case scenarios where the buck converter output exhibits voltage variations as small as 4mV peak-to-peak, an overall gain of approximately 500 is required to normalize the signal to the ADC's input range. Achieving such high gain in a single stage would introduce significant gain-bandwidth product limitations. The multi-stage approach distributes the gain requirement, preserving bandwidth while maintaining stability.

The circuit incorporates several additional refinements to enhance performance. Resistors at the positive terminals of each operational amplifier stage provide flexibility for input bias current offset compensation. The design deliberately employs 10kΩ resistors instead of 1kΩ to reduce current flow through the signal path, which empirically improves signal fidelity. While this approach theoretically increases resistor thermal noise, the improved accuracy from reduced current flow outweighs this disadvantage. The noise concern can be mitigated by adding appropriately sized compensation capacitors in parallel with the feedback resistors of each stage, creating low-pass filtering that suppresses high-frequency noise components.

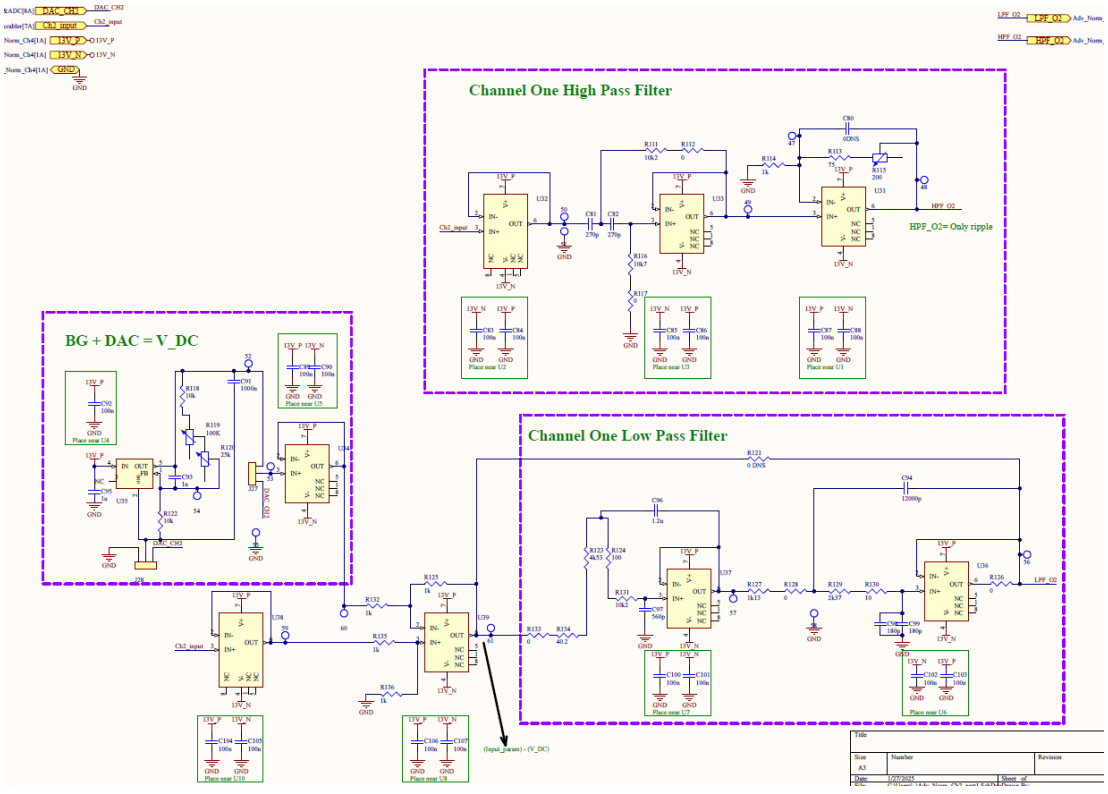
Multiple test points and jumpers are strategically placed throughout the circuit to enable selective bypassing of individual gain stages when the application requires less than maximum gain. This adaptability allows for optimized performance across varying signal conditions.

The final stage employs a fully-differential operational amplifier to convert the single-ended normalized signal to a differential output compatible with the ADC's input requirements. This differential conversion enhances common-mode noise rejection and optimizes the signal-to-noise ratio at the converter interface.

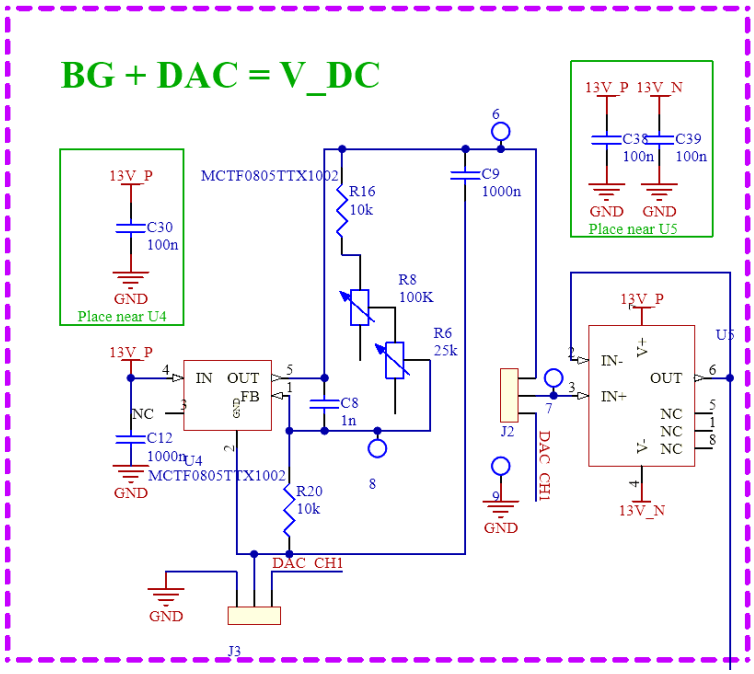
Power supply integrity is maintained through comprehensive bypass capacitor implementation for each operational amplifier stage. The PCB design incorporates three separate ground planes dedicated to analog circuitry, digital components, and power supplies respectively, minimizing interference between these functionally distinct domains.

This meticulously designed normalizer circuit exemplifies the practical translation of theoretical normalization principles into a robust implementation suitable for experimental validation, with particular emphasis on precision, adjustability, and signal integrity.

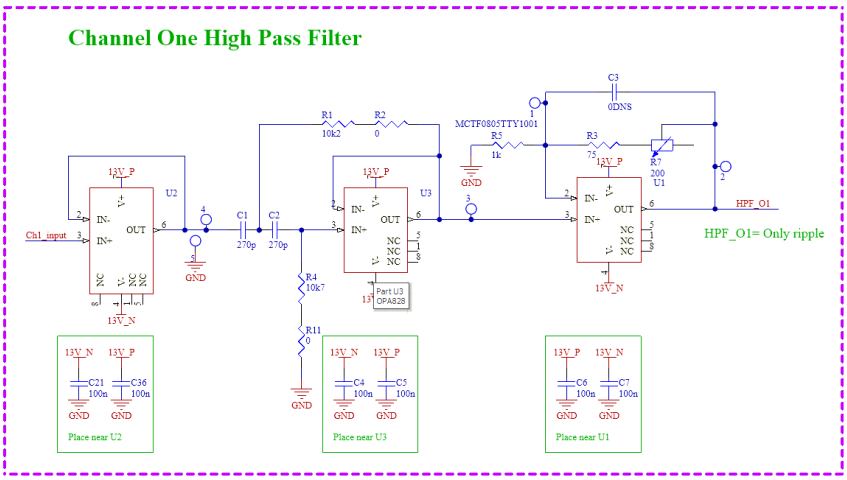
3.3 Advanced Normalizer



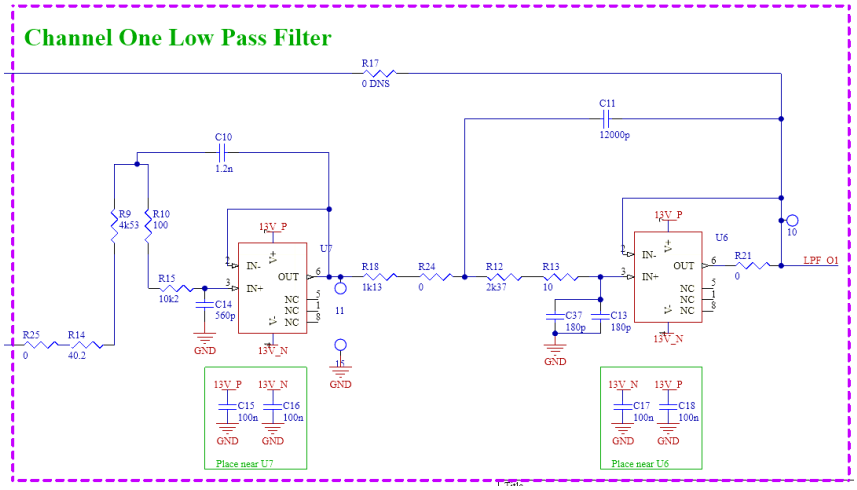
(a)


BG + DAC = V_DC
13V_P
C30
100n
GND
Place near U4
MCTF0805TTX1002
R16
10k
C9
1000n
13V_P 13V_N
C38
100n
C39
100n
GND GND
Place near U5
R8
100K
R6
25k
13V_P
IN OUT
FB
NC
GND
C8
1n
C12
1000n
U4
MCTF0805TTX1002
GND
R20
10k
DAC_CH1
GND
J3
J2
DAC CH1
GND
13V_P
U5
IN-
IN+
V+
V-
OUT
NC
NC
NC
13V_N

(b)


Channel One High Pass Filter
C3
0DNS
R1
10k2
R2
0
MCTF0805TTY1001
R5
1k
R3
75
R7
200
U1
13V_P
U2
U3
Ch1_input
C1
270p
C2
270p
R4
10k7
R11
0
GND
HPF_O1
HPF_O1= Only ripple
13V_N
Part U3
OPA828
C21
100n
C36
100n
Place near U2
C4
100n
C5
100n
Place near U3
C6
100n
C7
100n
Place near U1

(c)



(d)

Fig. 49. a) A Complete Advanced Normalizer b) Reference Selection c) Channel One High-Pass Filter d) Channel one Low-Pass Filter

The schematic in Fig. 49. part (a) illustrates the implementation of the advanced normalizer architecture incorporating both high-pass and low-pass filtering paths. This design represents a significant advancement over the simple normalizer previously discussed, offering enhanced capabilities for signal decomposition and processing.

Central to this advanced normalizer is the innovative approach to reference selection. Rather than utilizing X_min as in the simple normalizer, this architecture requires the provision of X_DC, which represents the average value of the input signal calculated as (X_min + X_max)/2. This fundamental shift in reference selection offers substantial practical advantages. There is no doubt that this approach simplifies the reference generation for signals with negative excursions, such as those found at switching nodes. While generating precise negative voltage references presents considerable design challenges, the X_DC value remains consistently positive for most power converter signals, significantly simplifying the reference generation circuitry.

The circuit implementation is divided into three primary functional blocks clearly delineated in the schematic. The first block, as demonstrated in Fig. 49. part (b), labeled "BG + DAC = V_DC," employs a similar hybrid approach to reference generation as seen in the simple normalizer, combining an adjustable bandgap reference with a precision DAC to establish the X_DC reference value with high accuracy.

The second block, as visualized in Fig. 49. part (c), "Channel One High Pass Filter," implements a second-order high-pass filter that selectively extracts the AC components of the input signal. This filtering configuration effectively eliminates the DC content while preserving the transient information and ripple characteristics critical for comprehensive system analysis.

The third block, as represented in Fig. 49. part (d), "Channel One Low Pass Filter," implements a fourth-order low-pass filter that isolates the DC and low-frequency components of the input signal. This more complex filter topology provides superior stopband attenuation compared to simpler first-order designs, ensuring effective separation of frequency components. The implementation utilizes multiple operational amplifier stages with carefully selected resistor and capacitor values to establish the desired filter characteristics.

Buffering amplifiers are strategically placed at the filter inputs to ensure that the parallel signal paths do not create undesirable loading effects or impedance mismatches that could compromise signal integrity. This isolation is critical for maintaining the accuracy of both frequency-selective paths.

The fundamental advantage of this architecture lies in its ability to separately process and normalize the AC and DC components of the input signal. By decomposing the signal into these constituent components, we effectively eliminate the constant DC offset that would otherwise dominate the signal characteristics. This approach circumvents the limitations encountered when attempting to amplify signals with substantial DC components, as the removal of the static DC level allows for significantly higher gain factors to be applied to the dynamic portions of the signal without encountering saturation limitations. The high-pass filter path captures transient information and ripple characteristics while the low-pass filter path tracks only the slowly varying DC components, both of which can be processed independently before recombination. When these processed components are subsequently summed, the resulting signal preserves all essential information while being properly conditioned for further amplification, enabling much more effective utilization of the available dynamic range in subsequent stages. In subsequent schematics, the outputs from these high-pass and low-pass filter paths will be summed and further amplified to produce the final normalized output. This recombination process allows for independent

optimization of each signal component before reconstitution, resulting in superior normalization performance particularly for signals with complex frequency content such as those found in switching power converters.

The implementation of second-order high-pass and fourth-order low-pass filter topologies represents a deliberate design decision to achieve optimal frequency selectivity while maintaining manageable circuit complexity and component count. This balanced approach ensures practical implement ability while delivering the performance necessary for effective signal normalization.

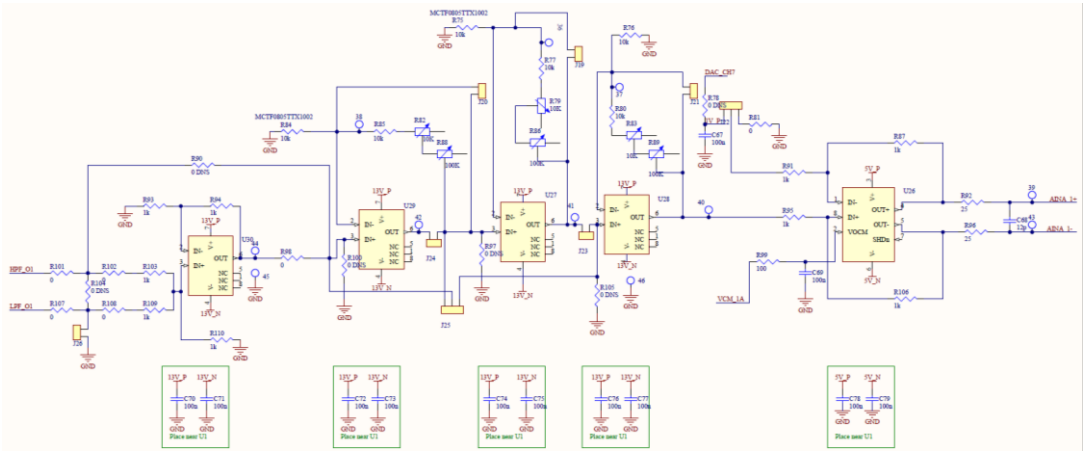


Fig. 50. Advanced Normalizer Gain Stages

The schematic presented in Fig. 50. illustrates the signal recombination and amplification stages that complete the advanced LPF + HPF normalizer architecture. This circuit continues the signal processing chain following the separate high-pass and low-pass filtering paths discussed previously.

At the input stage of this circuit, a precision summation amplifier performs the critical function of recombining the separately processed HPF_O1 and LPF_O1 signals. This operational amplifier is configured as a summing circuit with input resistors establishing the appropriate weighting for each signal component. The summation operation effectively reconstitutes the complete signal while preserving the advantages gained through the separate processing of AC and DC components.

Following the summation stage, the circuit implements three cascaded gain stages that are structurally identical to those employed in the simple normalizer architecture. These sequential amplification stages provide the flexibility to achieve high gain factors—up to 500 in the most demanding scenarios—while distributing the gain to maintain adequate bandwidth and stability. Each stage incorporates adjustable feedback elements implemented as potentiometers, allowing precise calibration of the gain distribution across the amplification chain.

The implementation includes numerous test points and jumper connections that enable selective bypassing of individual gain stages when the full amplification capability is not required. This adaptability allows the circuit to be optimized for varying input signal characteristics and normalization requirements.

At the final stage, a fully-differential operational amplifier converts the single-ended processed signal into a differential output format required by the analog-to-digital converter. This differential driver stage employs precision resistors to establish the appropriate common-mode and differential signal characteristics.

Throughout the circuit, meticulous attention to power supply integrity is evident through the comprehensive implementation of bypass capacitors for each operational amplifier. These components are organized in power supply decoupling blocks, strategically placed near each active device to minimize supply noise and ensure clean operation of the analog signal chain.

3.4 DAC's and ADC's

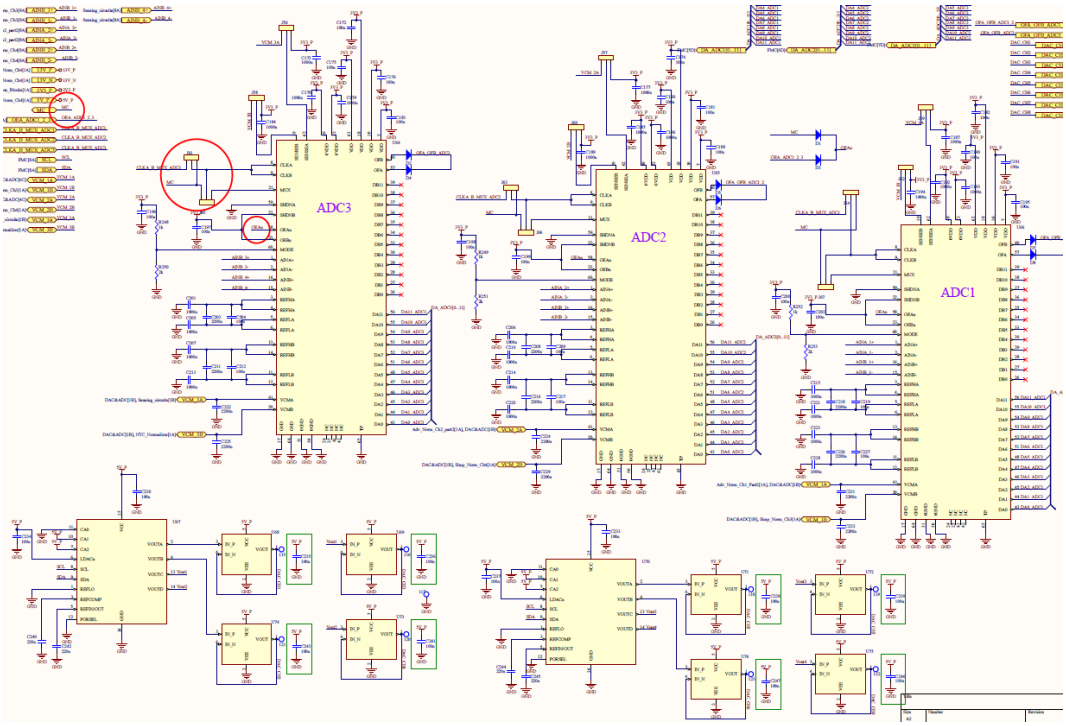


Fig. 51. DAC's and ADC's

The schematic depicted in Fig. 51. illustrates the comprehensive data conversion infrastructure that forms a critical bridge between the analog signal conditioning circuits and the digital processing domain. This subsystem comprises analog-to-digital converters (ADCs) and digital-to-analog converters (DACs).

The design employs three LTC2292IUP dual-channel analog-to-digital converters (labeled ADC1, ADC2, and ADC3), providing a total of six digitization channels. These converters receive the differentially-driven normalized signals from the previously described normalization circuits. Each ADC is configured with appropriate input termination, supply filtering, and reference conditioning to ensure optimal conversion accuracy. The careful layout includes AC coupling capacitors at the inputs and ground reference points necessary for maintaining signal integrity throughout the conversion process.

The digitized data from these converters is routed to the digital processing system where the neural network algorithms are implemented. This arrangement enables real-

time acquisition and processing of the normalized signals, including the critical temperature measurements derived from the NTC thermistor circuits discussed earlier.

The system incorporates two high-precision digital-to-analog converters that generate the reference voltages essential for proper system operation. Notably, each DAC output is followed by a dedicated buffer amplifier, providing critical impedance isolation and current-driving capability. These buffers serve two essential functions: they enable the DACs to drive high capacitive loads without stability issues, and they provide isolation that prevents loading effects from disturbing the precision of the reference voltages. This buffering stage is particularly important as it ensures that fluctuating current demands in the downstream circuits do not reflect back to compromise the reference accuracy.

These DACs fulfill multiple critical functions:

1. Generation of precise X_min references required by the simple normalizer circuits
2. Production of X_DC (average) references needed by the advanced LPF+HPF normalizers
3. Creation of accurate reference voltages for the error amplifier that facilitates closed-loop control

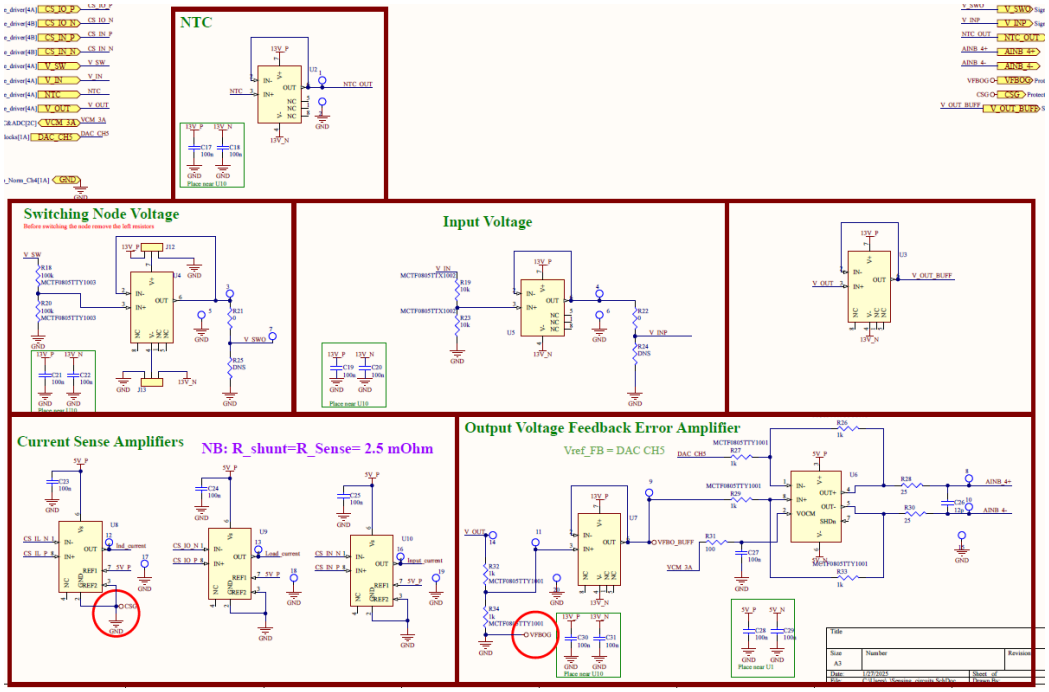
The DAC implementation includes comprehensive filtering and buffering to ensure stable, low-noise reference voltages. This attention to signal integrity is essential as these references directly impact the accuracy of the entire normalization process.

The interfaces between these data converters and the digital processing system are carefully designed to maintain signal integrity, with proper consideration for digital isolation, clock distribution, and power supply management. The entire data conversion subsystem incorporates extensive decoupling capacitors and regulated supply voltages to minimize noise and ensure reliable operation.

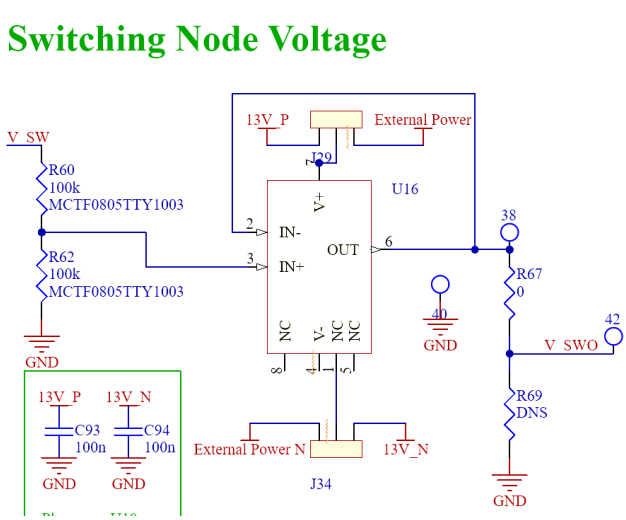
This bidirectional data conversion infrastructure enables not only the acquisition of normalized analog signals for neural network processing but also provides the means for adaptive reference adjustment based on system conditions and requirements, creating a complete feedback loop between the analog and digital domains.

3.5 SENSING CIRCUITRY

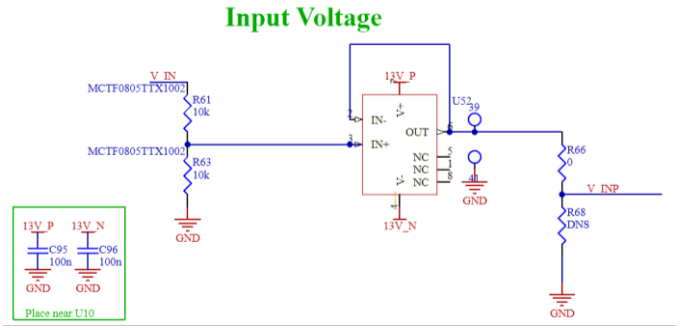
The schematic presented in Fig. 52. (a) illustrates the comprehensive sensing infrastructure that interfaces between the DC-DC buck converter and the normalization circuits. This signal acquisition subsystem is partitioned into five distinct functional blocks, each serving a specific measurement purpose.



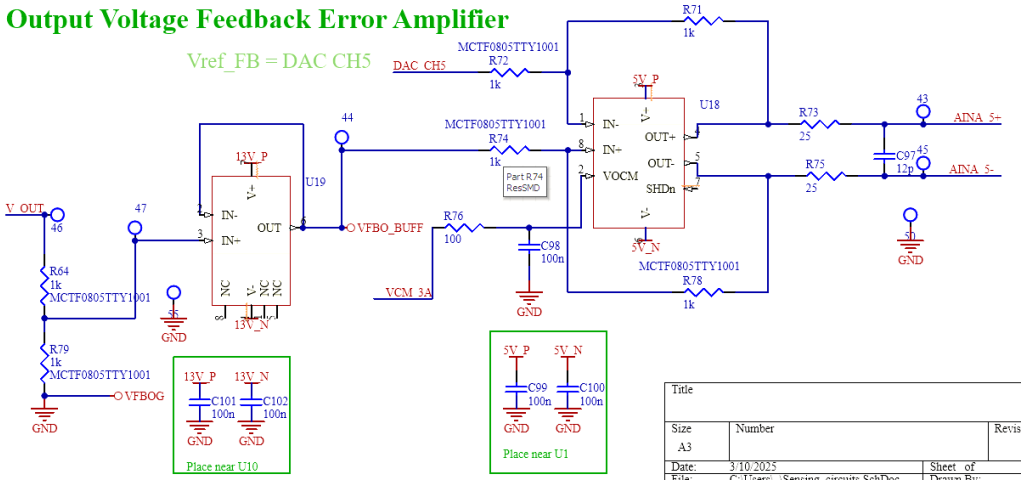
(a)



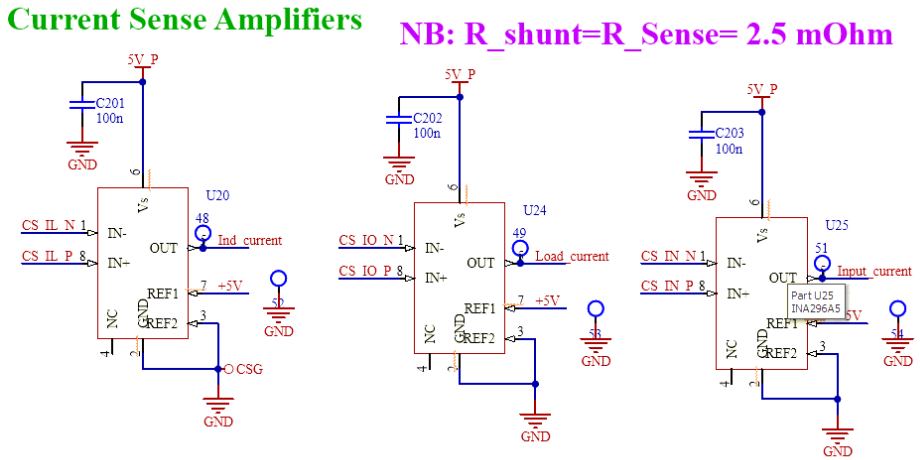
(b)


Input Voltage
V_IN
MCTF0805TTX1002
R61
10k
MCTF0805TTX1002
R63
10k
GND
13V_P
U52
IN-
IN+
OUT
NC
NC
NC
V+
V-
13V_N
R66
0
V_INP
R68
DNS
GND
13V_P
13V_N
C95
100n
C96
100n
GND
GND
Place near U10

(c)


Output Voltage Feedback Error Amplifier
Vref_FB = DAC CH5
DAC_CH5
R72
1k
MCTF0805TTY1001
R71
1k
5V_P
U18
IN-
IN+
VOCM
OUT+
OUT-
SHDn
V+
V-
5V_N
R73
25
R75
25
43
AINA_5+
45
AINA_5-
C97
12p
MCTF0805TTY1001
R74
1k
Part R74
ResSMD
44
U19
13V_P
13V_N
V_OUT
46
47
R64
1k
MCTF0805TTY1001
R79
1k
MCTF0805TTY1001
VFBOG
VFBO_BUFF
R76
100
C98
100n
VCM_3A
MCTF0805TTY1001
R78
1k
C101
100n
C102
100n
Place near U10
5V_P
5V_N
C99
100n
C100
100n
Place near U1
Title
Size
A3
Number
Revis
Date:
3/10/2025
Sheet of

(d)


Current Sense Amplifiers
NB: R_shunt=R_Sense= 2.5 mOhm
5V_P
C201
100n
U20
CS_IL_N
CS_IL_P
IN-
IN+
OUT
Vs
REF1
REF2
NC
GND
48
Ind_current
+5V
CSG
C202
100n
U24
CS_IO_N
CS_IO_P
49
Load_current
C203
100n
U25
CS_IN_N
CS_IN_P
51
Input_current
Part U25
INA296A5
5V
GND

(e)

Fig. 52. Sensing Circuitry: a) The Whole Schematic b) Switching Node Voltage Sensing c) Input Voltage Sensing d) Differential Sensing of the Output Voltage e) Current Sense Amplifiers

The "NTC" block in the upper section implements a temperature sensing circuit utilizing a negative temperature coefficient thermistor positioned adjacent to the high-side transistor. This circuit employs a buffer amplifier to provide impedance isolation, ensuring that the measurement does not affect the thermal characteristics of the component being monitored. The NTC signal path incorporates appropriate bypass capacitors to ensure clean power supply to the buffer amplifier.

As shown in Fig. 52. part (b), the "Switching Node Voltage" block employs a voltage divider network consisting of precision resistors to scale down the high-voltage switching node signal to a level compatible with the subsequent processing stages. This voltage division is necessary because the switching node voltage often exceeds the supply voltage range of the operational amplifiers and buffers in the circuits. The divider is followed by a buffer amplifier that provides isolation, preventing any loading effects that might disturb the normal operation of the power converter. This voltage division introduces a scaling factor that must be compensated by increased gain in the normalization stages.

Similarly, as illustrated in Fig. 52. part (c), the "Input Voltage" block implements voltage division and buffering for the input supply voltage. This arrangement enables accurate monitoring of the input voltage without perturbing the power converter operation.

Referring to Fig. 52. Part (e), the "Current Sense Amplifiers" section utilizes specialized integrated current sense amplifiers (INA296) coupled with precision low-resistance shunts (2.5 milliohm). These components are carefully selected to minimize power loss while providing adequate signal levels for accurate current measurement. A significant advantage of these amplifiers is their bidirectional capability, enabling measurement of both forward and reverse inductor currents—a critical parameter for comprehensive power converter analysis. The circuit implementation includes three separate current sensing channels for monitoring input current, inductor current, and output current.

Evident from Fig. 52. part (d), the "Output Voltage Feedback Error Amplifier" block implements differential sensing of the output voltage, comparing it with a precision reference voltage derived from DAC CH5. This error amplifier generates a feedback signal that can be used for PID controller tuning. The implementation employs a fully-differential operational amplifier that converts the single-ended error signal to differential outputs suitable for the ADC interface.

Throughout the sensing circuitry, careful attention has been paid to power supply decoupling, with dedicated bypass capacitors for each active component. Additionally, the design incorporates numerous test points (labeled with signal names) that facilitate debugging and performance verification during testing.

This sensing infrastructure addresses several critical design challenges:

1. It provides appropriate signal scaling to accommodate wide voltage ranges within the limited supply voltage constraints of the processing circuits
2. It maintains signal integrity through careful buffering and isolation
3. It enables accurate current measurement with minimal impact on power conversion efficiency
4. It supports comprehensive monitoring of all critical parameters necessary for both neural network training and control system implementation

While the voltage division in the voltage sensing paths necessitates higher gain in the subsequent normalization stages, the three-stage gain architecture discussed previously offers sufficient amplification capability to compensate for this scaling without compromising performance.

3.6 DC-DC BUCK CONVERTER

The schematic illustrated in Fig. 53. presents the comprehensive implementation of the DC-DC buck converter that serves as the power processing platform for the experimental system. This carefully designed power stage incorporates flexibility features that enable parametric variation for experimental characterization.

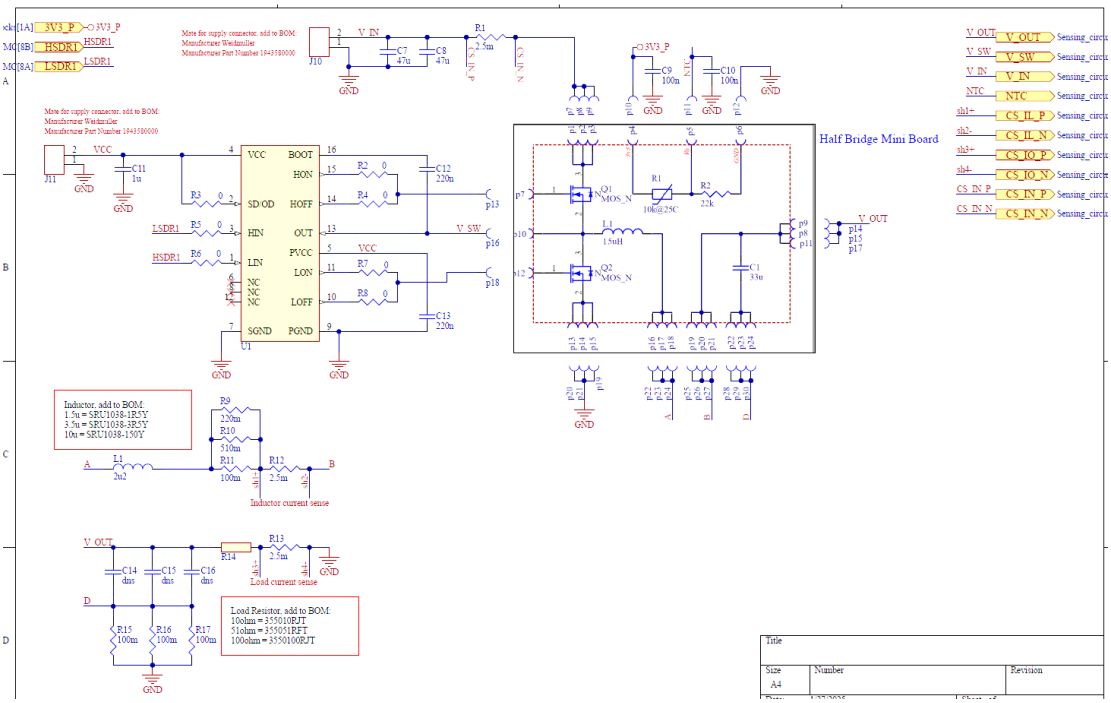


Fig. 53. DC-DC Buck Converter

The converter is constructed around a specialized gate driver IC that interfaces with the external control signals (HSDR1, LSDR1) to drive the power MOSFETs within the "Half Bridge Mini Board" module. This driver IC incorporates critical timing control circuits that manage dead-time insertion, bootstrap capacitor charging, and level-shifting functions necessary for proper half-bridge operation.

This arrangement contains two N-channel MOSFETs configured in a high-side/low-side configuration, with appropriate gate resistors to control switching transition rates. The modular implementation facilitates thermal management and provides shielding from electromagnetic interference.

A particularly noteworthy aspect of this design is the configurable output filter section, which offers exceptional flexibility for experimental characterization:

1. The inductor section features a series connection capability, with available inductor values (1.5µH, 3.5µH, or 10µH using SRU1038 series components). The implementation includes small-value resistors in series with the inductor, which serve as current sensing points without significantly impacting converter efficiency and also flexible ESL.

2. The output capacitor bank consists of multiple parallel capacitors with associated parallel resistors. This configuration allows selective population of different capacitor values and types, enabling investigation of various output capacitance profiles.
3. Dedicated current sensing resistors are strategically positioned for both inductor current and load current measurement, enabling comprehensive monitoring of converter operation.

All critical signals are routed to the sensing circuitry described in previous schematics, as indicated by the labeled connection points on the right side of the diagram (V_OUT, V_SW, V_IN, NTC, etc.). These connections establish the complete signal path from the power converter to the normalization circuitry and ultimately to the neural network processing system.

This highly configurable power stage design enables comprehensive experimental validation of the normalization techniques under various operating conditions. The ability to modify key parameters such as inductor value, output capacitance, ESR, and load resistance provides a versatile platform for characterizing system performance across a wide range of operating scenarios. This flexibility is essential for developing robust normalization techniques that can accommodate the diverse characteristics encountered in practical power conversion applications.

CONCLUSION AND FUTURE WORK

This thesis has presented a comprehensive approach to analog signal normalization for neural network-based monitoring and control of DC-DC power converters. The research addresses a fundamental challenge in edge AI applications for power electronics: the preprocessing of signals with widely varying characteristics to make them suitable for neural network analysis.

Through systematic investigation, we have analyzed the limitations of traditional digital normalization approaches, particularly their excessive area requirements compared to the total system's area and quantization effects when dealing with signals exhibiting small dynamic ranges relative to their DC levels. Two novel analog normalization architectures have been developed and characterized: a simple three-stage normalizer and an advanced HPF+LPF normalizer. Each architecture offers distinct advantages, with the simple normalizer providing a straightforward implementation for DC signal monitoring, while the advanced normalizer excels in capturing both AC and DC components independently, facilitating more comprehensive signal analysis.

The detailed system board development presented in this work demonstrates the practical implementation of these normalization concepts using discrete components to facilitate flexibility in studying various normalization techniques and the supervision of power converters with respect to aging parameters. The meticulous design includes adjustable reference generation, multi-stage amplification with configurable gain distribution, and sophisticated signal routing capabilities. The testing platform's flexibility allows for experimental validation across a wide range of operating conditions, with provisions for varying inductor values, output capacitance, ESR characteristics, and load resistances.

This research establishes a foundation for implementing edge AI as an efficient approach to creating a tiny multimeter for DC-DC power converter supervision. Such intelligent power management systems can adapt to compensate for aging effects, component tolerances, external parasitic elements, and degradation, maintaining performance over time while providing predictive maintenance capabilities.

Future work will focus on physical system verification using the developed hardware board, followed by the design of a silicon test-chip to implement the described functions. If the advanced normalizer demonstrates superior performance in experimental validation, significant size reduction can be achieved through optimized circuit design techniques when translated to an integrated circuit implementation. The current discrete implementation prioritizes flexibility and testability, but a more efficient architecture with shared resources and optimized filter topologies could substantially reduce the silicon footprint in the final design.

For the integrated circuit implementation, also Gilbert cell multiplier architectures present a particularly promising approach for realizing the analog normalization functions efficiently. These four-quadrant multipliers can be optimized in silicon to perform the required mathematical operations with significantly reduced area and power consumption compared to discrete implementations. The Gilbert cell topology aligns perfectly with the mathematical basis of the normalization process and offers superior performance characteristics when implemented in an integrated circuit context.

By leveraging the STM32 NUCLEO platform equipped on the developed board, comparative analysis between neural networks implemented in wired logic circuitry versus firmware will be possible, though integrated logic circuitry is anticipated to offer optimized area efficiency.

A particularly interesting direction for future investigation will be evaluating system robustness when parameters extend beyond their expected ranges, examining neural network performance without circuit modifications that would necessitate retraining. This exploration of operational boundaries will provide valuable insights into the generalization capabilities and practical limitations of the neural network-based monitoring system.

The analog normalization techniques developed in this thesis represent a critical enabling technology for the practical integration of machine learning capabilities into power management systems, paving the way for more intelligent, adaptive, and reliable power converters for next-generation electronic systems.

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