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Design of the driving ASIC for a PMUT matrix in ultrasound air applications

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Abstract

This thesis describes the design of the driving application specific integrated circuit (ASIC) for a piezoelectric micromachined ultrasonic transducer (PMUT) matrix used in an in-air ultrasonic rangefinder with beamforming capabilities. The research begins with an analysis of the target application and a comparison with the solutions currently available. It continues with the experimental characterization of the selected transducer, analyzing the features influencing the design of the ASIC. Based on these results, a high level description of the required ASIC architecture is derived, to meet the application requirements. It proceeds with a more detailed analysis of each functional block starting with an in-depth review of the PMUT driving stage, including the necessary surrounding circuits. Then, it continues reviewing the circuits along the signal path, going from the transducer to the digitization and memorization of the waveform.
The designed ASIC can independently drive each element within the PMUT matrix, sense the received signal, and process it. The architecture also provides significant flexibility, enabling the use of the final sensor in various applications.

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Introduction

Ultrasonic sensing is gaining popularity due to its potential in a wide range of applications. The ultrasonic approach enables the development of new sensors and enhances the capabilities of existing ones. Currently, these sensors are employed in a diverse array of fields with vastly different objectives. Their implementation ranges from automotive to medical, robotics, construction, and various consumer electronics. New approaches and functionalities continue to emerge.

The use of sound waves in sensing has been explored for a long time, with its first rudimentary implementation traced back to Leonardo da Vinci in 1490. He used a tube inserted in water to detect distant vessels by ear. Ultrasonic sensing gained significant popularity and technological advancements at the beginning of the 20th century. Implementations such as sonar and echography advanced substantially, enabling submarine navigation and exploration, as well as aiding modern medical diagnosis. Since their invention, these applications have evolved by embedding years of technological advancements and have become capable of gathering more complex information. For example, echography has achieved 3D imaging and blood flow measurements capability. These use cases exploit beamforming approach and the Doppler effect to retrieve the necessary information. However, all these implementations of ultrasonic sensing are performed in-water, whereas in-air applications have not advanced as rapidly. They remain substantially limited to simpler rangefinder sensors. This is primarily due to the significant differences between the two media through which the wave propagates. These differences profoundly affect wave propagation parameters, such as the propagation speed and the encountered attenuation, which represent the major obstacle. Despite this, the potential for employing this technology for in-air applications remains high.

Ultrasonic sensors consist of two main components: the transducer and the driving and sensing electronics. In some cases, a dedicated microprocessor or microcontroller is included if the application requires a demanding analysis of the received ultrasonic signal.

The driving electronics for simple rangefinders can be implemented using a general-purpose chip that feature a pulser and a receiver. Alternatively, the development of an application-specific integrated circuit (ASIC) may be

required to interface with specific transducers or to manage more complex and refined functionalities, such as those discussed in this document.

The ultrasonic transducer can be implemented in various ways to meet different applications and requirements. It can be implemented as discrete components, such as classic speakers or bulk piezoelectric devices, or as highly integrated components using MEMS (micro-electromechanical systems) technology. The MEMS process can use different working principles to realize micromachined ultrasonic transducers (MUTs), such as the capacitive approach (CMUTs) or the piezoelectric approach (PMUTs).

Chapter 1

Application

The designed sensor aims to cover a pool of applications with similar characteristics, which are: range finder functionality for short distances, capability to implement beam forming approach and being harmless for human interactions.
The two target applications are:

- Robotic applications: placing this sensor on robotic arms enables precise control during the final approach phase, before grabbing an object. Unlike stereoscopic cameras, this type of sensor does not require a demanding post-processing and is more energy efficient. It also allows robots to reach object outside their main camera's field of view.
- Eye tracking: utilizing the beamforming capabilities, it is possible to scan the eye surface and recognize where the pupil is pointing. With that information is not difficult to reconstruct what the person is looking at. Also, for this function the designed sensor is less computationally demanding and more efficient, than processing the feed of a camera.

There are various methods and technologies to implement a distance meter, such as: electromagnetic(radar), ultrasonic and optical (as LIDAR and stereoscopic cameras), with LIDAR and ultrasonic technologies being more widely adopted for consumer applications. Each method has its strengths and weaknesses that determine the use case for which it is best suited [1] [2].

Both those methods work with a Time-Of-Flight (TOF) approach. It consists in emitting a pulse wave (sonic or light) and measuring the time that elapses before receiving the signal back after it bounces off the target object. With this time information, the distance of the target can be easily retrieved as:

$$D = \frac{c \cdot t}{2} \tag{1.1}$$

Where: D is the distance of the target, c is the speed of the wave in the medium and t is the elapsed time.

Comparing the two main technologies, the measurable range difference is immediately noticeable. LIDAR experiences minimal attenuation when propagating through air and, therefore, is capable of achieving a very long range. However, it struggles with lengths shorter than a few centimeters. This is due to the TOF approach of this sensor topology. Combined with the extremely high speed, of light, this results in a very short operation time available for the sensing circuit.

In contrast, ultrasonic sensors face the opposite challenge. Although they also use the TOF approach, they are able to measure very short distances because they rely on a sound wave, which propagates at a much lower speed. This slower propagation relaxes the timing requirements of the sensing circuit. However, they encounter difficulties with long distances due to the dispersion and attenuation of the sound wave. This reduces the power of the reflected wave, making it difficult to sense the echo signal as the object distance increases.

Between these two technologies, the ultrasound approach better suits the target application, mainly due to the short distances targeted and the beamforming capabilities.

Beamforming enhances the sensor's capabilities by electronically steering the angle at which it focuses the ultrasonic wave. It allows to obtaining measurements from different directions without the need to mechanically rearrange the sensor. This enables scanning the surface of an object and reconstructing its shape, retrieving much more information than just its distance. To utilize beamforming, an array of transducers is required, with the elements spaced no more than $\lambda/2$ (where λ represents the wavelength) to avoid the excitation of side lobes. The larger the array, and therefore the greater the number of elements it contains, the finer the achievable control over the output beam. This means that the transducer must incorporate a matrix of independent elements, and the driving ASIC must be capable of individually drive each element. It must provide each element with the driving waveform at the correct phase to steer the beam toward the selected direction.

Another feature of the final sensor is its small size, which facilitates its integration into various systems. To achieve this, the optimal solution is to implement a system-in-package approach with stacked dice, where the transducer is attached on top of the control ASIC. As shown in Fig.1.1. The final structure is then placed inside a single package, as illustrated in Fig.1.2.

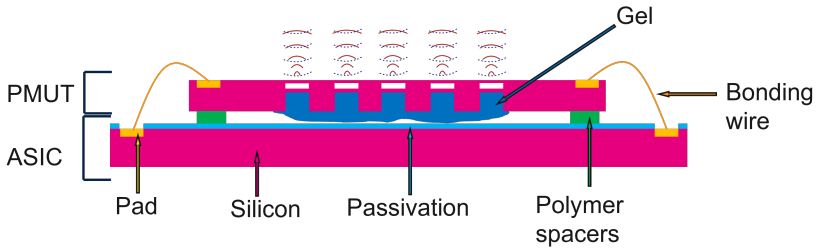


Figure 1.1: Dice stack cross section.

This means that the dimensions of the transducer must be compact, which limits the number of possible elements. This restriction is critical for selecting the appropriate technology of the transducer. It excludes all discrete and bulk actuators, highlighting MEMS e as the best solution. It enables the manufacturing of the matrix of elements while maintaining compact dimensions and offering high versatility in terms of the size and shape of the array. Additionally, this process is highly cost-effective compared to other alternatives. Several processes have already been developed to enable the attachment of the ASIC die to the transducer die, and packages capable of hosting this stack are already available.

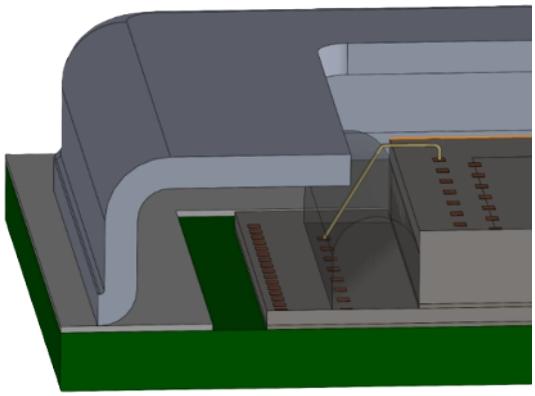


Figure 1.2: 3D render of the final package.

1.1 ASIC architecture

The required architecture has been determined, based on the application requirements described earlier, the PMUT characterization results presented in Chapter 2 and the ASIC requested functionalities. The final ASIC must be capable of individually driving each transducer membrane with the appropriate timing to perform the beamforming of the emitted sound wave.

After transmitting the wave, it must switch to the reception phase, amplify the signal from the transducer elements, digitize it using an ADC, and store it in the RAM present on-chip, waiting to transmit these data out the connected microcontroller.

The top-level block diagram of the ASIC is illustrated in the Fig.1.3. It includes 25 channels, each interfacing with a membrane in the 5×5 matrix of the transducer.

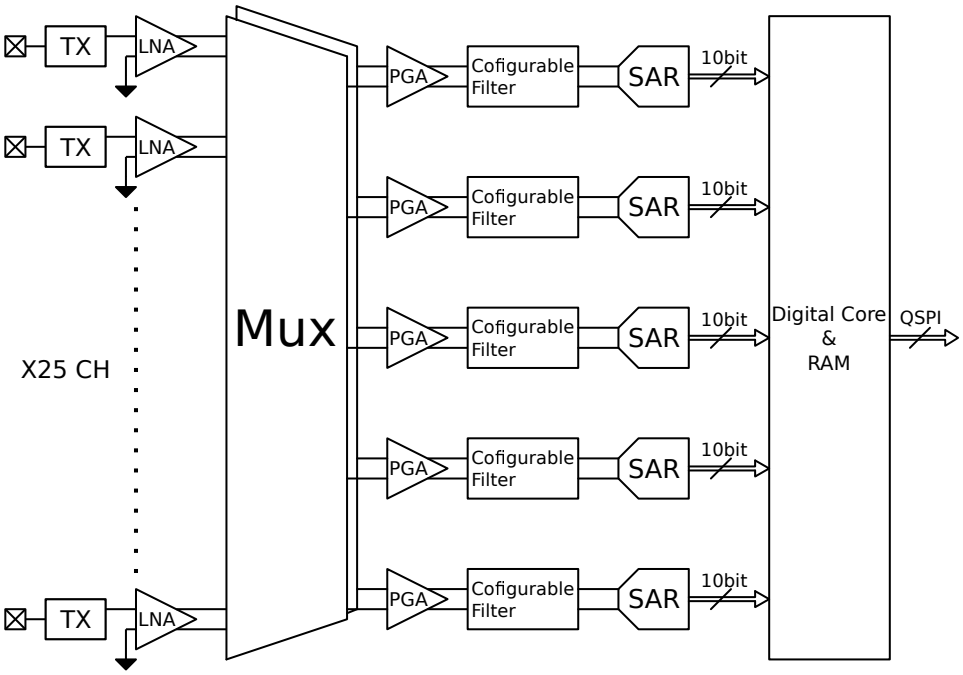


Figure 1.3: Top level block diagram of the ASIC's architecture.

The TX blocks shown in Fig.1.4, are composed by a pulser to drive the PMUT, a resistor bank to attenuate the ringing and incorporate the T/R switch (Transmit / Receive). This element is able to drive the membrane with pulses of $20V_{pp}$ and rising and falling edges faster then 25 ns.

Following this, a low-noise amplifier (LNA) is connected, to position it as close as possible to the pad where the membrane, it senses, is bonded. This placement aims to amplify the input signal before any routing or manipulation to achieve optimal signal to noise ratio (SNR) performance. The amplifier has a programmable gain ranging from 14 dB to 36 dB and incorporates the time-gain compensation (TGC). The LNA takes the single-ended input from the PMUT and outputs an amplified differential version of the signal. From this point, the entire signal path is differential.

The outputs of the LNAs are connected to the two multiplexers: one for the positive differential signal and one for the negative differential signal.

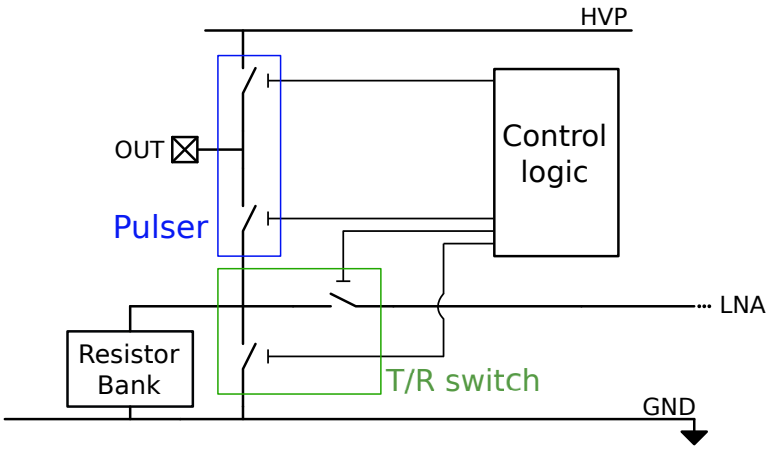


Figure 1.4: Block diagram of the TX circuit.

The multiplexers provide flexibility to route the PMUT elements to the five receiving channels, allowing the grouping of the matrix's membranes in different sectors.

Each of the five receiving channels is a chain composed by: a programmable gain amplifier (PGA), a programmable filter, and an Analog to digital converter (ADC) with 10 bits of precision. Afterward, the digitized signals enter the digital core of the ASIC and are stored in the 900 KB of RAM present on-chip, ready to be processed and transmitted through the QSPI to the microcontroller it interfaces with.

1.2 Operation phases

To determine the architecture of each unit and especially of the TX block, it is important to define the operational phases required by the circuits to perform their functions. The ASIC must provide the driving waveform to the PMUT to emit the sonic wave. After which must attenuate the residual ringing before proceeding with the reception. The received signal must then be amplified by an amount proportional to its original amplitude. Finally, it is digitized and stored in the RAM.

From these functional requirements we can extract the operation phases of the circuit.

1. Transmission: The ASIC must provide the driving pattern to the transducer.

2. Ringing Dampening: The circuit has to attenuate the residual vibration on the membrane.

3. Reception: The ASIC must sense the signal coming from the membrane amplify and store it.

4. Idle: Between consecutive measurements, there is an idle time whose length depends on the selected update interval.

In the different phases, each block must perform specific tasks. We can divide the elements into two groups based on their active phases: one is the RX chain, from the LNAs to the ADCs, and the other is the TX block.

- RX chain: They must operate during phase 3, while for the rest of the time they can remain idle or perform secondary tasks.

- TX block: In phase 1 it must drive the PMUT with the driving waveform, in phase 2 it must dampen the residual ringing on the membrane, in phase 3 it must connect the pad where its membrane is bonded, to the LNA and in phase 4 it must clamp the PMUT to ground, to avoid spurious excitations.

1.3 Layout

The complete complete ASIC is shown in Fig.1.5. The various elements are arranged with consideration for the final package dimensions. The TX blocks are positioned half on the top and half on the bottom of the integrated circuit. This arrangement ensures that each driving element is located close to the pad where the membrane it drives is bonded, thereby minimizing the routing length between them. For the same reason, the relative LNA is positioned adjacent to this element.

The five reception chains, including the two multiplexers, are located in the right half of the central section. The digital core and the RAM are located in the left half of the central space. Surrounding these elements are the supplementary functional blocks required to ensure the operation of the ASIC, such as the bandgap circuit, the power-on reset, and level shifters for translating the control signals from the 1.2 V domain used by the digital core to the 3 V and 5 V domains used by the analog elements.
All around the integrated circuit there is the pad ring, which include the ESD protections and the input/output buffers. The remaining pins, apart from those connected to the transducer, are used for power supplies, digital communication, and debugging.

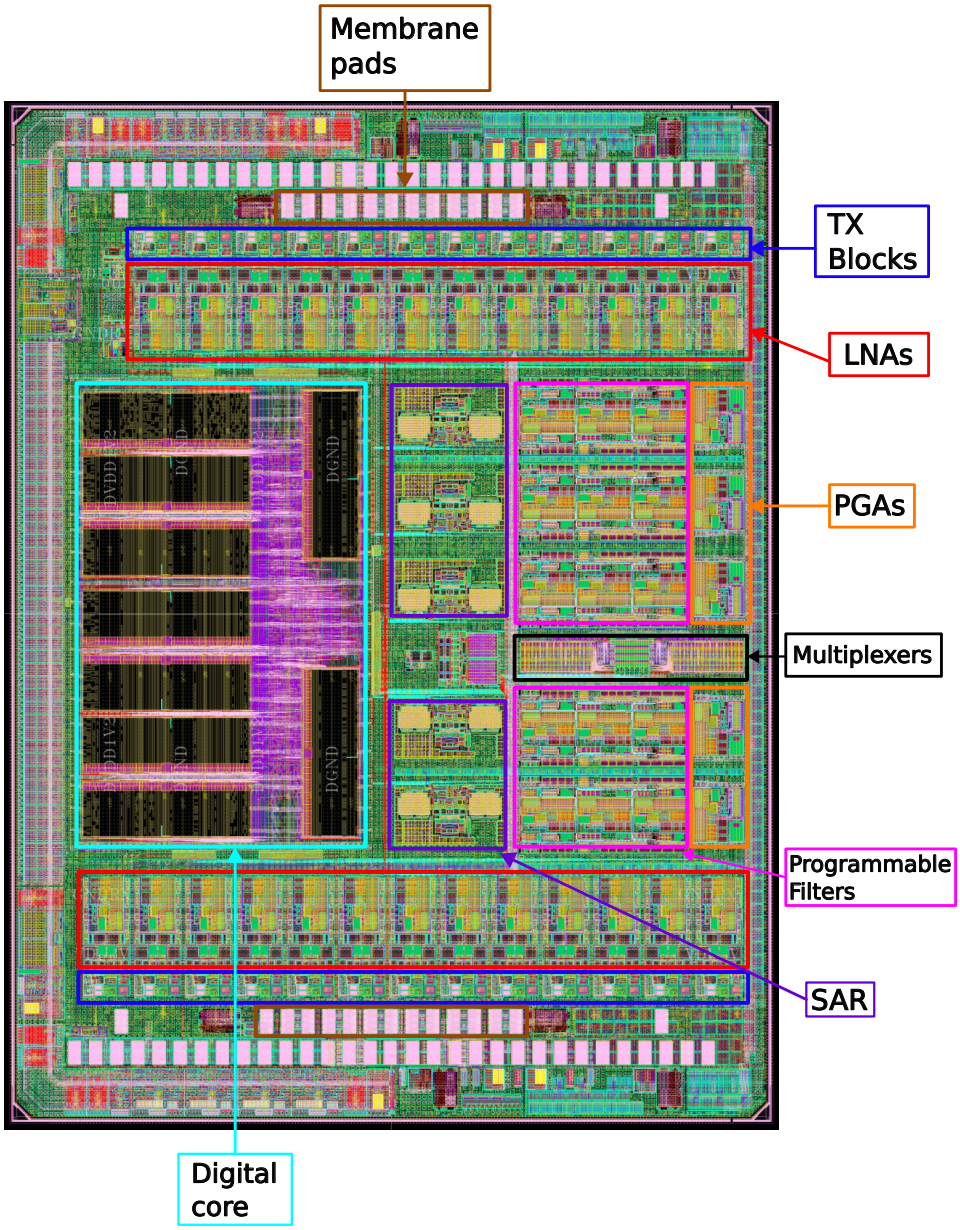


Figure 1.5: Complete layout of the ASIC, with all the main blocks highlighted.

Chapter 2

Transducer

2.1 PMUT overview

The selected transducer is a PMUT (piezoelectric micro-machined ultrasonic transducer), which is a membrane created with a piezoelectric layer, enclosed between two electrodes contacting both of its faces. It is manufactured on the structure, shown in Fig.2.1, which allows it to oscillate freely.

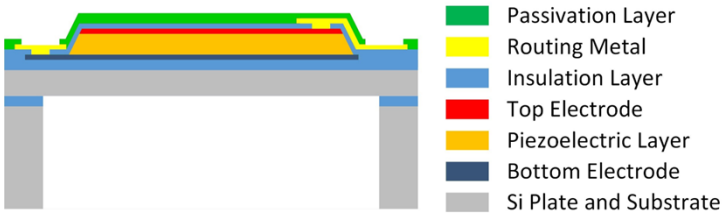


Figure 2.1: Schematic cross section of a PMUT cell, showing the details of the material stack and the cavity.

PMUTs have received significant attention due to their various advantages such as low manufacturing costs, high design flexibility and reproducibility. They offer high versatility, enabled by the wide range of available materials and various processes for their manufacturing. The geometrical shape, the materials and the processes used to realize these membranes determine the final electromechanical characteristics of the PMUTs [3], making them suitable for a large spectrum of applications.

The working principle is based on applying an electric field between the top and bottom electrodes, that creates a transverse stress inside the piezoelectric layer and so a bending moment, which result in the deflection of the structure. Once the electric field is released, the membrane starts oscillating before settling back to the neutral position. The oscillation can be enhanced by applying a waveform in phase with the natural vibration of

the membrane to the electrodes.

The oscillation frequency of the PMUT strictly depends on the geometric shape of the suspended element. Therefore, each transducer can be manufactured to target the desired frequency.

In particular the selected transducer is a PMUT matrix composed by an array of 5×5 membranes, as illustrated in Fig.2.2. The piezoelectric material used to create the active layer is PZT (lead zirconium titanate). The shape and size of the suspended element are designed to achieve a resonance frequency of 600 kHz.

This frequency has been chosen as compromise, between the in-air attenuation of the sonic wave, which increases at higher frequencies, and the longitudinal achievable resolution, which decreases at lower frequencies, since the resolution is strictly bound with the wavelength of the transmitted signal.

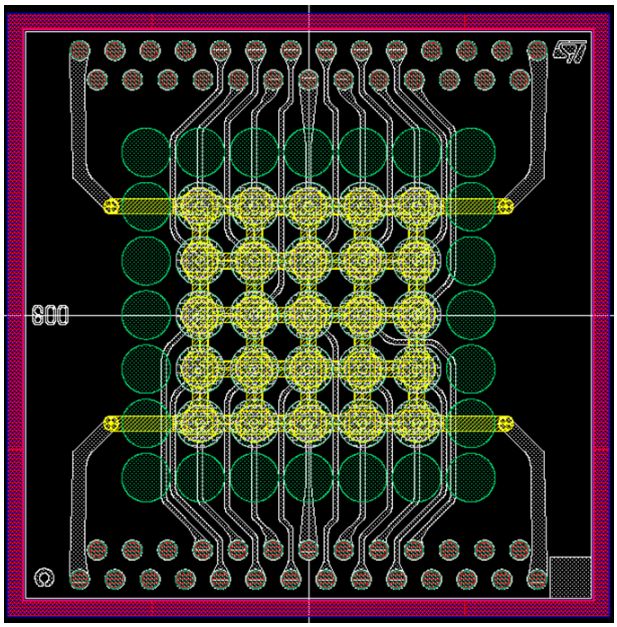


Figure 2.2: Top view of the PMUT die, it shows the 5×5 membranes and the routing between the pads and each element.

The electrical model of each membrane is illustrated in Fig.2.3. The electrical schematic consists of a series resonator in parallel with a capacitance. The capacitor C_0 models the capacitive behavior of the sandwich structure, composed by the piezoelectric layer with the contacts on the top and bottom. It has a value of 120 fF and is responsible for the emission of the sonic wave.
The series resonator, composed of R_s = 1010.8 Ω, C_s = 2.12 pF, and L_s = 33.65 mH, accounts for the intrinsic oscillation of the membrane.

The equivalent circuit and the component values were obtained by fitting the measured impedance-over-frequency curve of the transducer. A statistical measurement of this curve was performed to derive the quality factor of the elements. This factor is defined as $Q = \frac{f_{res}}{\Delta f}$, where f_{res} is the resonance frequency and Δf is the resonance width, obtained as the bandwidth over which the power of vibration exceeds half the power at the resonant frequency. This measurement indicate that the quality factor is equal to Q=123.78. The R_s for the resonator has been calculated, to model the measured Q factor as follow:

$$R_s = \frac{1}{\omega \cdot C_s \cdot Q} = 1010.8\Omega \qquad \omega = 2\pi f_{res} \tag{2.1}$$

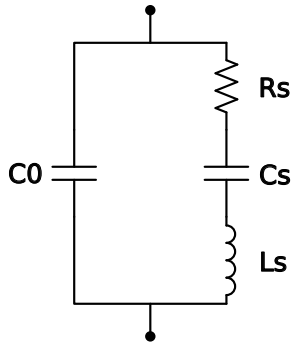


Figure 2.3: PMUT equivalent electric model.

2.2 PMUT characterization

To properly drive the selected transducer it is important to address its characteristics. It requires a positive polarization to achieve optimal performance in both transmission and reception. Additionally, it has a very high Q factor, which results in very low internal losses. This implies that the membrane keeps oscillating for a long time after the driving excitation. I will refer to this phenomenon as "ringing" in this document; a representation of this residual vibration evolution is depicted in Fig.2.4. The ringing can limit the accuracy of the final sensor if not properly managed. This residual vibration of the membrane adds to the received wave. If not attenuated, it can be several times larger than the incoming signal, obscuring it and significantly increasing the complexity required for its detection. This issue is particu-

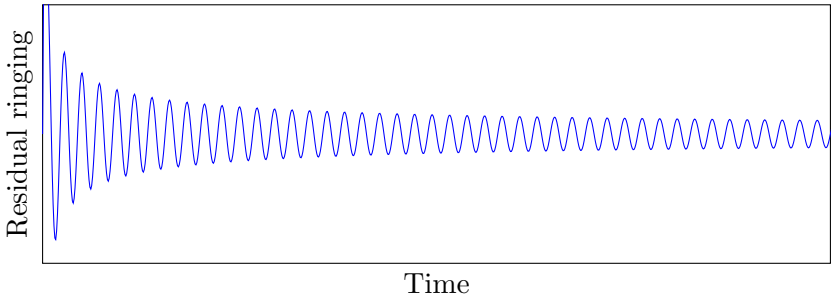


Figure 2.4: Representation of the residual ringing, on the transmitting membrane after the end of the driving excitation.

larly significant for short distances (up to approximately 2 cm) because the vibration does not have sufficient time to attenuate. However, it also persists over longer distances, since also the received signal is further attenuated due to the extended path.

Some analyses were preformed in laboratory to evaluate the transducer under all operating conditions, the test setup is shown in Fig.2.5. To simulate the work environment while isolating the various effects, the tests were conducted using two PMUTs: one for transmission and one for reception. This setup aimed to replicate the entire sensor operation, from the transmission of the wave to the reception of the signal, while isolating potential side effects that may arise, due to the powerful driving waveform (compared to the received signal) which could obscure proprieties of the received signal. The receiving PMUT was connected to an oscilloscope while the

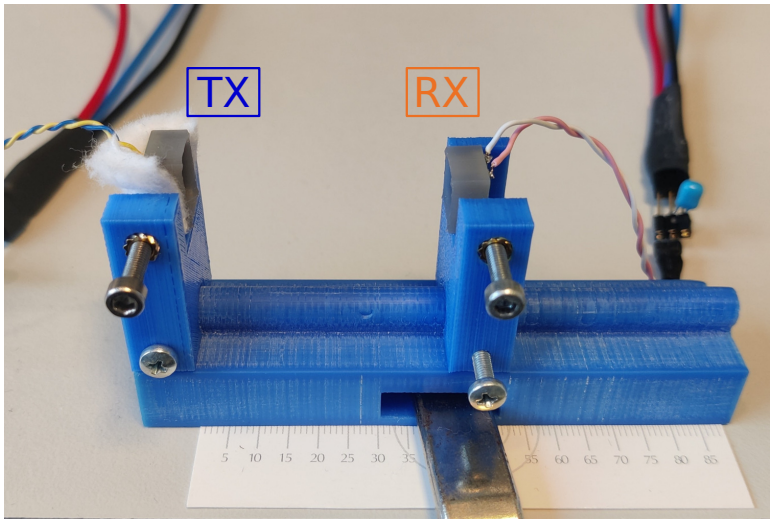


Figure 2.5: PMUT laboratory setup.

transmitting one was attached to a pulser capable of driving the transducer with a programmable square waveform in amplitude, period, duty cycle and number of pulses. The main parameters analyzed are the transmitted and received power, as well as the ringing trend. Multiple analyses were performed to assess the impact of various driving methods, which are detailed in the subsequent sections

2.2.1 Driving amplitude

To study how the driving waveform amplitude influences transmission, a test is conducted by placing the transmitting and receiving PMUTs facing each other at a fixed distance of 4cm. Then the transmitting membrane is driven with a pattern of three square pulses, with a period of 1.66μs, which is equal to the membrane resonance. For each iteration, the pattern's amplitude is increased, starting at 5 V and reaching up to 20 V. For every pattern, the received signal amplitude by the second PMUT is measured, as well as the residual ringing on the TX membrane.

The graph Fig.2.6 shows that the received amplitude increases monotonically with the driving amplitude, with a decrease in the slope around 10 V, meaning there is an improvement to increase the driving voltage.

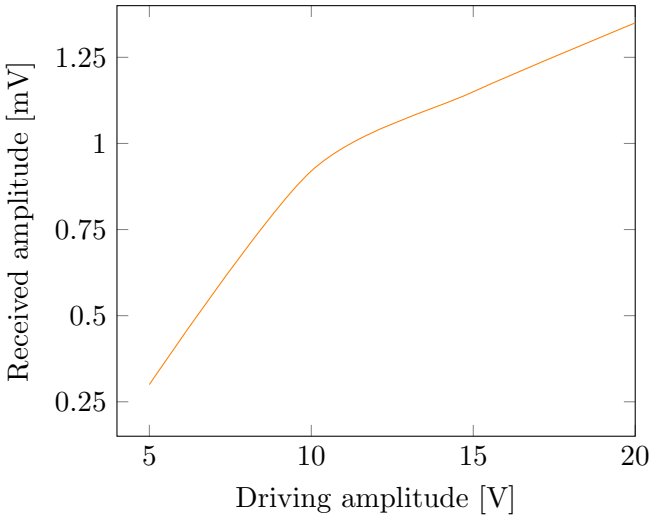


Figure 2.6: Received signal amplitude as function of the driving pulses amplitude.

However, it is equally important to control the trend of the residual ringing, which as been measured at a fixed time (80 μs) after the excitation stops. As can be observed in the graph Fig.2.7, it shows a progression similar to the transmitted signal amplitude.

This indicates that increasing the driving voltage similarly influence both

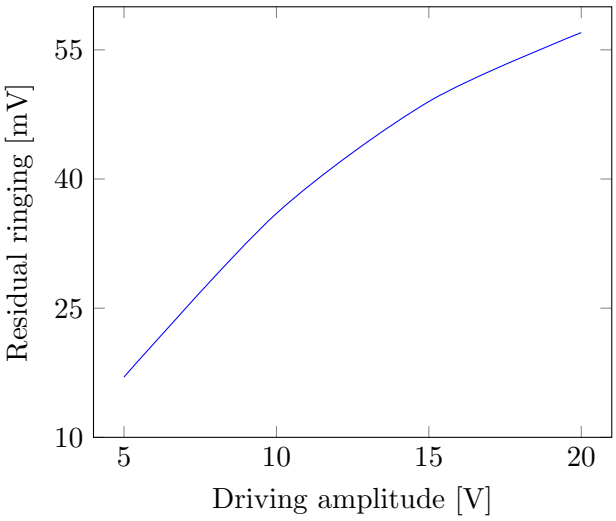


Figure 2.7: Residual ringing on the transmitting membrane as function of the the driving amplitude.

the output signal and the residual ringing. Therefore, increasing the amplitude does not provide advantages in controlling ringing, but also does not introduce disadvantages, since the ratio between the output signal power and the residual ringing remain practically unchanged. So the driving voltage can be increased to maximize the output signal power.

2.2.2 Number of driving pulses

As mentioned earlier, an increase in the output signal intensity is expected if the transducer is driven using a long waveform, that is in phase with the natural oscillation of the membrane. This test aims to study how the length of the driving waveform affects the output signal, also for this analysis the two PMUTs are placed facing each other and at fixed distance of 4cm. The pattern used for this test consist in a train of square pulses, with a fixed amplitude of 10V, and a period of 1.66μs (the same as the membrane natural vibration). The duty cycle is 50%, so a pulse remains high for 830ns and low for 830ns. For every iteration of the test, the number of pulses in the pattern is increased by one, starting from one pulse and reaching 10 pulses. At each iteration, the received amplitude, by the second PMUT is measured.

In graph Fig.2.8, the orange line represents the measured data, while the grey line illustrates an ideal reconstruction of the interpreted trend. The difference between the reconstructed curve and the measured one can be explained by an error between the driving waveform period and the PMUT intrinsic oscillation period. This error accumulates, creating a phase shift between the membrane's vibration and the driving waveform. Consequently,

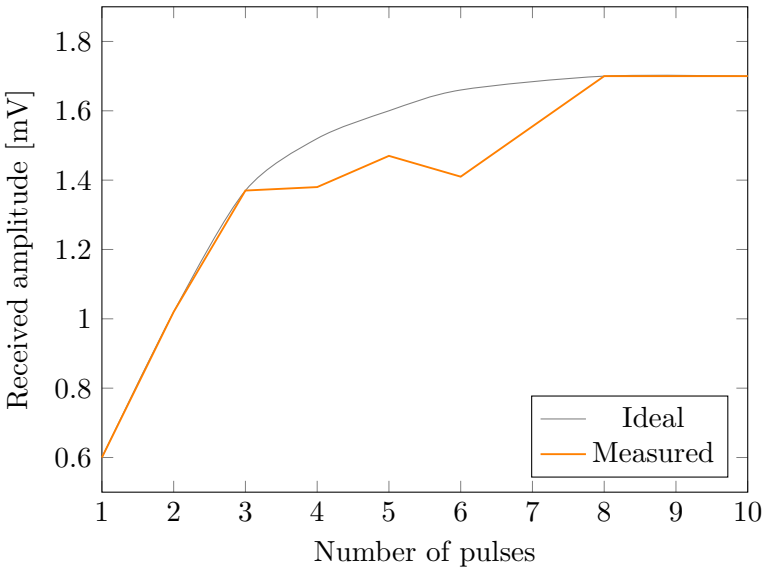


Figure 2.8: Received signal amplitude as function the number of driving pulses.

the new pulses do not sum perfectly in phase with the accumulated oscillation, reducing their effects. By increasing the number of pulses further, the new ones can sum in opposite phase, reducing the present vibration. By continuing to extend the pattern even more, the phase error can reach 2π, causing the new pulses to sum in phase again.

This effect can be modeled as a sum of sinusoids. Each new sinusoid has the same frequency of the membrane natural vibration and start when the next pulse occurs. Therefore, it is spaced with frequency of electronic stimulus that can be considered delayed in phase of $2\pi+\epsilon$ (where ϵ represent the alignment among the two frequencies). Over time the present vibration in the PMUT attenuates, reducing the contribution of older sinusoids to the present membrane oscillation.

$$\sum_{i=0}^{N_{pulses}-1} H_{(t-i\tau)} \sin(\omega t + i\tau_{err}) e^{-\alpha \frac{t-i(\tau-\tau_{err})}{\tau}} = \tag{2.2}$$

$$= \sin(\omega t) + H_{(t-\tau)} \sin(\omega t + \tau_e rr) e^{-\alpha \frac{t-(\tau-\tau_{err})}{\tau}} + \dots$$

Where τ is the oscillation period, τ_{err} is the phase shift error, $e^{-\alpha \frac{t-i(\tau-\tau_{err})}{\tau}}$ is the exponential term that account for the vibration attenuation, H(x) is the Heaviside step function:

$$H_{(x)} = \begin{cases} 0, & x < 0 \\ 1, & x \geq 0 \end{cases} \tag{2.3}$$

to account for the sinusoids being added at different times, by the driving pulses.

A graphical visualization of this model is shown in Fig.2.9. Observing this phenomenon in the time domain it appears as a notch in the received signal. A representation of the output signal generated by a pattern of 9 pulses is depicted in Fig.2.10. it shows an increase of the received amplitude up to the third driving pulse. Then, the accumulated phase error causes the new pulses to reduce the existing oscillation, until the seventh pulse which starts increasing the membrane vibration again. By the ninth and final pulse, the internal vibration within the PMUT (ringing) evolves autonomously, gradually damping.

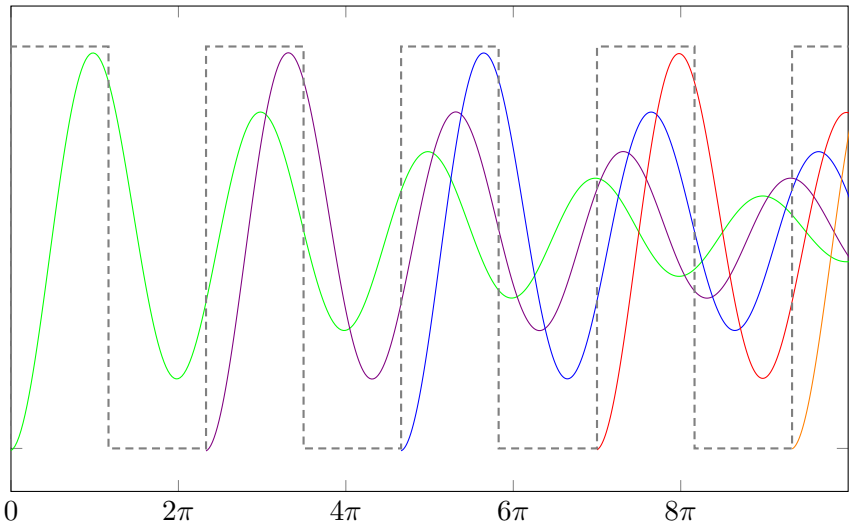


Figure 2.9: Graphical visualization of the sum of sinusoids model, described by the equation 2.2. The dashed line represents the driving pulses, that excite the sinusoids. The x-axis is relative to the first sinusoid.

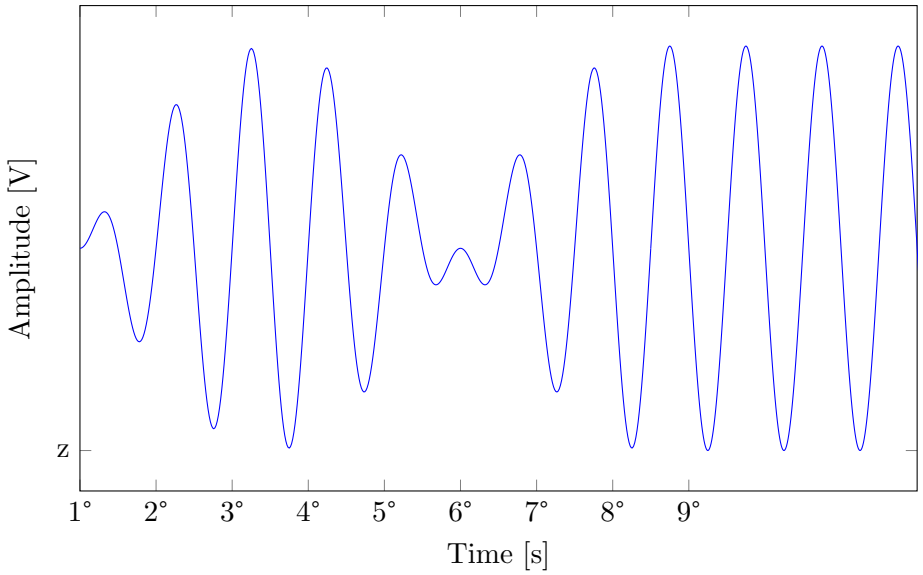


Figure 2.10: Output signal in the time domain, generated by a driving pattern of 9 pulses. The x-axis marks the instants when a new driving pulse occurs.

These results indicate that it is mandatory to keep the driving waveform precisely in phase with the natural oscillation of the membrane. Otherwise, the output power does not increase as expected from the longer driving pattern. Even worse, if the phase shift is significant, the output power may decrease. However, maintaining the driving pulses aligned with the natural vibration of the PMUT is challenging due to the variability introduced by the manufacturing process of membranes.

In each case, observing the tests results and the ideal reconstruction, depicted in Fig.2.8. It shows a rapid increase in the output power for the first part of the curve (up to three or four pulses), after which the contribution of each new pulse becomes progressively less significant, because the oscillation's amplitude reaches its saturation.

2.2.3 Pre-polarization

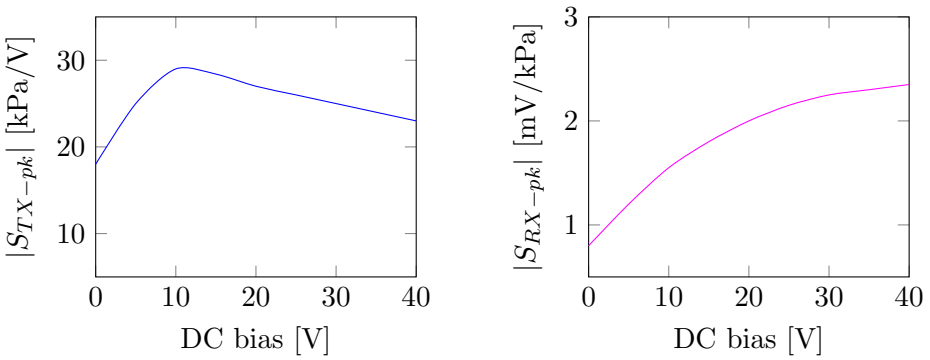
The selected PMUT transducer utilizes PZT as the piezoelectric layer. This material has an intrinsic ferroelectric nature, which makes it susceptible to external factors such as DC bias voltage [3]. The polarization voltage applied to the PMUT influences both the transmission sensitivity (from driving voltage to sound pressure) shown in Fig.2.11(a) and the reception sensitivity (from sound pressure to input voltage) shown in Fig.2.11(b). However, since the final sensor utilizes a TOF approach, the parameter of interest is the two-way sensitivity, obtained as the product of the two transfer functions. As shown in the graph Fig.2.11(c), the two-way transfer function exhibits a rapid increase in value, up to 20V of DC bias, after which its increase became marginal.

This analysis highlights the importance of applying a polarization DC voltage to the transducer. Due to the PMUT characteristics, the polarization voltage cannot be applied in reverse. The higher potential must be applied to the positive terminal and the lower potential must be applied to the negative terminal.

In the selected transducer, all the membranes composing the 5×5 matrix, share the same negative contact and have only the positive terminal independent from each other. This implies that if the membrane gets pre-polarized between ground and a positive voltage, the driving waveform must be applied around this new bias potential. This condition increases the requirements for the driving ASIC, therefore has been decided to polarize the membranes by applying a negative voltage, provided externally, to the common terminal and connecting the positive one to the ASIC, as illustrated in the scheme Fig.2.12. In this way the requirements for the ASIC can be relaxed.

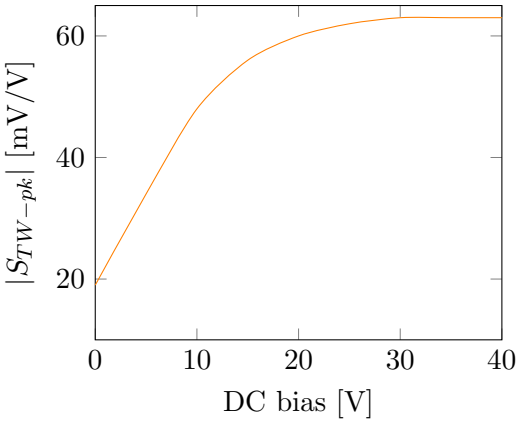
For reliability purposes, the PMUT must not sustain a voltage difference greater than 40 V across its terminals. Since the two-way sensitivity shows saturation beyond 20 V of bias, it has been decided to polarize the negative

terminal at -20 V to maintain a 20 V margin for the amplitude of the driving waveform.



(a) TX peak sensitivity

(b) RX peak sensitivity



(c) Two-Way peak sensitivity

Figure 2.11: TX, RX and Two-way peak sensitivities with respect to the applied DC bias.

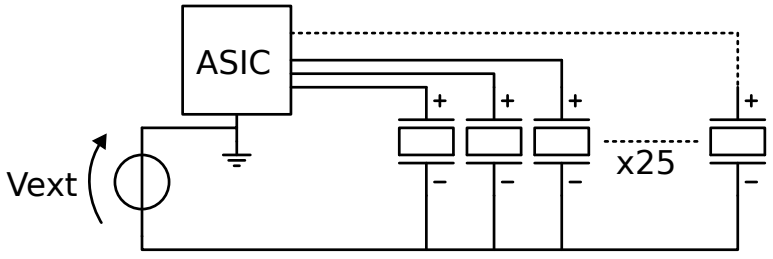


Figure 2.12: PMUT polarization scheme.

2.3 Driving approach

It was necessary to decide the shape of the driving waveform. In the literature there are several possible approaches, each one aimed to enhance an aspect of the signal, like: multi-level driving to better approximate a sinusoid and reduce harmonic generation, utilize long driving patterns to narrow the output spectrum, or continuous wave driving (CW) to exploit the Doppler effect and many more [4]. Therefore, it is important to determine what is essential for the target application and what is not, to define the waveform that best suits these requirements.

The final core application is a rangefinder sensor. This implies that a high longitudinal accuracy is required, as well as keeping the design as simple as possible. While harmonic generation and the output spectrum are not significant concerns.

According to these constraints a square waveform has been selected. The square waveform excites a high number of harmonics; however, due to the extremely narrow band of the PMUT, it acts as a band-pass filter, significantly attenuating this issue. And since avoiding harmonic excitation is not one of the primary requirements, the square waveform has been chosen to simplify the driving circuit design.

As mentioned, one requirement is to obtain a high longitudinal accuracy, which imply to use a short driving pattern in the time domain. But to increase the output signal power it is useful to drive the PMUT with some pulses that are in phase with its natural oscillations. Accordingly to the analysis performed the best compromise between those requirements is to use 3 pulses and enhance the output power by increasing the amplitude of the driving pulses. Therefore the ASIC has been designed to handle up to 20 V of driving amplitude. This solution provides flexibility to better fit the desired application.

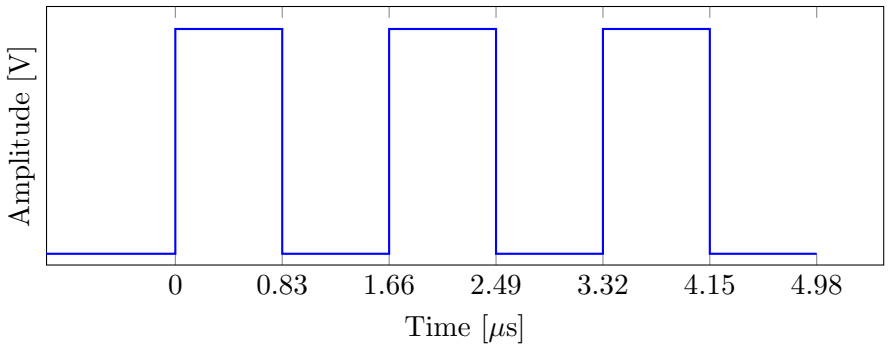


Figure 2.13: Driving waveform applied to the membrane.

The final driving pattern is represented in the plot Fig.2.13, before the driving, the membrane is in clamp state, connected to ground to avoid spu-

rious excitations. Then at $t = 0$ the driving start, applying the 3 square pulses to the PMUT, after those the ASIC enter in the next phase, the "Ringing dampening". The driving pattern ends by forcing the transducer to ground. Consequently, the ringing oscillations and the reception of the echo signal occur around 0 V.

2.4 Ringing dampening

As mentioned in section 2.2, the ringing is a significant limitation that increases the difficulty of detecting the echo coming back from the target object. The ideal goal is to eliminate the ringing quickly to enter the reception phase immediately after the transmission of the sound wave. This allows the sensor to measure distances very close to it.

The main challenge is to attenuate the ringing without re-exciting the vibration of the membrane. To achieve this objective, two methods have been devised, one active and one passive. The first involves driving the membrane with a waveform in counter phase to the existing vibration. The second method connects the transducer to a resistor to maximize power dissipation from the internal oscillation.

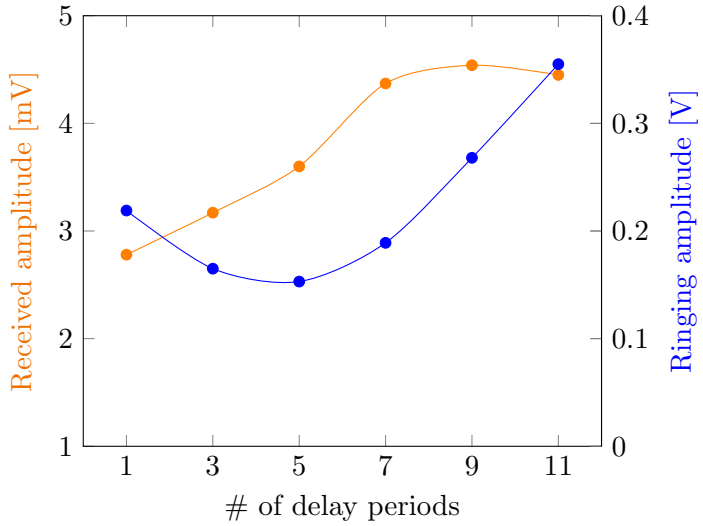
The active method is more efficient but struggles to dampen low values of ringing, as it risks re-exciting the transducer. The passive method, on the other hand, requires more time to achieve the same reduction in residual vibration but does not risk re-exciting the transducer. Therefore, the best approach is a combination of the two methods: starting with the active approach and then switching to the passive solution.

2.4.1 Active damping

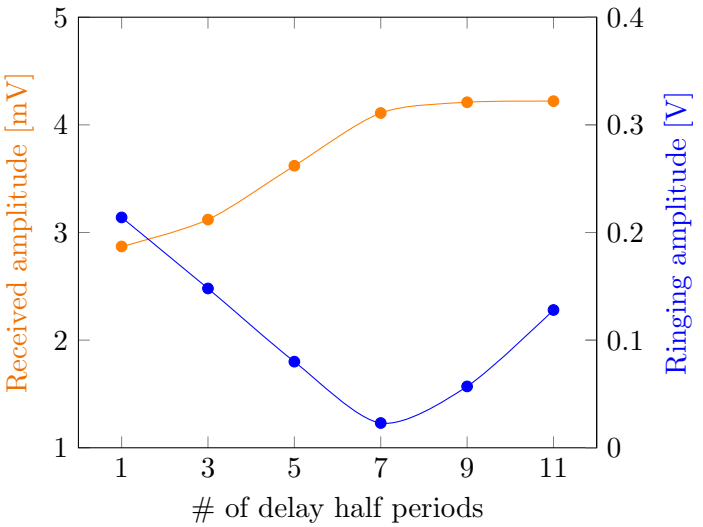
This approach consists of driving the membrane again after the transmission phase, but with a waveform in anti-phase to the residual ringing. This method is very effective, however presents the risk of re-exciting the membrane vibration. This can occur if the damping pulses are not perfectly out of phase with the ringing. In such cases, a component of the pattern does not cancel out the existing vibration but instead adds to it. Additionally, if the pattern is too long, it may stop the vibration and then restart it. Moreover, the damping pattern cannot be applied to the membrane immediately after the end of the transmission pattern. This is because the oscillations with the largest amplitude in the membrane occur right after the end of the transmission pattern, where the energy provided by the impulses accumulates. It is therefore necessary to wait for a few cycles to allow the membrane to emit before initiating the damping process.

To identify the optimal approach, a test was conducted using the previous setup, with the pair of PMUTs facing each other. The analysis consisted in exciting the membrane with three driving pulses, waiting for a variable

time, and then applying the counter pulses. The test was performed twice: the first time using three counter pulses, and the second time using two counter pulses. During the analysis, the amplitude received by the second PMUT and the residual ringing amplitude at the end of the damping pattern were measured.



(a) Active damping with 3 counter pulses



(b) Active damping with 2 counter pulses

Figure 2.14: Received amplitude and residual ringing over the number of half periods as delay.

The results are shown in Fig.2.14. The two plots represent the ringing

and the received signal, over the waiting time. The delay is expressed in number of half oscillation periods that elapse after the end of the driving pulses. Consequently, an odd number of delay periods causes the new pulses to be out of phase with the residual oscillation, while an even number aligns the new pulses in phase with the existing ringing (For this reason, an even number of delays has not been tested.).

The graph shows that it is necessary to wait at least seven periods to avoid attenuating the emitted wave, while waiting longer provides no additional benefit. While comparing the two tests, the one using only 2 counter pulses, shows a grater ringing attenuation, mainly because it doesn't re-excite the membrane vibration.
This approach inherently presents a limiting factor: it can attenuate the membrane's vibration only in discrete steps. Once the residual oscillation falls below a certain threshold, this method cannot further reduce the vibration. This limitation arises because the use of an additional counter-impulse would re-excite the membrane.

2.4.2 Passive damping

This approach involves connecting passive components to the membrane, to maximize the power dissipated during each oscillation cycle. This method is clearly less effective than active damping; however, being a passive approach, it has the significant advantage of not re-exciting the membrane under any conditions.

As shown in Fig.2.2, the transducer equivalent electric model, is a series oscillator with a capacitor in parallel. The optimal way to maximize energy extraction from the resonator is to connect a load with an impedance value that is the complex conjugate of the membrane's impedance. Since the membrane impedance is dominated by the parallel capacitor, the conjugate load should include an inductor as the reactive element. However, the technology used does not include integrated inductors, and since the transducer consists of 25 membranes, using an external inductor for each element becomes too expensive.

The method employed consists in using only a resistor as the load. This approach ensures that the current of the series resonator splits between the capacitor and the resistor. The portion of the current flowing through the resistor is dissipated, thereby attenuating the oscillation. To maximize the power dissipated, the optimum is to apply a resistor with a value equal to the impedance of the parallel capacitor C_0 at the resonance frequency. This configuration divides the current equally between the two components, achieving the highest power dissipation on the external resistor. The capacitor impedance at the resonance frequency, of 600KHz, is $C_0 = -j2.287E^3\Omega$, therefore the ideal resistor value is $R = 2.287K\Omega$

This approach has been tested by exciting the membrane with three pulses, then connecting the resistor to the PMUT. The resistor remains connected to the transducer for 20 μs. At the end of this period, the resistor is disconnected, and the residual oscillation is measured 50 μs after the start of the pattern. Several measurements have been taken with different resistor values; the results are shown in Fig.2.15.

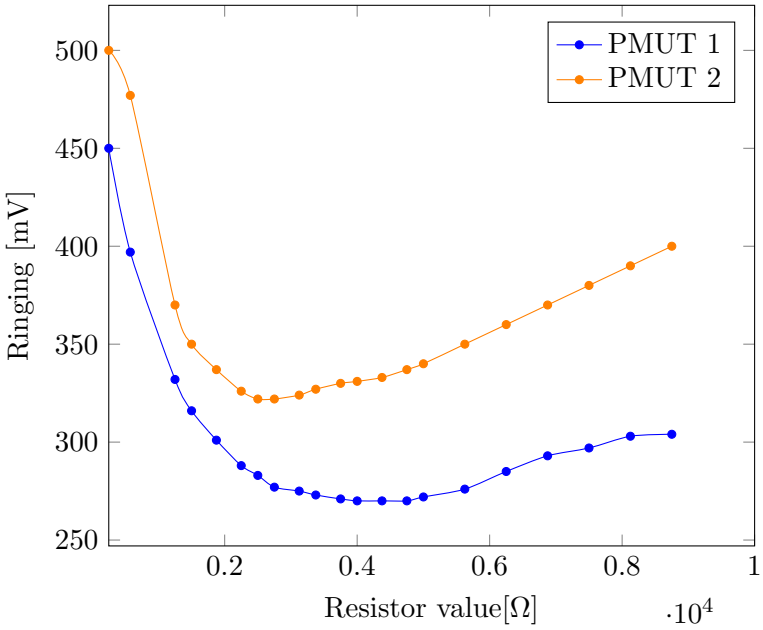


Figure 2.15: Residual ringing after 50μs from the excitation, over the damping resistor value. The two curves are the results for two different PMUTs.

Analyzing the results, both PMUTs exhibit a minimum in the residual oscillation in function of the applied resistance. However, the two trends differ significantly: the first shows the minimum for resistance values around 4 KΩ, while the second exhibits the minimum values around 2 KΩ. This is due to the spread in the production of the transducers. Consequently, to maximize the effectiveness of this method, the ASIC must be able to provide a resistor with the appropriate value for the connected transducer.

Chapter 3

TX in depth analysis

The transmission block requires several subsystems to perform its functions. A detailed view of all the required blocks is shown in Fig.3.1.

As mentioned in section 2.3, this circuit must provide a driving waveform with amplitude up to 20V to the PMUT. Therefore, the ASIC requires a high-voltage rail, externally supplied with the desired pattern voltage. The TX blocks are the only circuits that handle the high-voltage, while the rest of the ASIC operates within the low-voltage domain.

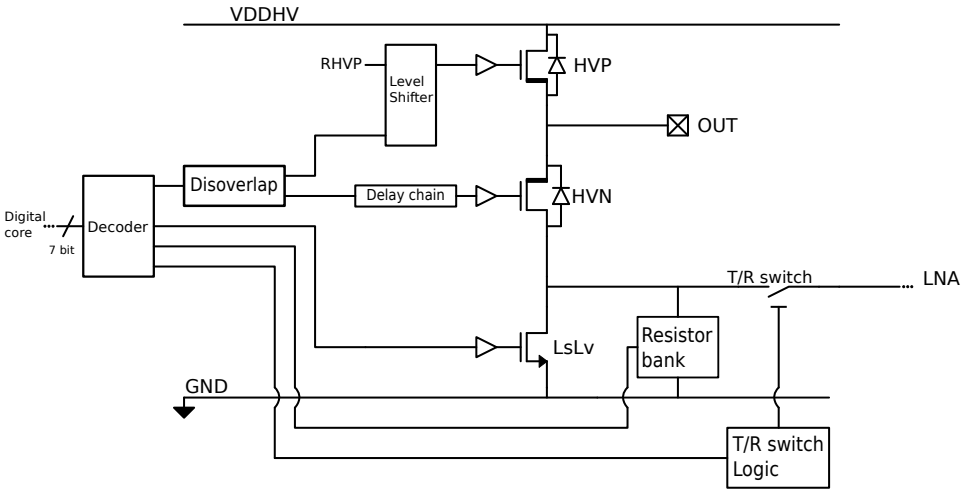


Figure 3.1: More detailed view of the TX block.

To provide the digital control signal required to drive the high-side transistor of the pulser, a level shifter is necessary to translate this signal from the low-voltage domain, where it is generated, to the high-voltage domain, where the transistor operates. Due to the delay in the signal propagation caused by this element, a delay chain must be inserted on the low side path, to replicate the operation time of the level shifter. This approach minimize

the timing skew between the two paths.

It also requires a decoder that takes as input the bus from the digital core and outputs the control signal for each element. Then, a disoverlap block is needed to prevent both power MOSFETs from being ON at the same time, which would cause a short circuit between the supply and ground. Lastly, there is the resistor bank for the ringing damping and the T/R switch with its logic.

In this block there are 4 supply lines:

- GND
- VDD5V: The 5 volts rail to supply the low voltage circuits.
- VDDHV: The high-voltage supply line that is provided externally and that can reach up to 20V.
- RHVP: The high-voltage reference is a supply line generated at 5V below the VDDHV. This creates the second rail of the high-voltage domain and allows the circuits in that domain to operate between VDDHV and RHVP, experiencing a maximum drop of 5V.

3.1 Pulser

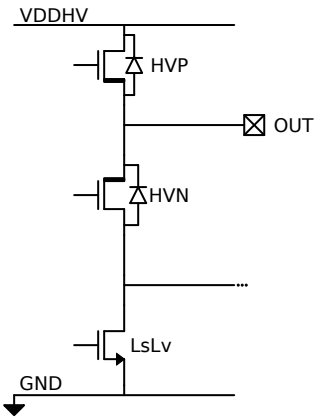


Figure 3.2: Highlight of the pulser components.

The output branch interfaces with the PAD to which the membrane is connected. It consists of HVP, HVN and LsLv as shown in Fig.3.2. HVP and HVN (high voltage P and N) are the two D-MOS transistors that sustain the high supply voltage, while LsLv (low-side low-voltage) is a 5V N-MOS transistor. Table 3.1 lists the parameters of these three transistors.

All 3 MOS are designed with the minimum L allowed by the design kit, to maximize their W/L ratio. Their width has been selected to achieve a

Mos	Voltage Class	Width	Ron
HVP	25 V	410 μm	45 Ω
HVN	27 V	170 μm	32.5 Ω
LsLv	5 V	200 μm	8 Ω

Table 3.1: Pulser components parameters.

rising and falling edge of the output node faster than 25 ns in all conditions, when driving the PMUT. The achieved value is approximately 23 ns for the typical production corner.

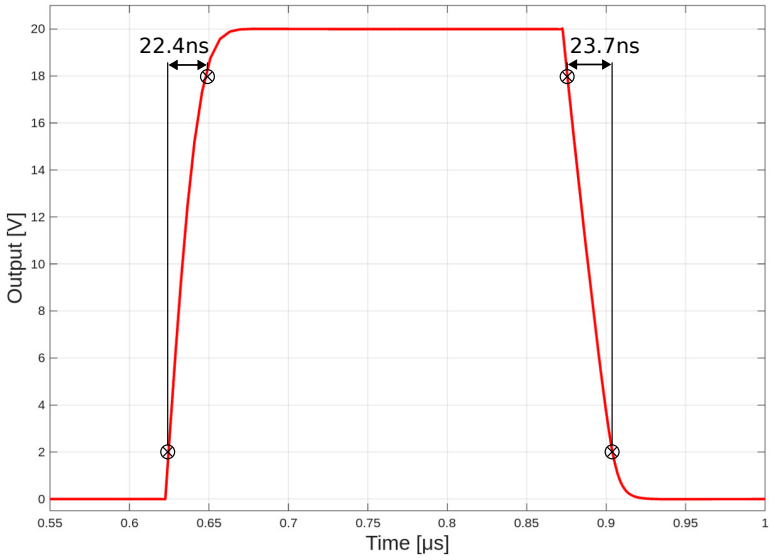


Figure 3.3: Output waveform of the pulser.

Table 3.2 shows the state of each element in the pulser during the different working phases of the TX block. It also includes the state of the T/R switch (RX) and the resistor bank (Res). During the driving phase the LsLv MOS is kept ON when the HVP is ON. This is to protect the low-voltage components, by preventing the node at its drain from remaining floating, which otherwise could raise its potential by collecting charges, for example, from the leakage current of HVN.

3.2 Level shifter

The D-MOS transistors can sustain a maximum VGS of 5V. Therefore, the HVN gate must be driven between GND and 5V, while the HVP gate must be driven between VDDHV and RHVP. However, the control signal for these

			Elements				
			HVP	HVN	LsLv	RX	Res
Phases	Driving	high	ON	OFF	ON	OFF	OFF
		low	OFF	ON	ON	OFF	OFF
	Reception		OFF	ON	OFF	ON	OFF
	Damping		OFF	ON	OFF	OFF	ON

Table 3.2: The table represents the state of each component during the different working phases of the TX block.

transistors is generated in the low-voltage domain. To properly drive the HVP, a level shifter is required to translate this control signal to the high-voltage domain where the transistor operates.

For the level shifter architecture four main topologies have been considered: resistive load inverter, pulse triggered SR latch, capacitive floating level shifter (CFLS), differential cascade voltage switch (DCVS).

3.2.1 Resistive-load inverter

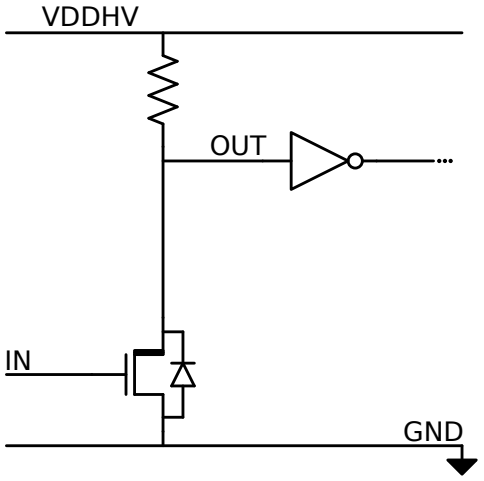


Figure 3.4: Resistive load inverter scheme.

The schematic of this configuration is depicted in Fig.3.4, as the name suggests, this configuration is based on a resistive-load inverter. It is a simple inverter created with an N-type transistor and a pull-up resistor. When the gate of the transistor is driven with a low logic state, the resistor pulls the output node up to the high-voltage rail. Conversely, when a high logic state is applied to the gate, the transistor turns on, lowering the output node. It is good practice to connect a chain of inverters at the output node to

regenerate the signal and minimize the capacitive load applied to the node. In this topology, the high voltage, drops across the transistor. Therefore, it is necessary to use a DMOS that can withstand the required voltage.

To ensure that the output node remains confined between the high-voltage domain rails, the current drawn by the transistor multiplied by the resistor value must equal the difference between the two rails (in this case 5 V).
This is not a reliable approach, as the manufacturing process spread and the operating conditions (temperature, imprecise rail voltage, etc...) can significantly alter these parameters, causing the output voltage to vary excessively. If the output is pulled down and the voltage drop across the resistor is too low, the signal will not be recognized. Conversely, if the drop is too high, it will damage the inverter, as it would apply a voltage higher than the technology limit.
Numerous methods can be applied to address this problem. This will not eliminate the problem but will prevent the voltage drop across the resistor from reaching an excessive value. Another parameter to consider is the time required for the transition. To reduce this delay, the transistor must draw a high current to discharge the output node's capacitance faster. This implies that the resistor value must also decrease (to maintain their product equal to the rail difference). As a result, the static consumption increases when outputting a low logic state.

This topology is inherently asymmetric because the pull-up of the node is performed through the resistor, while the pull-down is performed through the transistor. This results in an imbalance between the rise and fall times of the output.

The main advantage of this topology is the very low area required because it essentially needs only two components. Another key feature is that it automatically recovers in the case of a glitch that commutates the output.

The primary concern is its power consumption. When the output is at a high logic level, the power consumption is zero. However, when the output is at a low logic level, the power consumption equals the current drawn by the transistor multiplied by the supply voltage. This power consumption can be significant for circuits that handle very high voltages or for circuits that need to output a low logic level for an extended duration.

3.2.2 Pulse triggered SR latch

The schematic of this configuration is depicted in Fig.3.5. This configuration is an evolution of the resistive-load inverter described in the previous section 3.2.1. The goal is to reduce the steady state power consumption of the previous topology. The working principle is to use two resistive-load

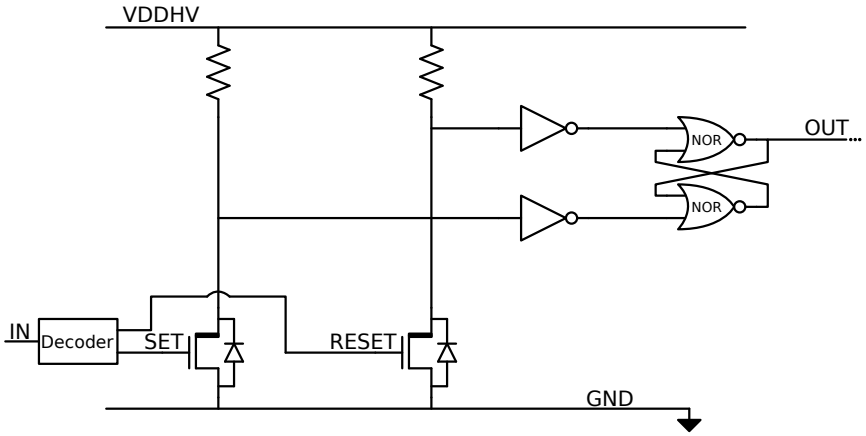


Figure 3.5: Pulse triggered SR latch scheme.

inverters, connected to the inputs of two NOR gates in a set-reset latch configuration. An inverter is inserted before the NOR gates to minimize the load applied on the resistive-load inverters. With this configuration to transmit a one or a zero through the level shifter, it is necessary to turn on the transistor on the set or reset branch. Those transistors are activated only for a short pulse, just enough to rotate the latch changing its output. With this method there is no static consumption for neither one of the two logic states. The delay introduced by the level shifter can be reduced by increasing the current drawn by the transistors when they are activated and reducing the resistors value. This is a significant concern for the simple resistive-load inverter, because the increased consumption is integrated over the entire duration when the output remains in the low logic state. While for this configuration, the increased consumption is integrated only over the short pulses. Therefore, the trade-off between the level shifter's delay and the consumption becomes more advantageous.

In this topology, as in the case of the resistive-load inverter, the high voltage drops across the transistors. Therefore, it is necessary to use DMOS transistors of an appropriate voltage class. These type of transistors are highly area intensive. Additionally, due to the added logic gates, this topology requires more than twice the area of the previous one. Another downside of this implementation is its inability to recover automatically from spike noise high enough to rotate the latch and change its output. The output remains incorrect until the next bit is sent through the level shifter. This issue can be mitigated by increasing the component size, which reduces the impedance driving the internal nodes. This modification increases the spike noise amplitude required to alter the output.

3.2.3 Differential Cascade Voltage Switch

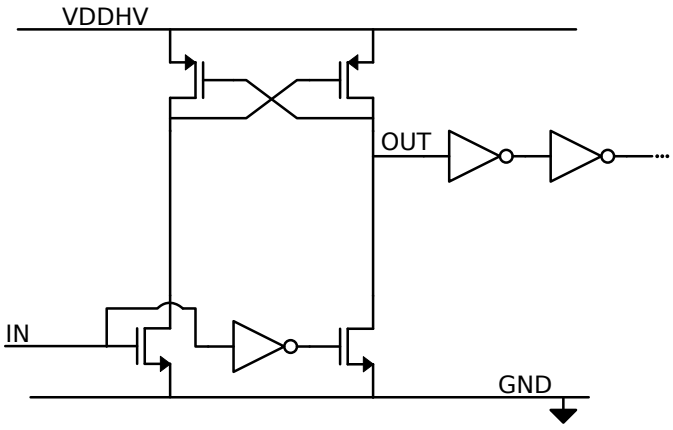


Figure 3.6: Scheme of the DCVS level shifter topology.

The core of this configuration is depicted in Fig.3.6. The two PMOS transistors are cross-coupled, creating a latch structure. The state of the latch can be changed by reversing the input. This action switches which of the two NMOS transistors is ON and which is OFF, effectively toggling the latch and thereby changing the output. To ensure this configuration works, the NMOS transistors must be stronger than the PMOS transistors, enabling them to overcome the PMOS latch and reverse its state. Also for this architecture, it is recommended to connect a chain of inverters after the latch, to regenerate the signal and prevent overloading the output node with excessive capacitance, which would slow down the transition.

The advantages of this scheme are the zero steady-state power consumption, because at equilibrium each branch has one of the two transistors turned off, and the ability to automatically recover from an involuntary change of the latch state, caused, for example, by a noise spike.

However, the circuit shown in Fig.3.6 cannot function as a level shifter because it is unable to withstand high voltages. To transform it into a proper level shifter, it is necessary to replace its components with transistors capable of withstanding high voltage. For the two NMOS transistors, the process is straightforward. It is sufficient to replace them with D-MOS transistors of an appropriate voltage class.

For the two PMOS transistors composing the latch, the transformation is more challenging because a DMOS can sustain a high voltage between its drain and source terminals, while the voltage drop between its source and gate is limited to the maximum drop of a normal MOS (for the technology used, this is limited to 5 V). However, the key feature of this level shifter topology is the latch created with the cross-coupled PMOS transistors. To operate, the gates of these transistors must experience the full voltage swing;

therefore, they cannot simply be replaced by DMOS.
To overcome this challenge, two DMOS-type P transistors are used to cascade the latch. By doing so, the high voltage drops across the DMOS transistors, which act as a shield for the low-voltage PMOS constituting the latch. The DMOS gates must be properly biased to ensure that their source does not fall below the RHVP. This prevents exposing the low-voltage transistors to an excessively high potential, which could damage them. At the same time, they must exhibit the lowest possible resistivity to avoid slowing down the commutation of the nodes, while always maintaining their VGS within the technology limit.

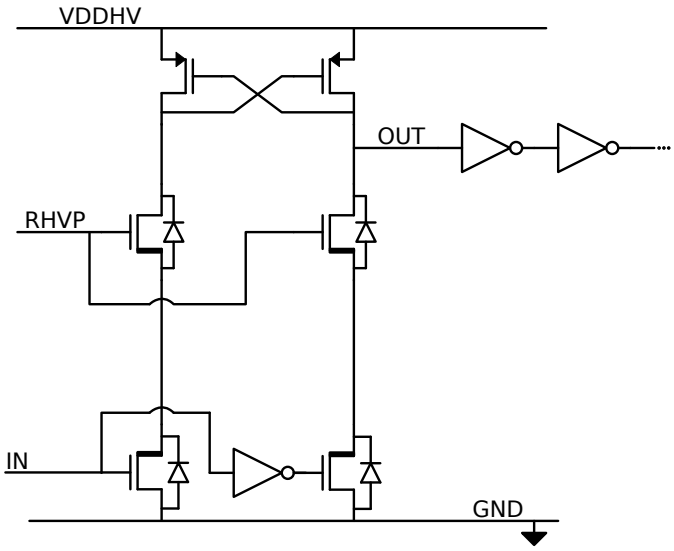


Figure 3.7: More detailed view of the DCVS topology.

The simplest way to properly bias the DMOS transistors, while complying with these requirements, is to connect their gates to RHVP. The main downside of this solution is that their VGS varies during the latch commutation, which changes the transistors conductivity. This issue can be mitigated by increasing their size (paying attention to the leakage). In particular, this becomes problematic toward the final phase of the latch commutation. However, by that time, the inverter chain will have already propagated the change in state. Therefore, the overall level shifter's delay is not significantly affected. The final configuration is depicted in Fig.3.7.

The only disadvantage of this topology is the area consumption. It utilizes four DMOS components, which, as already mentioned, are highly area-consuming.

3.2.4 CFLS

This topology [5] is the one selected to be implemented in the ASIC, as the best compromise between area usage, power consumption and noise immunity.
The schematic depicted in Fig.3.8 shows the core elements of this configuration. It is composed of a latch created with 2 inverters, and situated in

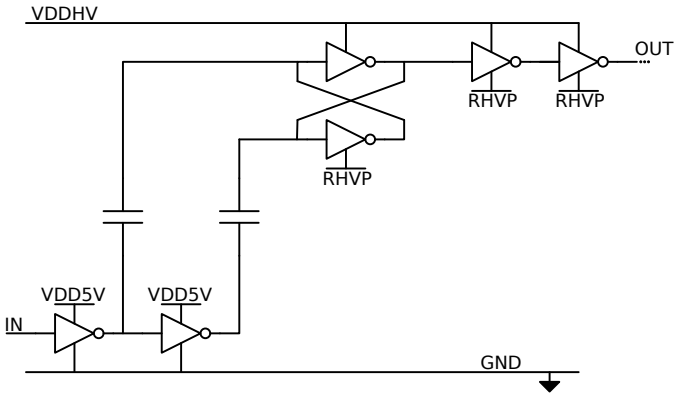


Figure 3.8: Basic representation of the capacitive floating level shifter scheme. The inverters composing the latch are supplied between VDDHV and RHVP.

the high-voltage domain. It is then connected via a chain of inverters to the output; this chain is present to regenerate the signal and minimize the capacitive load applied to the latch. The two latch nodes are also connected via a pair of capacitors to a couple of inverters situated in the low-voltage domain, which are driven by the input.

In this architecture the capacitors, are the elements that sustain the high-voltage drop. Therefore this topology can be implemented if the technology provides a variant of these components with the appropriate voltage class.

The level shifter uses the capacitors as voltage generators with a value equal to the desired voltage shift. Therefore, they must be charged with a potential difference equal to RHVP. The output of the two low-voltage domain inverters is shifted by the voltage stored inside the capacitors and applied to the latch in the high-voltage domain. Consequently, when the input switches, the first two inverters reverse the latch, changing the output logic level.

To select the best level shifter among the four options, the architectures are compared based on three criteria: power consumption, area occupation and noise immunity.

The consumption has been analyzed while performing two full commuta-

tions of the output, starting with an output logic level equal to zero and inverting it 3 times 0→1→0→1.
In this test the worst topology is the resistive-load inverter due to the non-zero steady state consumption.

Analyzing the area required to implement the different architectures, the DCVS stands out as the worst one. Even in their smallest possible implementations, the DCVS is 2 to 3 times bigger than the others, this is because it uses 4 D-MOS which are highly area demanding.

Regarding the noise tolerance, the worst case is a spike noise that capacitively couples to the level shifter nodes, those spikes are generated from the pulser when driving the membrane.

To compare the different topologies, with a realistic test case, a step voltage generator with an amplitude of 10 V, is connected through a capacitor to the weaker node of the level shifter under test. The voltage generator emulates the spike noise, while the capacitor models the capacitive coupling between the noisy node and the level shifter node. The analysis aims to find which architecture can sustain the bigger coupling capacitor, without propagating an error.

For the schemes containing a latch, the error is encountered when the noise rotates the latch state, permanently changing the output. While in the case of the DCVS and the resistive-load inverter, that can automatically recover the output, the error is encountered when the output varies more than half dynamic, which would propagate a glitch through the inverter chain.

From the different analysis, the two best architectures are the pulse triggered SR latch and the CFLS. Between these two, the CFLS is the one that can be implemented using the smaller area, since it doesn't imply any D-MOS but relay only on high-voltage capacitors. Comparing their minimum realizations, the pulse triggered SR latch is 1.8 times bigger than the CFLS, therefore the difference in area can be used to increase the CFLS noise resistance.
To properly compare the two architectures, the CFLS has been improved until it reached the same area of the pulse triggered SR latch. From the tests results the CFLS is much more robust against the noise, and is also more energy efficient, although with a smaller margin.

Thanks to these results the CFLS architecture has been chosen as the one to be implemented in the ASIC. The table 3.3, summarizes the comparison of the various topologies under the three criteria.

However, this architecture presents a critical point: the voltage stored in the capacitors must always remain equal to RHVP.
In steady state it is not a problem, the input inverters connect one of the two

	Resistive-load inverter	Pulse triggered SR latch	DCVS	CFLS
Area occupation	**Best**	Bad	Worst	Good
Consumption	Worst	Good	Bad	**Best**
Noise immunity	Good	Worst	Good	**Best**

Table 3.3: Level shifter topologies comparison.

terminals of the capacitors to a low-voltage supply rail, GND or VDD5V. While the inverters of the latch ensure that the other terminal is connected to one of the high-voltage rails, VDDHV or RHVP.

It became an issue during the start up of the circuit, when the latch assumes a random state, this can lead to one capacitor being charged to VDDHV and the other being charged to $RHVP - 5V$.

To prevent this unpredictable condition, a reset signal has been added to drive a pair of MOSFETs, steering the output toward the known default state. That is the state for which the output DMOS HVP is off. The reset signal is also kept active, clamping the latch in the default state, outside of the driving phase, where the HVP must remain turned off.

The issue became more challenging during the transition, when the input inverters switch their outputs, forcing the latch to change state through the capacitors. During the commutation, two phenomena attempt to change the charge stored in the capacitors. Initially when the capacitors are shifted up or down to the new voltage level, the stored potential is perturbed by the charge sharing, occurring between the main capacitors and all the parasitic capacitances impinging on the latch nodes. The following effect occurs during the time between the start of the transition and the state change of the latch. In this time frame the inverters discharge one capacitor and overcharge the other.

To minimize the first phenomena, the components connected to the latch nodes, must be as small as possible to reduce their parasitic capacitance. While to reduce the second effect, the input inverters must be significantly bigger than the latch ones, to force the transition to occur as quickly as possible.

A possible solution to limit the issue in both cases, is to increase the size of the capacitors. This reduces the change in voltage for the same variation in the stored charge. However, this approach highly affects the area occupation, since these capacitors are high-voltage components which are very area demanding. After the transition occurs, the latch, which has the smallest inverters, must restore the charge inside the capacitors. Therefore, a high capacitance value with minimum-size latch is not a good solution, since it leads to a long restoring time.

The final implementation is drawn in Fig.3.9. In the final schematic,

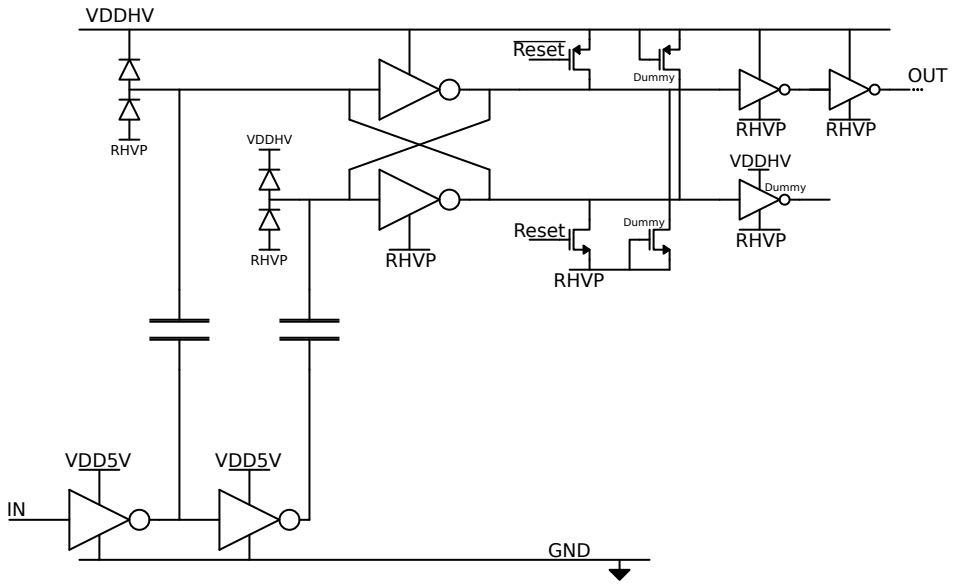


Figure 3.9: Complete representation of the capacitive floating level shifter scheme as implemented inside the ASIC.

two pairs of diodes have been added to the latch terminals, to protect the components in case the capacitors get overcharged or undercharged. If the voltage stored inside them differs from RHVP, when they are shifted up or down during the transition, they can push the latch nodes outside the high-voltage supply rails. Causing the latch to experience a higher voltage drop than the one its components are rated for.

In the final schematic, a pair of MOS transistors and a dummy inverter were added to maintain symmetry in the two branches of the latch. This adjustment ensures that the two output transitions, from 0 to 1 and from 1 to 0, occur in the same amount of time.

Some specifications:
The delay introduced by the level shifter is 1.08ns for the 0→1 and 1.14ns for the 1→0 transition. This delay is calculated as the time that elapses from when the input rises above 10% of its dynamic range to when the output rises above 10% of its dynamic range. The same applies to the falling delay, but with the threshold set to 90% of their dynamic ranges.

3.3 DisOverlap

The purpose of this element is to prevent both power D-MOS transistors, from being ON simultaneously. This block receives a signal from the decoder as input. When the signal has a logic level of 1, HVP must be ON and HVN OFF. Conversely, when the signal has a logic level of 0, HVN must be ON

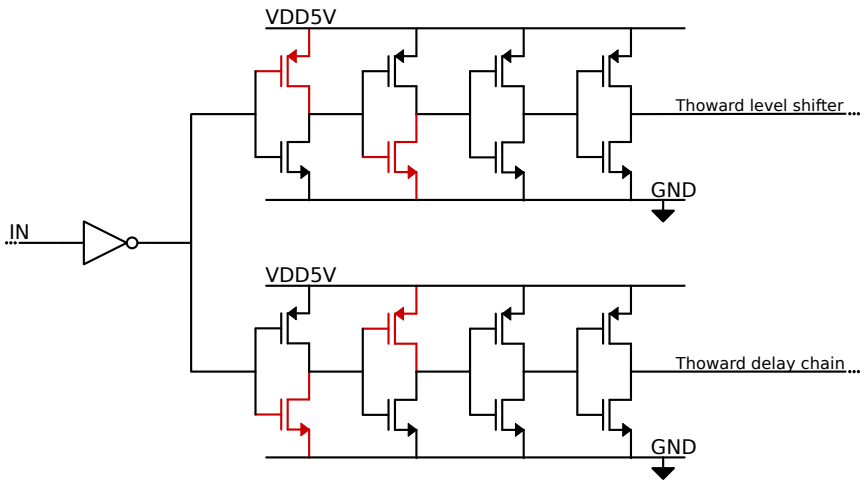


Figure 3.10: Disoverlap scheme. The MOS transistors in red represent the ones with minimum W and increased L.

and HVP OFF.

The goal is to turn OFF the active D-MOS before turning ON the other one. To achieve this, the circuit has two internal paths that drive two outputs: the high-side path, whose output is connected to the level shifter propagating its signal to HVP, and the low-side path, whose output is connected to the delay chain propagating its signal to HVN. The blocks connected between the output of this element and the corresponding power transistor do not invert the logic state of the signal. Therefore, the logic state of the two outputs matches the one applied to the gate of the corresponding D-MOS. These internal paths consist of a chain of unbalanced inverters that favor one transition over the other, as depicted in Fig.3.10.

For the high-side path, the input transition 1→0 generates a transition 0→1 at its output, which turns OFF the HVP transistor. Therefore, this signal propagates through the inverter chain without any added delay. Conversely, the input transition 0→1 generates a transition 1→0 at the output, which turns ON the D-MOS. As a result, this signal is delayed by the inverter chain. For the low-side path, the situation is the opposite. The input transition 0→1 turns OFF the HVN transistor and propagates without any added delay. Conversely, the input transition 1→0 turns ON the D-MOS and must be delayed.

The delay in propagation is created by using transistors with minimum width and increased length on the inverter side that will propagate this transition, they are depicted in red in Fig.3.10. Because the two paths must delay opposite transitions, the inverters that form the respective chains are also unbalanced in an opposite manner.

The last two elements for both chains, are normal symmetric inverters,

their role is to square the signal before output.

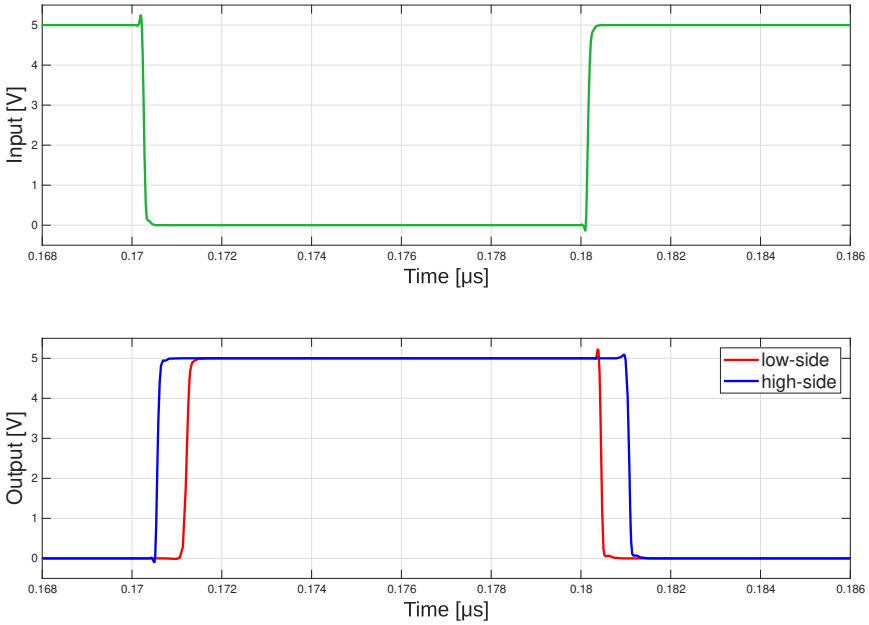


Figure 3.11: Disoverlap outputs over the input signal.

The output signals over the input, are shown in Fig.3.11, the blue output is generated by the high-side path and drive HVP, while the red output is generated by the low-side path and drive HVN. The figure illustrates how the edge that triggers the activation of the corresponding DMOS is delayed, whereas the deactivation edge does not experience additional delays. This creates a separation between the transitions of the two output waveforms.

The separation delay between the two outputs is designed to be 620 ps. This target value has been selected by considering the spread in the propagation delay of the following blocks, across all operating corners, and the variation in the delay generated by this block. Therefore, 620 ps is selected as the nominal value to ensure that the ON-ON condition is avoided in all manufacturing corners.

3.4 Charge injection

The charge injection issue affects the MOSFETs used as switches [6]. When a MOSFET is turned ON, it accumulates charges in the gate capacitances, C_{gd} and C_{gs}, and inside the channel. These charges are released from the source and drain terminals once the MOSFET is turned OFF. It can be assumed that the charge flowing into and out of the transistor is equally divided between the drain and the source.

The overall accumulated charge depends on the transistor size and the Vgs applied to activate the switch. It can be calculated as:

$$Q_{ch} = W \cdot L \cdot C_{ox} \cdot (V_{gs} - V_{th}) \tag{3.1}$$

Where Q_{ch} is the stored charge, W and L are the transistor's width and length, C_{ox} is the gate oxide capacitance, V_{gs} is the applied gate-source voltage to turn on the MOS and V_{th} is the threshold voltage of the transistor.

This charge is injected into the adjacent nodes, creating an instantaneous variation in their voltage. This sudden variation can lead to an error in the digitization of a signal or saturate an amplifier.

In the TX block, this issue occurs during the switching of LSLV and the T/R switch.

3.4.1 LsLv charge injection

The charge injected from this transistor creates an issue when it is turned OFF. During that transition, the charge injected from the drain flows into the PMUT, as it is the only available path at the moment. This can cause an unintended excitation to the membrane, increasing the ringing issue.

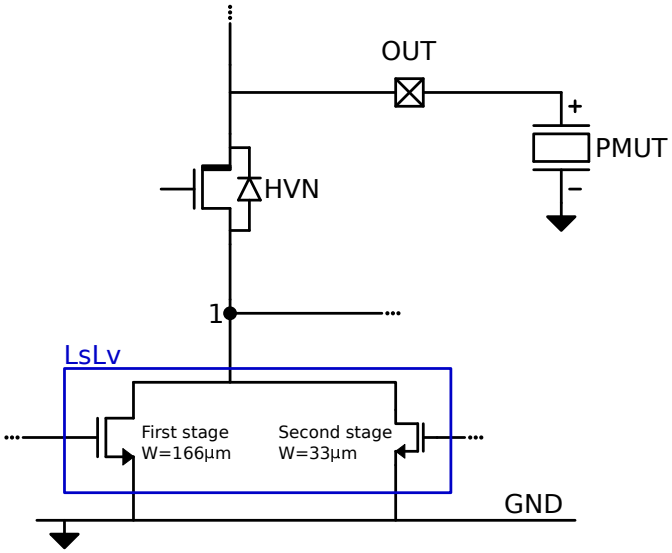


Figure 3.12: LsLv stages subdivision.

To reduce the amount of injected charge, the LsLv transistor has been divided in two segments, as depicted in Fig.3.12. The first segment accounting for 83% of the original width, and the second accounting for the remaining 17%. The purpose of this division is to split the MOSFET shutdown process into two stages. Initially both segments are ON, the shutdown sequence

start by turning OFF the main segment, while the smaller one remain active creating a low-impedance path to ground, this allows the charge to flow towards GND. Subsequently, the second stage is turned OFF. At this point, the charge from the second segment will inevitably flow towards the PMUT. However, since this second stage is significantly smaller in size, the charge it injects is also reduced.

In the Fig.3.13, is depicted the voltage on node 1 during the shutdown of LsLv with and without the subdivision of the transistor in stages. The red curve shows the voltage variation on node 1, in the case of a single LsLv transistor. The curve in blue depicts the variation in voltage of node 1, if the shutdown of the MOS is subdivided in two phases. Analyzing the segmented

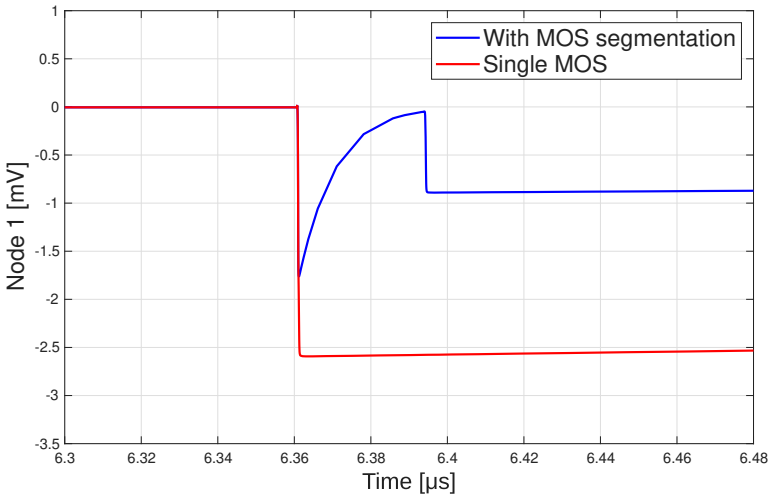


Figure 3.13: LsLv charge injection, waveform.

solution, an initial voltage drop is observed due to the shutdown of the first stage. This drop is smaller compared to the single MOS case, because the section being turned OFF is smaller, thereby injecting less charge. Additionally, the injected charge flows to GND through the second stage, which remains active and discharges the node. Subsequently, a second voltage drop occurs due to the charge injected during the shutdown of the second stage. However, this second section is smaller in size, injecting significantly less charge and causing minimal disturbance to the node. Even if there is an initial spike in the node 1 potential, it reduces the excitation to the PMUT compared to the single-MOS case. This is because the spike has a smaller amplitude and recovers much faster than the PMUT can react.

3.4.2 T/R switch charge injection

The T/R (transmit/receive) switch connects the RX chain to the PMUT during the receiving phase and disconnects it during the other phases. It

also includes a clamp that connects the LNA input to GND for the common mode polarization of the amplifier. The clamp is active outside the receiving phase and is driven with the opposite phase relative to the T/R switch. The schematic of this block components is shown in Fig.3.14. This switch consists

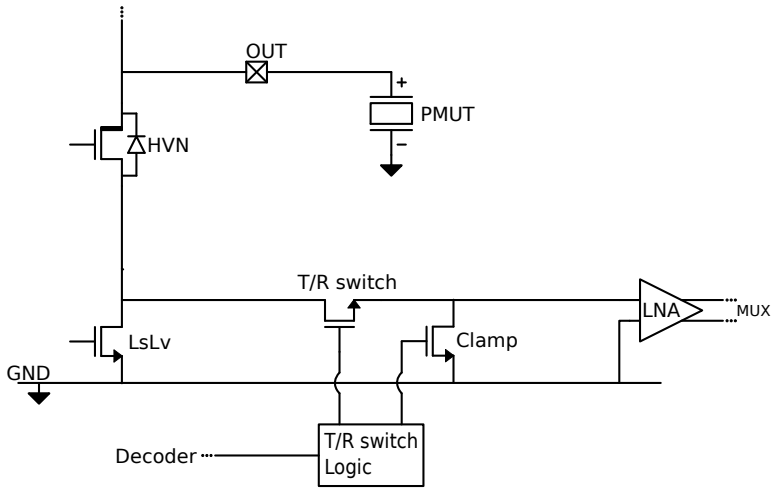


Figure 3.14: T/R switch base scheme.

of an N-MOS with a width of 150 µm. This size is chosen to minimize the transistor Ron, reducing signal attenuation through the switch. The low impedance also aims to reduce the voltage drop across the transistor, to minimize the switch resistance modulation caused by the signal, thereby minimizing the resulting signal distortion.

The charge injected from this transistor causes an issue both when it is turned ON and when it is turned OFF. This occurs because it injects charge directly into the LNA input. Therefore, the induced change in voltage is amplified, which became especially problematic when the overall RX chain is set to a high gain, as this voltage variation could saturate the amplifiers.

The maximum gain of the RX chain is 73 dB and the output dynamic range is ±1.5 V. To avoid saturation, the change in the input voltage must be less than 310 μV. Achieving this goal across all the production corners is very challenging. To meet this requirement, several approaches are combined: the T/R switch is divided into stages, a dummy switch is added, and the clamp switch is used with adjusted timing to absorb the charge. The final scheme is presented in Fig.3.15.

The main T/R switch transistor is subdivided into three stages. S1 is the primary stage and accounts for 66% of the total width. Then, in decreasing order, S2 accounts for 20%, and S3 accounts for the remaining 13% of the total width.

The dummy switch is added to absorb the charge injected into the node. It is 80 μm in width, which is approximately half the size of the T/R switch.

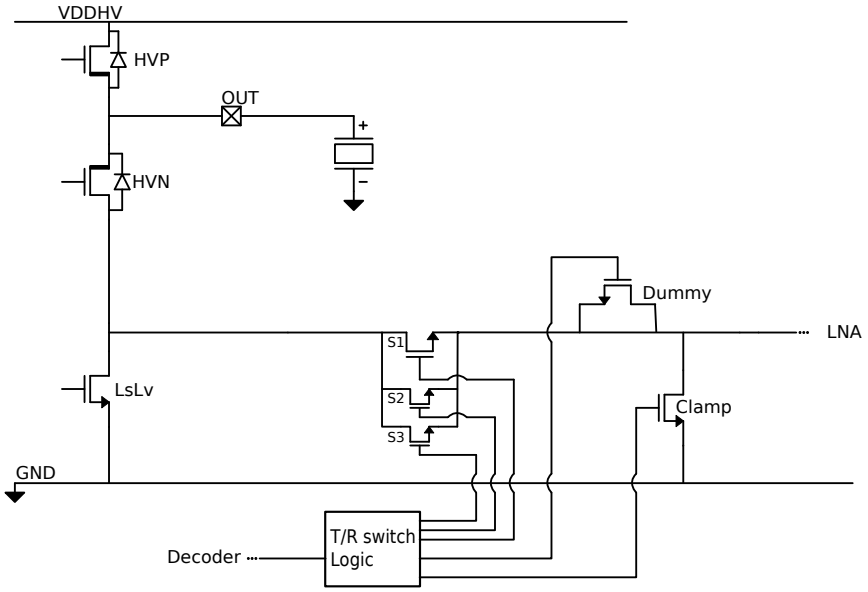


Figure 3.15: T/R switch complete scheme.

This is because the charge flowing in and out of the transistor is split roughly in half between its source and drain terminals. The dummy switch is driven in opposite phase relative to the T/R switch. This is because both are N-MOS transistors; in this way, the dummy switch absorbs charges when the T/R switch injects them, and vice versa.

The clamp transistor's function is to connect the LNA input to ground, for its common-mode polarization. The clamp is driven in opposite phase with respect to the T/R switch, so it is active when the switch is open and inactive when the switch is closed. The timing of its transition has been tuned to help absorb the injected charge. The concept is to keep the clamp active during the commutation of the T/R switch to create a low-impedance path toward the ground, allowing the charge to flow in this direction.

Regarding the transition to the reception phase and therefore the closure of the T/R switch, the driving of the individual transistors occurs following the sequence presented in table 3.4.

Fig.3.16 shows the voltage at the LNA input node during the transition into the reception phase. The green curve represents the voltage at this node, while the pink curve is a mathematically filtered version of that voltage, obtained by applying a low-pass filter function with a 5 MHz bandwidth. This bandwidth matches that of the LNA and thus represents the amplifier's output trend in response to the input signal. The marked points in the figure, corresponds to the time instance when each transition listed in table 3.4 occurs. It can be seen from the green curve how the voltage of the node is affected from each transistor commutation. The charge adsorbed from

1°	The first stage of the T/R switch (S1) is closed.
2°	The dummy is deactivated.
3°	The second stage of the T/R switch (S2) is closed.
4°	The third stage of the T/R switch (S3) is closed.
5°	The clamp is released.

Table 3.4: Sequence for driving each element during the transition into the reception phase of the T/R switch. (The dummy is active when its gate is connected to VDD5V, forming the channel. It is inactive when its gate is connected to GND, and the channel is not formed).

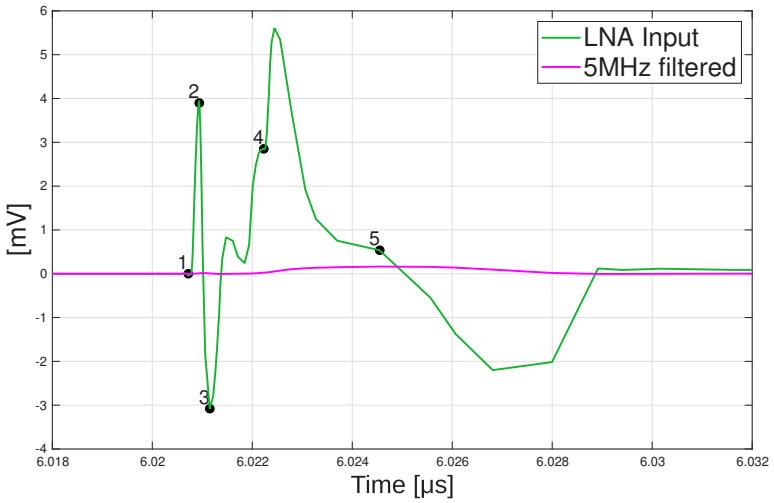


Figure 3.16: Voltage at the LNA input during the T/R switch closure.

turning on an N-MOS increases the voltage of the node, while the charge injected from turning off an N-MOS decreases the voltage.

The pink curve, being a filtered version of the input voltage to the LNA, effectively represents an average of the green curve and is the one of real interest in meeting the 310 μV condition. This curve exhibits a maximum in correspondence with point 5, where it reaches 160 μV, and then asymptotically approaches 83 µV. The initial condition was therefore largely met.

Regarding the transition to open the T/R switch, disconnecting the LNA from the PMUT. The driving of the individual transistors occurs following the sequence presented in table 3.5. As mentioned earlier, the clamp is used to create a low-impedance path to ground during the commutation of the T/R switch. This helps reduce voltage spikes. For this transition, the clamp is the first element which gets activated before initiating the sequence to open the T/R switch. The Fig.3.17 shows the LNA input node and the PMUT voltage, during the opening of the T/R switch. The green curve represents the LNA input voltage, while the pink curve is the filtered

1°	The clamp is released.
2°	first stage of the T/R switch (S1) is opened.
3°	The dummy is activated.
4°	The second stage of the T/R switch (S2) is opened.
5°	The third stage of the T/R switch (S3) is opened.

Table 3.5: Sequence for driving each element when transitioning out of the reception phase. (The dummy is active when its gate is connected to VDD5V, forming the channel. It is inactive when its gate is connected to GND, and the channel is not formed).

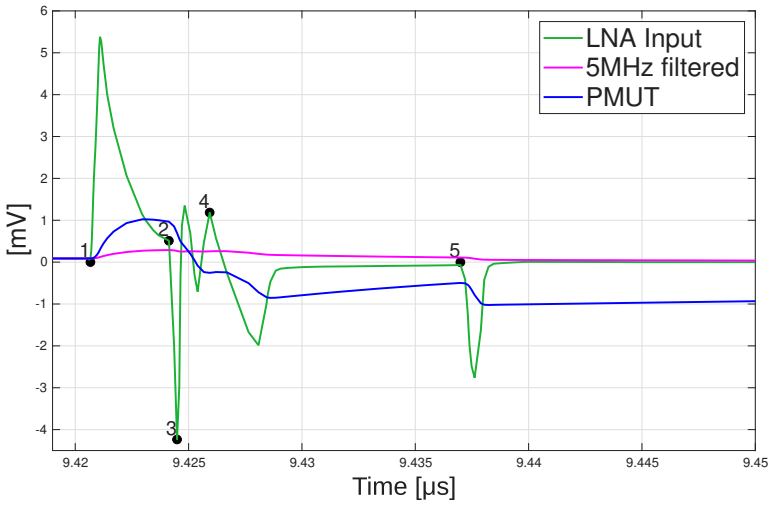


Figure 3.17: Voltage at the LNA input during the T/R switch opening.

version of it, using a low-pass filter with a 5 MHz bandwidth. The blue curve depicts the PMUT voltage. The marked points in the figure, correspond to the time instance when each transition listed in table 3.5 occurs. This time the switching of each element has the opposite effect to the node voltage, because all the transitions are reversed. In this commutation, the T/R switch opens, disconnecting the PMUT from the LNA and therefore also from the element used to reduce the injected charge. Consequently, the charge expelled from the switch toward the transducer is not attenuated, which can lead to unwanted excitation. To mitigate this issue, the last stage of the switch (S3) remains closed for a relatively long period. This creates a path between the PMUT and the LNA side, allowing the dummy and the clamp to absorb the charge.

One final approach to reduce the injected charge, present in the literature but not applicable to the final design, is to use a pass gate[1] instead of

[1]Pass gate: a P-MOS and a N-MOS connected in parallel, driven with complementary

the T/R switch composed solely of N-MOS transistors. This is because when simultaneously opening and closing a P-MOS and an N-MOS, they inject opposite charges that counteract each other. However, this approach cannot be used in this design since the switch needs to operate around GND. Therefore, the P-MOS will not create a channel if its gate is driven with 0 V. To correctly turn on the transistor, the gate should be driven with a negative voltage, which is not present in the ASIC.

3.5 T/R switch Logic

This logic must provide the driving signal for each transistor composing the T/R switch with the correct timing, starting from a single signal coming from the decoder. When this signal has a high logic level, the T/R switch must close, connecting the PMUT to the RX chain. Conversely, when the signal assumes a low logic level, the T/R switch must open.

This element must introduce delays to drive each transistor with the correct timing. To achieve this, minimum-size inverters with capacitors as loads are used. The selected delay is created by adjusting the number of stages.

The most intricate aspect is positioning the transition of the clamp, either at the beginning or the end of the sequence, depending on the transition in question. To achieve this goal, the circuit depicted in Fig.3.18 is used.

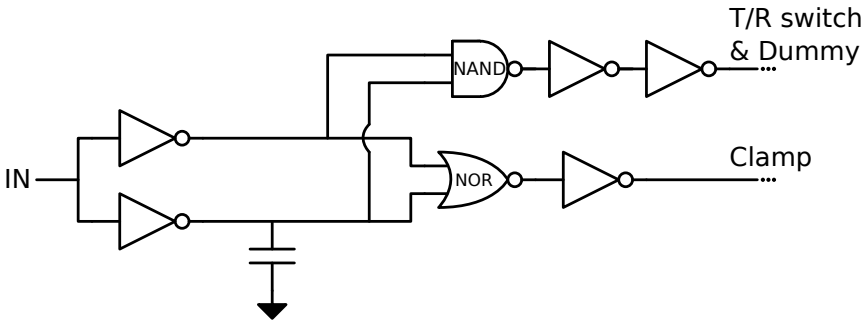
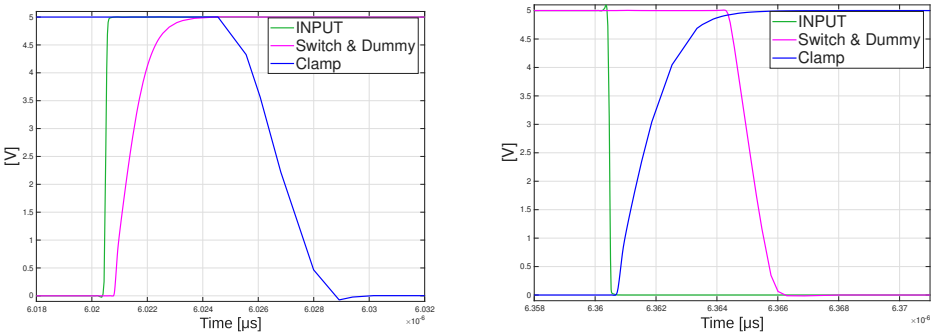


Figure 3.18: T/R Switch logic, scheme.

This scheme generates two signals: one drives the clamp transistor, and the other is directed to the delay elements. Where the signals to drive the T/R switch and the dummy are derived with the appropriate timing. The Fig.3.19, shows the outputs and input waveforms of this circuit. During the $0 \rightarrow 1$ transition of the input signal shown in Fig.3.19(a), the output directed to the switch commutates immediately, while the output directed

signals, ensuring that both are either ON or OFF simultaneously. They are used to transmit the signal regardless of its level and to minimize the resistivity modulation of the switch caused by the signal.

to the clamp is delayed to keep it active during the transition. Conversely, during the 1→0 transition of the input signal shown in Fig.3.19(b), the output driving the clamp commutates immediately after the input, while the output directed to the switch is delayed to allow the clamp sufficient time to turn on. As shown in the graph, the edges of the clamp drive signal are slowed down to avoid feed-through toward the drain.



(a) Outputs closing the T/R switch

(b) Outputs opening the T/R switch

Figure 3.19: The outputs of the T/R switch logic for the two transitions.

3.6 Resistor bank

The purpose of this component is to attenuate the ringing passively, by connecting a resistor to the transducer. As explained in section 2.4.2, the best way to attenuate the ringing using a passive approach, to avoid unwanted re-excitation, is to connect the PMUT to a resistor. To obtain the maximum attenuation, the resistor value must be precisely tuned to the impedance of the membrane it drives. Nevertheless, not all transducers exhibit identical parameters, even within a single transducer, each of the 25 membranes has different characteristics although to a much lesser extent. Therefore to maximize the ringing attenuation for each membrane, is mandatory to connect a resistor with a value tuned to its characteristics.

To implement this request, the circuit shown in Fig.3.20 has been designed. It consists of two resistor banks. The first bank can impose resistance values at the output between 1 kΩ and 7 kΩ in steps of 500 Ω; this range was selected based on the tests results presented in section 2.4.2, which indicate the optimal resistor value to be approximately 4 KΩ. While the second bank provides three resistance values: 53.5 kΩ, 55.25 kΩ and 57 kΩ.

The first bank of resistors, with values between 1 KΩ and 7 KΩ, is designed to damp PMUTs manufactured using PZT as the piezoelectric layer, which are the target transducers for the ASIC. The second bank of resistors,

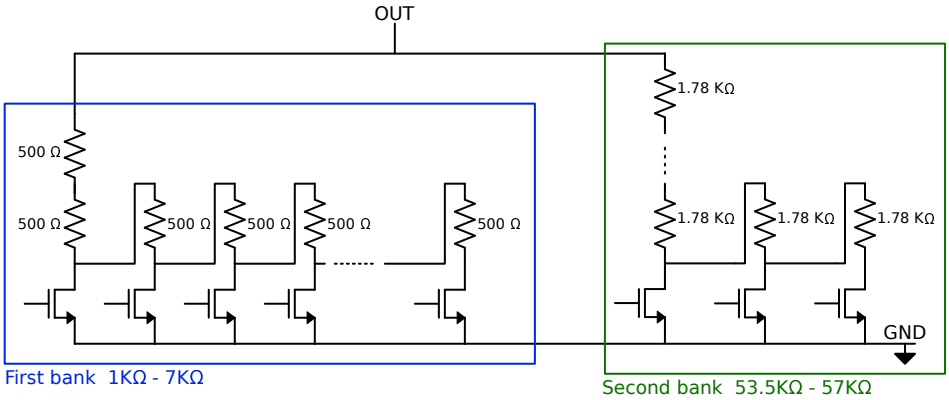


Figure 3.20: Resistor bank scheme.

with values between 53 KΩ and 57 KΩ, is intended to damp PMUTs manufactured using ScAlN as the piezoelectric layer. This design widens the capability of the integrated circuit. However, since this PMUT topology is not the primary target for the ASIC, the second bank offers a more limited range of resistance values

Each bank consists of a series of resistors, with transistors used as switches connected between ground and the intermediate nodes of the resistor chain. This configuration allows a portion of the series to be bypassed, modulating the resistance observed at the input node. If all the transistors remain open, the resistor chain is left floating, presenting an open circuit to the input.

For matching purposes, each bank is constructed using instances of a unitary resistor module, connected in series or parallel to achieve the desired value. In the case of the first bank, which realizes resistances between 1 KΩ and 7 kΩ. The unitary segment is composed of a module of 500Ω.

The resistor chain is designed considering the size limitations imposed by electromigration. For the same applied voltage across the resistor bank, selecting a low resistance value results in higher current flowing through the selected modules, compared to when higher resistance values are chosen. To ensure compliance with the current density limits imposed by the technology, more modules are placed in parallel to increase the width of the banks that handle the higher currents. The resulting strips are then stacked to achieve the desired resistance value, forming a matrix of unitary modules. As the chain progresses, the magnitude of the current decreases, and so does the size of the matrix, until reaching the last element, which is composed of only one unitary module. These requirements also apply to the transistors used to bypass the chain. Therefore, the switches that select a smaller portion of the chain are designed with a larger width to sustain the higher current. The dimensions of these transistors are tapered as they approach the end of

the chain.

The same approach is used to implement the second bank, which provides resistances between 53 KΩ and 57 kΩ. For this resistors chain, the unitary module has a resistance of 1.78 kΩ.

Chapter 4

Rx chain

The RX chain is composed of different elements to amplify, re-route and filter the signal coming from the membranes. The chain consists of the following components, in order: LNA, multiplexer, PGA, programmable filter, and the SAR ADC as shown in Fig.4.1.

All elements of the chain are powered at 3 V to keep the final ASIC's power consumption low, except for the ADC, which is powered at 1.2 V.

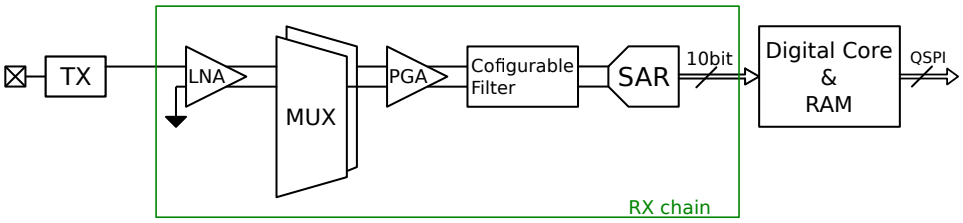


Figure 4.1: Highlight of one of the 5 receiving chains.

4.1 LNA

The LNA is at the beginning of the reception chain, to amplify the signal coming from the transducer immediately after the T/R switch. The amplifier receives the signal captured by the membrane as input, and outputs a differential amplified version of it. The LNA has programmable gain and incorporates the time gain compensation (TGC), which adjusts the gain during the reception phase, to compensate for the propagation attenuation accumulated by the traveling sound wave.

The scheme of the LNA is shown in Fig.4.2, it consists of a fully differential two-stage operational amplifier with capacitive feedback. To implement the amplifier feedback, capacitors are used instead of resistors to minimize

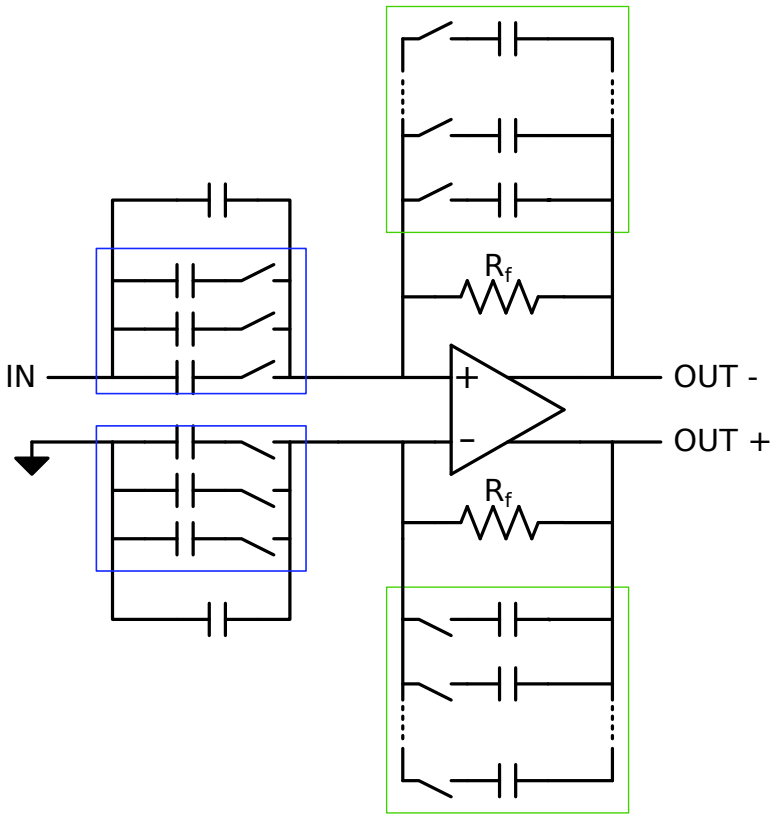


Figure 4.2: LNA scheme, the capacitor banks highlighted in green are used to set the amplifier gain, while the capacitor banks depicted in blue are used by the TGC to vary the gain over time.

the noise figure of this block, by avoiding the use of noisy components like resistors are.

To set the amplifier gain, the capacitors highlighted in green are connected or disconnected to modify the feedback value. This operation occurs only during the programming of the ASIC, and the selected gain value remains fixed until reprogramming. The TGC adjusts the gain of the LNA during the reception phase, by progressively increasing the gain over time. This compensates for the higher attenuation accumulated by the signal traveling further. The TGC adjust the gain by acting on the capacitors at the input of the amplifier, highlighted in blue.

To select the amplifier gain, 3 bits are allocated. These bits allow the management of 8 different gain levels, ranging from a minimum of 14 dB to a maximum of 35 dB, with a progressive step of 3 dB between the different configurations. For the TGC, there are four configurations available, ranging from 0 dB to 3 dB, with a step of 1 dB.
The resulting frequency response is shown in Fig.4.3, which illustrates three

different gain configurations, each with the four possible TGC values.

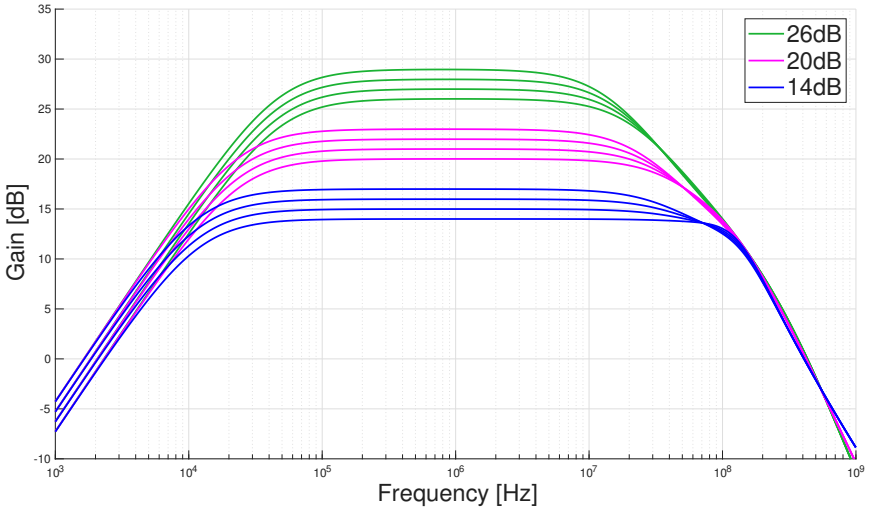


Figure 4.3: LNA frequency response in three different gain configurations: 14 dB, 20 dB, and 26 dB. For each of the three configurations, the frequency responses are shown with the four possible gain settings of the TGC.

The switches used to connect and disconnect the capacitors are designed using pass gates, with dimensions proportional to the capacitor they are connected to. This design ensures that the zero created between each feedback capacitor (green bank) and its switch resistance remains at a higher frequency compared to the second pole. At the same time, the area used by these switches is minimized.

To ensure the correct polarization of the capacitors in the feedback network of the amplifier, switches (not shown in Fig:4.2) have been added. These elements operate outside the reception phase to pre-charge the capacitors and maintain them at the correct voltage level, until the LNA starts amplifying the received signal.

For this operation the clamp switch, represented in the T/R switch in FIG.3.15, connects the amplifier input to ground. Additionally, two switches short-circuit the LNA inputs to the outputs, closing it in a buffer configuration. For each input capacitor of the TGC, a switch on their second terminal connects them to the common-mode reference rail of 1.5 V, therefore charging these capacitors between 0 V and 1.5 V.

These switches are operated in opposite phase to those controlled by the TCG. This ensures that the capacitors are pre-charged and that the charge is maintained until they are connected to the amplifier input. This operation minimizes the settling time during the gain commutation performed by the TGC.

4.2 Multiplexer

The goal of this element is to collect the signal from the LNA of each channel and rout it to the selected receiving path. After the LNA, the signal path is differential, therefore the ASIC includes two multiplexers: one to handle the positive differential signal and one to handle the negative differential signal. The multiplexers have 25 inputs, one for each channel of the ASIC interfacing with the transducer, and 5 outputs connected to the 5 reception paths.

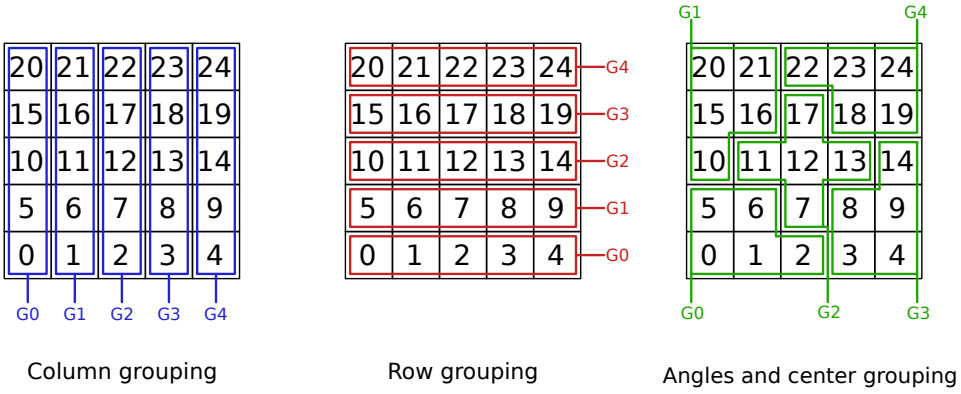


Figure 4.4: Shows the three different possible configurations in which the multiplexer can group the individual membranes within the transducer matrix.

Since there are only 5 receiving paths, this element combines the matrix membranes into five macro groups that can be created selecting among three different shapes: by columns, by rows, or by corners and center, as shown in Fig.4.4.

The five macro groups can then be connected independently, each to a separate output of the multiplexer. Or alternatively, they can be shorted together to a single output, sensing all the PMUT matrix as one big element. Partial groupings can also be created, such as connecting two or three groups to a single output and the remaining groups to other outputs.
It is also possible to select whether each of the elements contained within these main subdivisions must actually be connected to the final output or not.

The multiplexers are implemented using a matrix of switches that direct the 25 inputs to the selected output, through the grouping explained earlier. These switches are implemented using pass gates.

Each input has a 5KΩ resistor in series, it counts as the first resistor of the PGA feedback, as depicted in Fig.4.5. This implementation creates a

summing amplifier to combine the voltages of the inputs directed to that same output. It operates by leveraging the virtual ground at the operational amplifier input to merge the currents generated from the voltage drop of each input on the 5KΩ resistor and produce an output proportional to the sum of these currents.

$$V_{out} = \sum I_{in} \cdot R_f \qquad\qquad I_{in_x} = \frac{V_{in_x} - 1.5V}{R_{in}} \qquad (4.1)$$

This design also leverages the low-impedance node, enabled by the virtual ground, to minimize the voltage excursion experienced by the switch matrix, due to the input signal. This reduces the modulation of the switch resistivity, caused by the signal altering their Vgs, thereby reducing the signal distortion effect that this resistivity modulation implies.

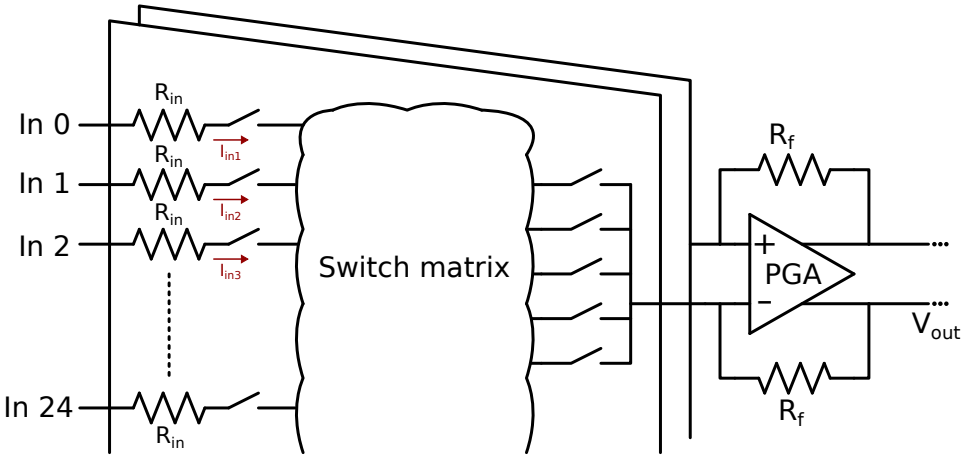


Figure 4.5: Internal scheme of the multiplexer.

4.3 PGA

The programmable gain amplifier (PGA), is the first element inside the five receiving chains. As mentioned, it is used as summing amplifier, to combine all the inputs directed to its chain by the multiplexer and amplify the resulting signal.

It is implemented using an operational amplifier with a programmable resistor in feedback, to modify its gain, as shown in Fig.4.6. The programmable resistor is implemented as a bank of resistors with different values connected in parallel. Each branch includes a switch to connect the resistor to the amplifier input or leave them open.

Also in this block, the switches are designed as pass gates and are positioned towards the input of the amplifier, leveraging the virtual ground to reduce the voltage swing experienced by the switch. This aims to minimize the signal distortion caused by the modulation of switch resistance.
The feedback loop also includes a capacitor to create the dominant pole and compensate the amplifier.

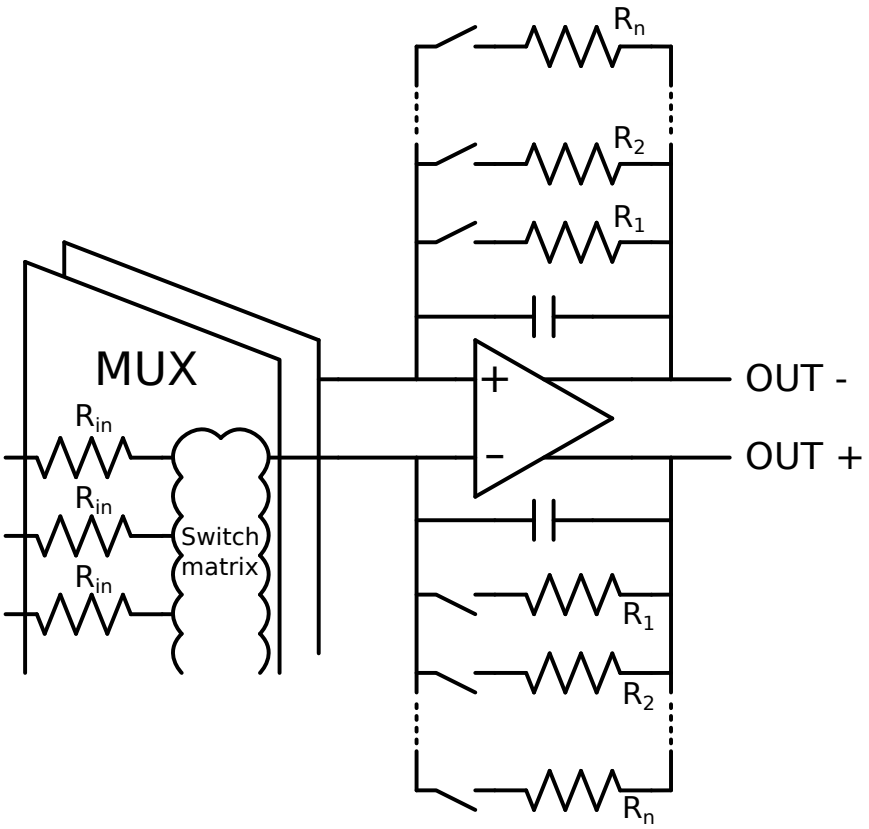


Figure 4.6: PGA internal scheme.

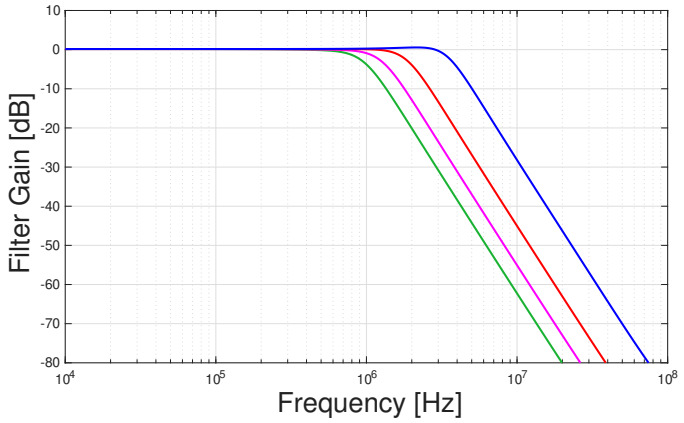
To ensure high versatility of the final ASIC, a wide range of possible gains have been provided for this amplifier. Specifically, 3 bits have been allocated for gain selection. Which allows the management of 8 different gain levels which are: -6 dB, 0 dB, 6 dB, 12 dB, 18 dB, 24 dB, 30 dB, and 36 dB.

4.4 Filter

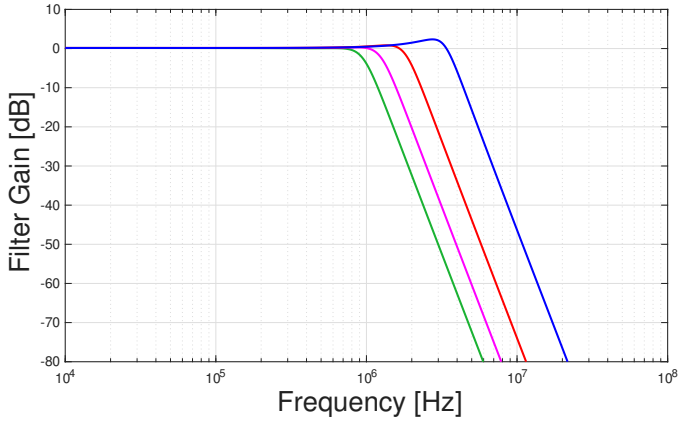
The filter is the final component inside the receiving chain, before the ADC and therefore the signal digitization. The filter reduces the bandwidth of the signal directed toward the ADC to respect the Nyquist criterion and to

minimize the out-of-band noise.

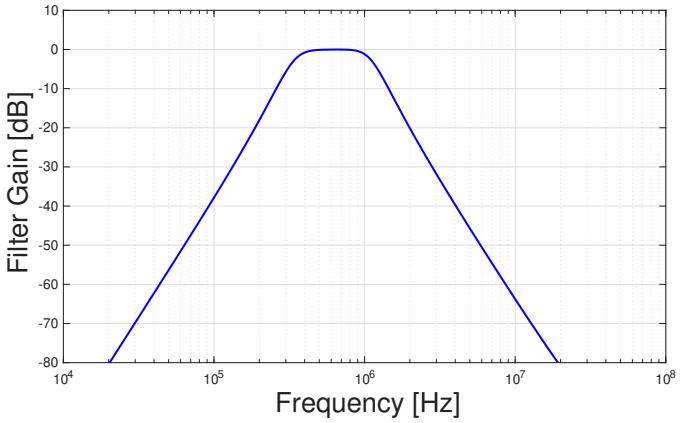
To increase the versatility of the ASIC, the filter is designed to have a programmable transfer function. Specifically, 4 bits are allocated to change the filter response: 2 bits are dedicated to select the filter type, and 2 bits are dedicated to select the filter bandwidth.
The possible filter types are: low-pass filters of the third and fifth order, third-order band-pass filters, and the option to bypass the filter. For bandwidth selection, the cutoff frequencies available are: 1 MHz, 1.3 MHz, 2 MHz, and 4 MHz. The bandwidth selection affects only the low-pass filter types. While for the band-pass filter, the -3 dB bandwidth is located between 330 kHz and 1.13 MHz. The Fig.4.7 depicts the filter frequency response for the different configurations.



(a) Third order Low Pass filter frequency response



(b) Fifth order Low Pass filter frequency response



(c) Band Pass filter frequency response

Figure 4.7: Filter frequency response for the three topology configurations, each with its possible cutoff frequencies.

4.5 ADC coupling

The ADC is supplied at 1.2 V while the previous elements in the receiving chain are supplied at 3 V.

The output dynamic range of the filter is between 0 V and 3 V, while the input dynamic range of the ADC is between 0 V and 1.2 V. Therefore, the filter cannot be directly connected to the SAR; otherwise, the signal will saturate the digital converter inputs. To address this issue, a buffer with a gain of $\frac{2}{5}$ has been added at the input of the ADC, to resize the input signal to the correct range. The input buffer is shown in Fig.4.8.

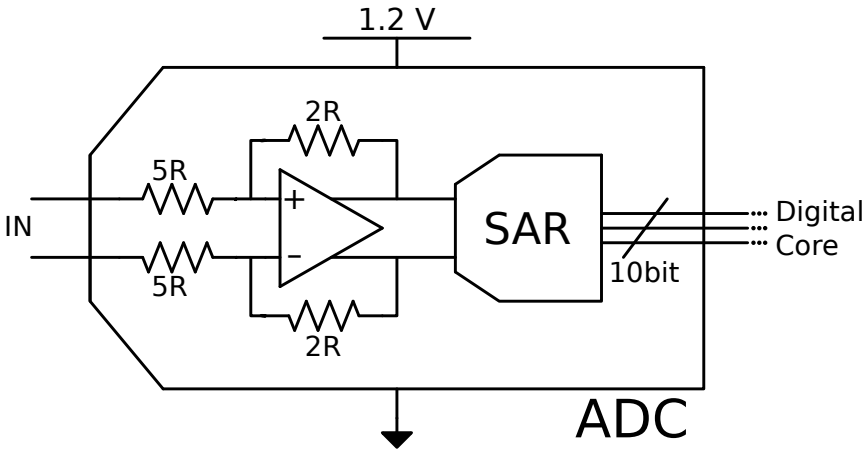


Figure 4.8: Depict the filter to ADC coupling buffer.

Chapter 5

Conclusion

This thesis describes the design of the driving ASIC for a PMUT matrix, used for an ultrasonic in-air rangefinder with beamforming capabilities.

Initially, the transducer used for the final sensor has been characterized, analyzing the features that influenced the design of the integrated circuit. Specifically, the analysis shows that the PMUT requires polarization to maximize the two-way sensitivity. The optimal solution identified is to apply a bias voltage of -20 V to the negative terminal of the membranes, while the positive terminal is connected to the ASIC.

During the analysis, it is observed that the membrane exhibits a narrow resonance band and is highly susceptible to phase and frequency errors, between the driving pulses and the membrane's natural oscillation. At the same time, it requires a sufficient number of driving pulses to maximize the transmitted power. As a compromise between these requirements, the selected driving pattern includes three square pulses to increase the output power while minimizing phase error accumulation. The low number of pulses also serves to maintain a sufficiently high longitudinal accuracy.
The driving pattern consists of three square pulses, with a duty cycle of 50% and a period of 1.66 μs selected to match the PMUT's 600 KHz resonance frequency. To perform the beamforming of the output wave, the driving pattern is sent to each membrane with the appropriate delay.

The issue of ringing, caused by the high Q factor of the transducer has also been analyzed. Two methods have been introduced to attenuate the residual oscillation of the membrane: active damping and passive damping. The first method is more effective but carries the risk of re-exciting the PMUT oscillation, while the second method requires more time to significantly attenuate the vibration but does not re-excite the transducer under any circumstances. The best solution found is therefore to combine the two approaches.

The designed driving ASIC features 25 channels to individually interface with each element inside the 5x5 matrix of the transducer. Every channel

integrates a pulser capable of providing pulses with an amplitude of up to 20 V to the connected membrane, with rising and falling edges lasting 23 ns (10% to 90%).

To achieve this amplitude of the driving pulses, the transmission elements require a level shifter to properly drive the high-side transistor of the pulser. After a careful comparison of different level shifter topologies, the capacitive floating architecture has been selected as the most suitable for the integrated circuit requirements in terms of power consumption, area usage, and noise immunity.

In the design of the T/R switch, the charge injected by the switches during the transition between the transmission and reception phases was considered. If not properly handled, this charge could re-excite the PMUT oscillation and saturate the LNA. To address this issue, several precautions were implemented, the main one being the subdivision of the switches into stages.

The ASIC incorporates an LNA for each channel with a programmable gain ranging from 14 dB to 36 dB. Additionally, it includes the TGC, which increases the gain by up to 3 dB during the reception phase, to compensate for the attenuation experienced by the sound wave over time.

Afterward, the transducer membranes are grouped into five macro-groups, and routed to the five possible reception channels. These channels consist of a PGA with a variable gain ranging from -6 dB to 36 dB, a programmable filter with configurable cut off frequency and four possible topologies: third-order low-pass, fifth-order low-pass, band-pass, or the possibility to bypass the filter. At the end of the chain, there is the SAR ADC with a resolution of 10 bits.

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