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MASTER'S DEGREE IN ELECTRONIC ENGINEERING

MASTER'S THESIS

Design Of a Low-Power Low-Noise Amplifier for Ultrasound Medical Imaging

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Abstract

This thesis is part of the PROUD project, conducted in collaboration with the medical imaging team at STMicroelectronics. The objective of this work is to assess the feasibility of a low-noise amplifier (LNA) with a noise level of 4 nV/$\sqrt{Hz}$, consuming only 10 mW of power, while maintaining a high input signal dynamic range of 360 mV, a broad bandwidth, and low harmonic distortion. The intended application is the reception of ultrasound waves for medical imaging, with the LNA designed for integration into a portable, battery-powered device.

The design process began with an analysis of different architectures to evaluate noise performance and power consumption. Subsequently, the amplifier topology and MOSFET characteristics were optimized to meet the specified requirements. Finally, a comparative analysis was conducted to determine the optimal LNA that best satisfies the design specifications.

Summary

List of Figures

List of Tables

Chapter 1

Introduction

Ultrasound, also referred to as sonography or ultrasonography, is a non-invasive imaging modality that utilizes high-frequency acoustic waves to generate real-time images or videos of internal organs and soft tissues, including blood vessels. Unlike X-ray imaging, ultrasound does not rely on ionizing radiation, making it a safer alternative for various diagnostic applications. Although it is widely associated with obstetric imaging, ultrasound is extensively used across multiple medical fields to examine different anatomical structures. The fundamental principle of ultrasonography is based on the transmission and reception of acoustic waves within the ultrasonic frequency range. Audible sound waves, perceptible to the human ear, have frequencies below 25 kHz, whereas ultrasound waves typically range between 1 MHz and 20 MHz. Lower frequencies enable deeper tissue penetration, making them suitable for abdominal imaging, while higher frequencies enhance spatial resolution and are preferred for superficial structures such as vascular imaging. Ultrasound waves are generated by the mechanical oscillations of a transducer, which is excited through electrical pulses based on the piezoelectric effect. As these waves propagate through biological tissues, their velocity varies depending on the medium's composition. However, most ultrasound imaging systems assume a uniform propagation speed of approximately 1540 m/s for all tissue types, introducing only a minor and generally negligible error.

As the ultrasound beam traverses biological tissues, it experiences attenuation, primarily of an exponential nature, which is influenced by the acoustic properties of the medium. This attenuation factor must be considered in imaging applications to ensure optimal signal processing and accurate diagnostic interpretation. The equa-

tion representing the amplitude of a plane wave propagating through the medium along the z direction is defined as:

$$A = A_0 e^{-\alpha z} \tag{1.1}$$

where
A : Amplitude of the wave attenuated after traveling a distance z from the initial position;
A_0 : Initial amplitude of the wave;
α : attenuation coefficient;

The higher the attenuation coefficient, the more wave energy is lost within the body. Analyzing the received signal, we can see the exponential decay variations in order to establish where tissues interface are, so we can get an image of the body part crossed by the ultrasound wave.

1.1 Ultrasound Transducers

In an ultrasound imaging system, the transducer plays a fundamental role in both transmitting acoustic waves into the body and detecting the returning echo signals. The depth of an echo's origin can be inferred from its time of arrival, while lateral resolution is achieved through beamforming. To facilitate this process, ultrasound transducers are typically divided into an array of elements. For two-dimensional (2D) imaging, one-dimensional (1D) arrays (linear or phased) are employed, incorporating up to 256 elements. In contrast, three-dimensional (3D) imaging without mechanical translation or rotation necessitates the use of a two-dimensional (2D) array, also referred to as a matrix transducer, which may consist of thousands of elements. The aperture of the array directly influences the field of view and spatial resolution, whereas the element pitch is determined by beamforming constraints, particularly the need to suppress grating lobes. In phased-array transducers, this requirement dictates that the element pitch should be approximately half the wavelength. Figure 1 shows a schematic representation of the transducers. Currently, the majority of ultrasound probes rely on bulk piezoelectric transducers (Fig. 1a). These transducers employ a piezoelectric layer (typically composed of piezoceramic materials such as lead zirconate titanate (PZT) or piezocompos-

ites) which is mechanically diced into discrete elements and equipped with top and bottom electrodes. The application of an alternating current (AC) voltage across these electrodes induces pressure waves through the piezoelectric effect, whereas incident pressure waves result in charge displacement or voltage changes, enabling signal detection. Structurally, the transducer functions as a thickness-mode resonator, tuned to the desired frequency range with a low quality factor to allow short pulse transmission. To ensure efficient acoustic coupling despite impedance mismatches between materials, backing and matching layers are incorporated. However, the fabrication of bulk piezoelectric transducer arrays (particularly in 2D configurations) is complex, time-intensive, and costly. To mitigate these manufacturing challenges, wafer-scale batch-fabrication techniques have been extensively explored. This has led to the development of micro-machined ultrasound transducers (MUTs), which employ a thin, flexible membrane fabricated using either surface or bulk micro-machining processes. In the case of piezoelectric MUTs (PMUTs), a thin piezoelectric film with electrodes is deposited onto

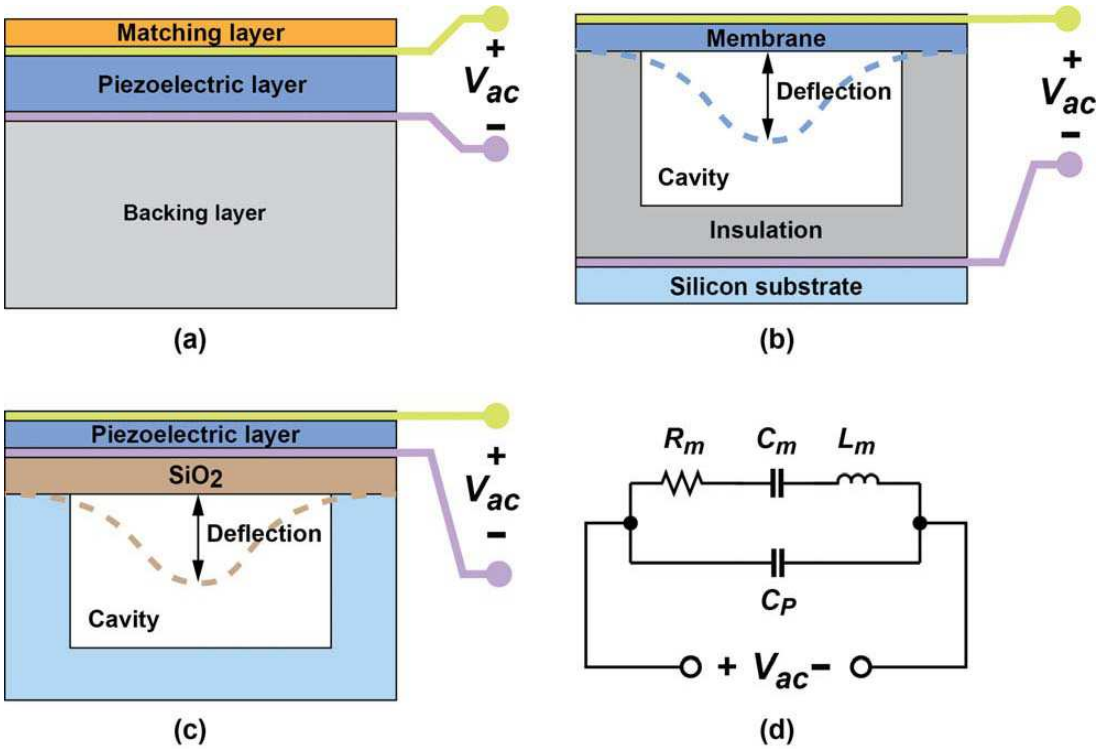

Figure 1: Schematic representation of (a) a bulk piezoelectric transducer, (b) a capacitive micromachine ultrasound transducer (CMUT), (c) a piezoelectric micromachined ultrasound transducer (PMUT), and (d) the Butterworth-Van Dyke equivalent circuit model. [1]

the membrane (Fig. 1c), while capacitive MUTs (CMUTs) utilize electrostatic actuation via electrodes positioned on both the membrane and the underlying substrate (Fig. 1b). Typically, a high direct current (DC) bias voltage is applied to pre-deflect the membrane, thereby linearizing its response. A superimposed AC voltage facilitates ultrasound wave transmission, while reception relies on detecting charge displacement due to capacitance variations associated with membrane deflection. Despite their differing operational principles, the electrical impedance of all three transducer types—bulk piezoelectric, PMUTs, and CMUTs—can be approximated using a first-order Butterworth-Van Dyke (BVD) model (Fig. 1d). This equivalent circuit includes a resonant branch, comprising resistance (R_m), inductance (L_m), and capacitance (C_m), to represent the mechanical resonance of the transducer, while an additional capacitor (C_p) accounts for its intrinsic electrical capacitance. The BVD model proves valuable in characterizing the transducer's load at the output of a transmission circuit, as well as in small-signal modelling at the input of a low-noise amplifier (LNA), where an acoustic source can be introduced into the resonant branch and the thermal noise associated with R_m represents the transducer's intrinsic noise contribution. For more accurate acoustic modelling, a two-port representation is often adopted [1].

1.2 Ultrasound System

Figure 2 shows the block diagram of a Ultrasound Imaging systems. The block are described as follows[2]:

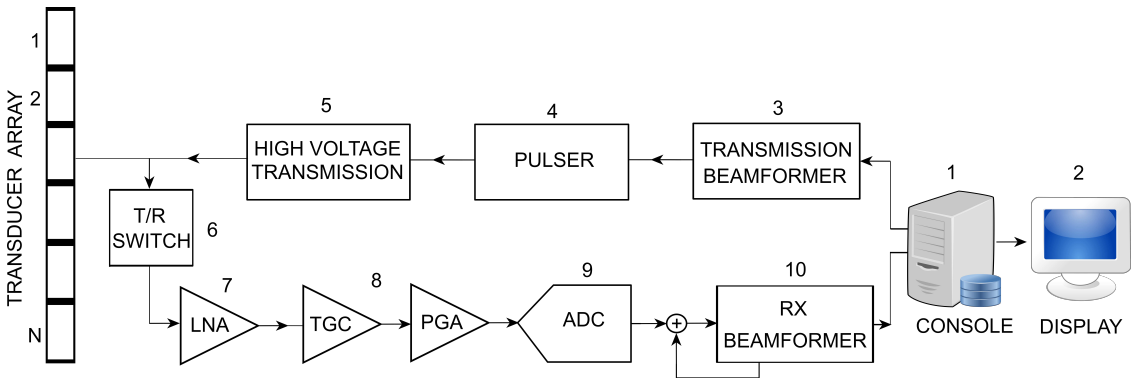

Figure 2: Block diagram of a standard Ultrasound Imaging System. [2]

1. The console is employed to perform initial digital processing and filtering of the ADC output data from all channels. This system manages the receive beamforming process, which is essential for modern phased-array probes, where transducers are activated with specific time delays during transmission.

2. The display shows the images made by the Console.

3. The TX beamformer is a digital block that transmit multiple TX channels simultaneously and coherently to achieve longer range in the main focused field of view.

4. The N Pulsers are Low Voltage (LV) circuits that control the High Voltage (HV) Trasmission blocks and that generate different pulses configuration.

5. They are typically composed of high-voltage devices. Additionally, HV switching matrices may be placed after this stage to direct the same signal to multiple transducers.

6. The N T/R switches are essential for protecting the low-voltage (LV) receiver chain during transmission mode, as both the transmitter and receiver chains are connected to the probe. During the transmission phase, the transducers are driven by high-voltage signals, which could severely damage the LV receiving circuitry if they were to reach it. To prevent this, the T/R switch disconnects the receiver chain from the transducers during transmission. At the onset of the receiving phase, the T/R switches restore the connection between the probe elements and the receiver circuitry.

7. The N Low Noise Amplifiers (LNAs) are responsible for receiving the echoes emitted by the transducer array and amplifying them with the goal of achieving the highest possible signal quality. These amplifiers are designed to operate with the lowest possible noise levels, ensuring that the amplified signal remains as clean and accurate as possible for subsequent processing. The primary function of the LNAs is to enhance the weak signals from the transducers without introducing significant noise, which is crucial for maintaining the integrity of the received data.

8. The N Time Gain Control (TGC) and Programmable Gain Amplifier (PGA) blocks are responsible for conditioning the received signal by compressing its

dynamic range, which in turn alleviates the requirements for the subsequent Analog-to-Digital Conversion (ADC) stage. Specifically, the TGCs help mitigate the attenuation effect that occurs as the signal propagates through the tissues. These blocks implement an amplification process that increases exponentially over time, effectively compensating for the loss of signal strength and ensuring the signal remains adequately amplified for accurate processing.

9. The N Analog to Digital Converters (ADC) receive the output coming from the PGA and convert into digital signals.

10. The RX Beamformer block combines the digital signals received from the ADCs to reconstruct the image, subsequently transmitting the processed signals to the Console for further display and analysis.

These block can be categorized into three groups

- The blocks from 4 to 8 represent the Analog Front End (AFE).
- The blocks 3, 9 and 10 represent the Beamformer and digital Front end.
- The blocks 1 and 2 represent the Backend.

The connection between the machine and the probe is established through multiple coaxial cables, with each transducer having a dedicated cable. Due to the one-to-one association between the transducer elements, cables, and transceiver channels, the total number of elements is constrained by practical limitations related to cable count. This restriction hinders the use of matrix transducers, which are essential for 3D imaging. Consequently, a key motivation for integrating ASICs into ultrasound probes is to overcome this limitation by bridging the gap between the high number of transducer elements required for 3D imaging and the restricted number of system channels available. Beyond merely reducing the number of channels, in-probe ASICs can offer significantly enhanced functionality. For example, they can enable full digitization and advanced processing of echo signals. This capability is particularly crucial in portable ultrasound probes, where the traditional imaging system—comprising analog front-ends and ADCs—has been replaced by a smartphone or tablet. As a result, the data acquisition function, which was historically implemented within the imaging system, is now integrated into the ASIC, while image processing is handled through software.

Chapter 2

Architecture Analysis

In ultrasound systems, the Low-Noise Amplifier (LNA) can be implemented in various ways to comply with different transducers and applications. For instance, when using traditional piezoelectric transducers (PZT), which exhibit a high output impedance (on the order of hundreds of kΩ/MΩ), the LNA must have a high input impedance to prevent loading the transducer [3]. Therefore, the recommended configuration is a common-source amplifier with high input impedance (Fig. 3a), combined with a buffer stage to enhance linearity and therefore reduce distortion. When CMUT transducers are used, they exhibit an output impedance characterized by a relatively small capacitance (on the order of a few pF) and generate an output signal in the form of a current. Since an ultrasonic transducer produces a current

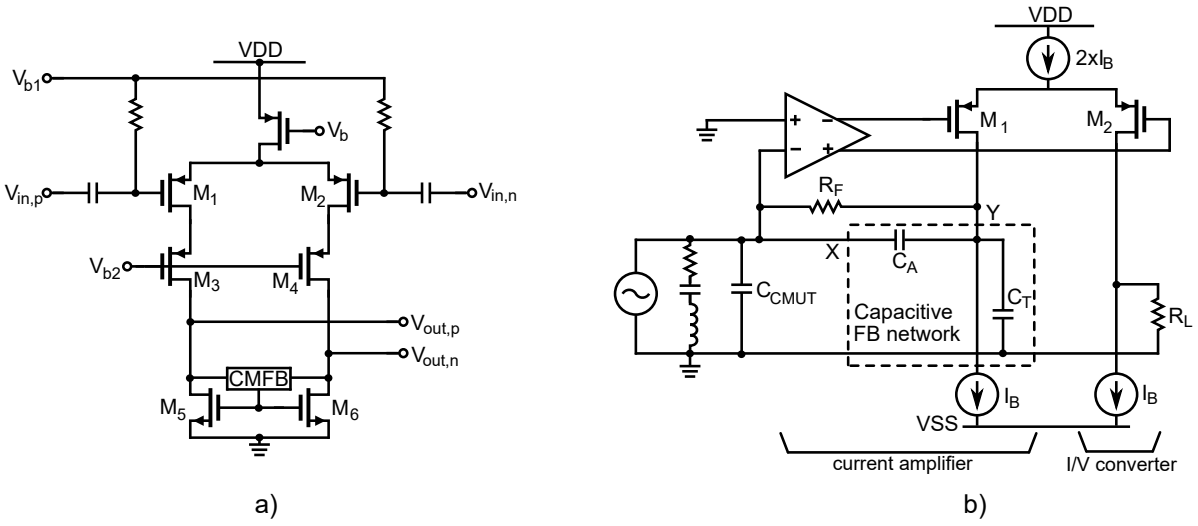

Figure 3: Schematic of: a) Common-Source Amplifier for PZT[3], b)TIA for CMUT[6].

signal in response to incident ultrasonic waves, the LNA can be implemented as a charge-based amplifier [4][5], or a transimpedance amplifier (TIA) [6]. Among these configurations, the TIA is the most widely adopted choice in ultrasound systems employing CMUT transducers, as it enables an efficient current-to-voltage conversion (Fig. 3b). Furthermore, this architecture is extensively utilized in other advanced applications, including biosensing and blood pressure monitoring via photoplethysmography [7][8][9].

When PMUT transducers are used, they exhibit a moderate impedance (on the order of a few kΩ); therefore, the circuit must be designed to ensure proper impedance matching with the receiver. The LNA can be implemented as a voltage amplifier, since it generates an output voltage (unlike CMUT transducers, which produce a current output), or alternatively, as a transimpedance stage. In the presence of a large output capacitance (Cp), as is the case with PMUTs, the voltage amplifier is significantly more power-efficient. Specifically, when employing a transimpedance stage, achieving the required bandwidth and noise specifications in the presence of a high Cp necessitates an impractically high input transistor transconductance, leading to increased power consumption. Conversely, this limitation does not apply to the voltage amplifier, whose noise and bandwidth performance, to a first approximation, remain unaffected by Cp [10].

In this work, the selected transducer type is the PMUT, since the PMUT array shows great promise for portable and implantable imaging applications, owing to their low sinusoidal input (10 V) in contrast to CMUT which requires high DC bias voltage ($>$ 100 V)[11]. The chosen configuration for the LNA design is the Voltage Amplifier, as it provides a suitable trade-off between noise performance and bandwidth. The following section will discuss the design specifications.

2.1 Design Specifications

Table 2.1 presents the required performance that the LNA requires. The reason why an input noise of 4 nV/$\sqrt{Hz}$ is required is multifaceted. The first reason is that the ultrasonic echoes received by the transducer are generally weak, especially those originating from deep structures within the body. A low-noise amplifier helps prevent the degradation of the SNR (signal-to-noise ratio) of the useful signal. The second reason is that a low-noise amplifier enables the detection of low-amplitude

signals that would otherwise be masked by electronic noise, thereby improving the resolution of image details. Furthermore, excessive noise introduced by the LNA can cause distortions and artifacts in the images, reducing diagnostic reliability.
The maximum amplitude of the signal from the transducer is 0.36 V; therefore, the amplifier must handle such a high-amplitude signal while maintaining second- and third-order harmonic distortion below -50 dB. Minimizing harmonic distortion is crucial, as it helps preserve signal integrity. If the LNA introduces harmonic distortion, phase and amplitude information will become unreliable, compromising the quality of signal reconstruction.
The LNA gain can be selected by the user among 15 dB, 18 dB, and 21 dB, depending on the operating frequency and the distance of the tissues from the probe. For deeper tissues, higher gain is required, and vice versa. The LNA bandwidth must cover the ultrasonic frequency range, which varies from 1 MHz to 15–20 MHz, depending on the application. Since the system must be portable and battery-powered, the LNA power consumption should not exceed 10 mW per channel.
Once the design specifications have been defined, a detailed analysis of various circuit architectures suitable for the implementation of the low-noise amplifier (LNA) will be carried out. In particular, the non-inverting amplifier, the fully differential amplifier, and the inverter-based amplifier will be examined, with the aim of evaluating their performance in terms of noise, linearity and power consumption.

Parameter	UNIT	VALUE
Equivalent voltage input noise(@3MHz)	nV/$\sqrt{Hz}$	4
LNA Gain (Selectable)	dB	15 18 21
Bandwidth (-3dB cutoff)	MHz	0.1 to 20
Input max voltage range	mVpp	710 @15dB 500 @18dB 360 @21dB
HD2 (@5MHz)	dB	-50
HD3 (@5MHz)	dB	-50
Power consumption	mW	10

Table 2.1: Design specifications.

2.2 Non-Inverting Amplifier

A non-inverting amplifier (Fig.4) is one of the most commonly used configurations for Low-Noise Amplifiers (LNA) in signal acquisition systems, including ultrasound imaging systems. This configuration is particularly valued for its high input impedance, good voltage gain, and low sensitivity to variations in component parameters. The fundamental architecture of a non-inverting LNA consists of:

- An Operational Amplifier (or Operational Transimpedance Amplifier(OTA));
- Feedback capacitors (C_{in}, C_f) to define the gain. A resistive feedback network can also used, but capacitive feedback is preferred to minimize thermal noise introduced by the resistance;
- The resistor R_f, which serves as a feedback element to set the common-mode voltage V_{CM} of the signal chain at the output node.

The voltage gain is given by:

$$A_v(s) = \frac{V_{out}}{V_{in}} = 1 + \frac{sC_{in}R_f}{1 + sC_fR_f} \tag{2.1}$$

Thanks to its high input impedance, this configuration allows the amplification of signals from ultrasonic transducers without excessively loading the sensor, thereby reducing signal loss and improving detection quality. Moreover, it enables gain adjustment, optimizing the signal level according to system requirements. However, an excessively high gain can lead to stability issues and increased noise. The input-

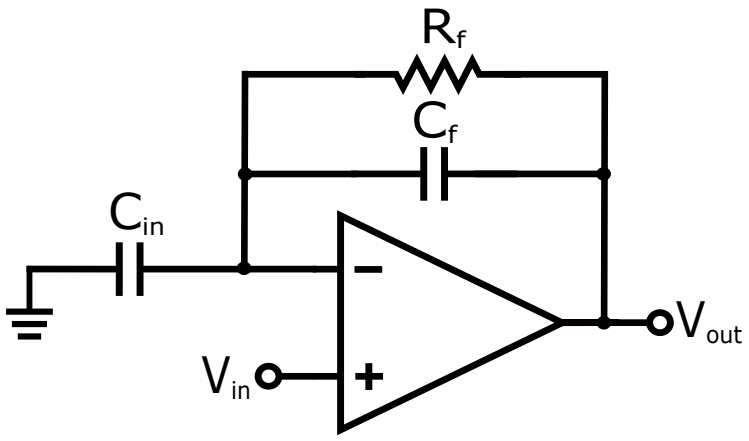

Figure 4: Non-Inverting Amplifier.

referred noise (V_n) of an operational amplifier depends on its internal architecture and components.

The LNA presented in [2], whose block diagram is shown in Figure 5, is implemented as a Voltage Amplifier (VA) with high input impedance. Its performance in terms of noise and bandwidth is, to a first approximation, independent of the output capacitance of the MUT (C_p). Similarly, the gain of the VA with capacitive feedback, determined by the ratio of C_2 to C_1 for the first stage and C_3 to C_4 for the second stage, is not affected by C_p. The input noise level was determined by imposing the condition SNR $\geq$ 0 dB within the bandwidth of the PMUT, ensuring adequate image quality. The SNR was calculated by integrating the power spectral density over the -3 dB bandwidth of the PMUT (ranging from 2 to 4 MHz in this case), yielding:

$$V_n = \sqrt{\int_{2MHz}^{4MHz} V_{n,in}^2 \, df} \leq \mu_S P_{S,min} \tag{2.2}$$

where:

- $V_{n,in}^2$ represent the power spectral density of the input noise;
- μ_S denotes the PMUT RX Sensitivity;
- $P_{S,min}$ refers to the minimum detectable input pressure.

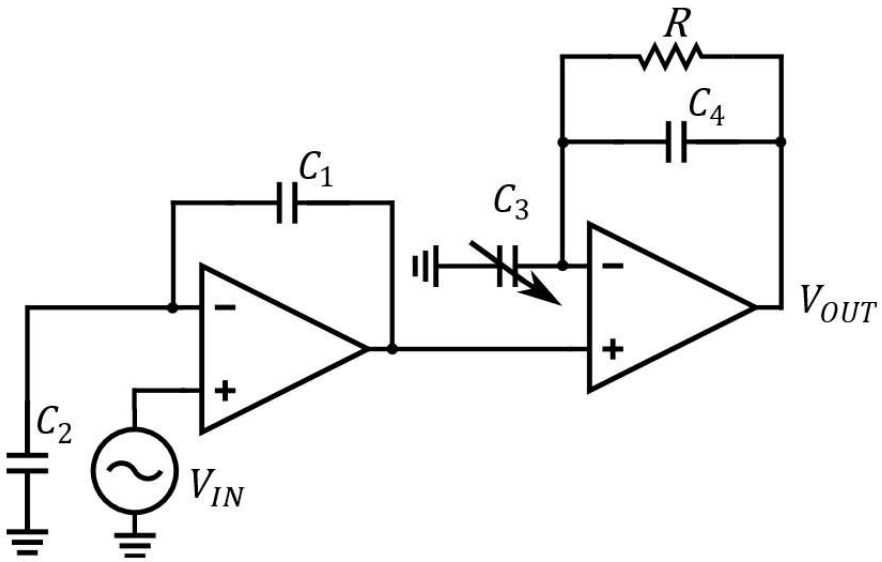

Figure 5: Block diagram of two-stage solution. [2]

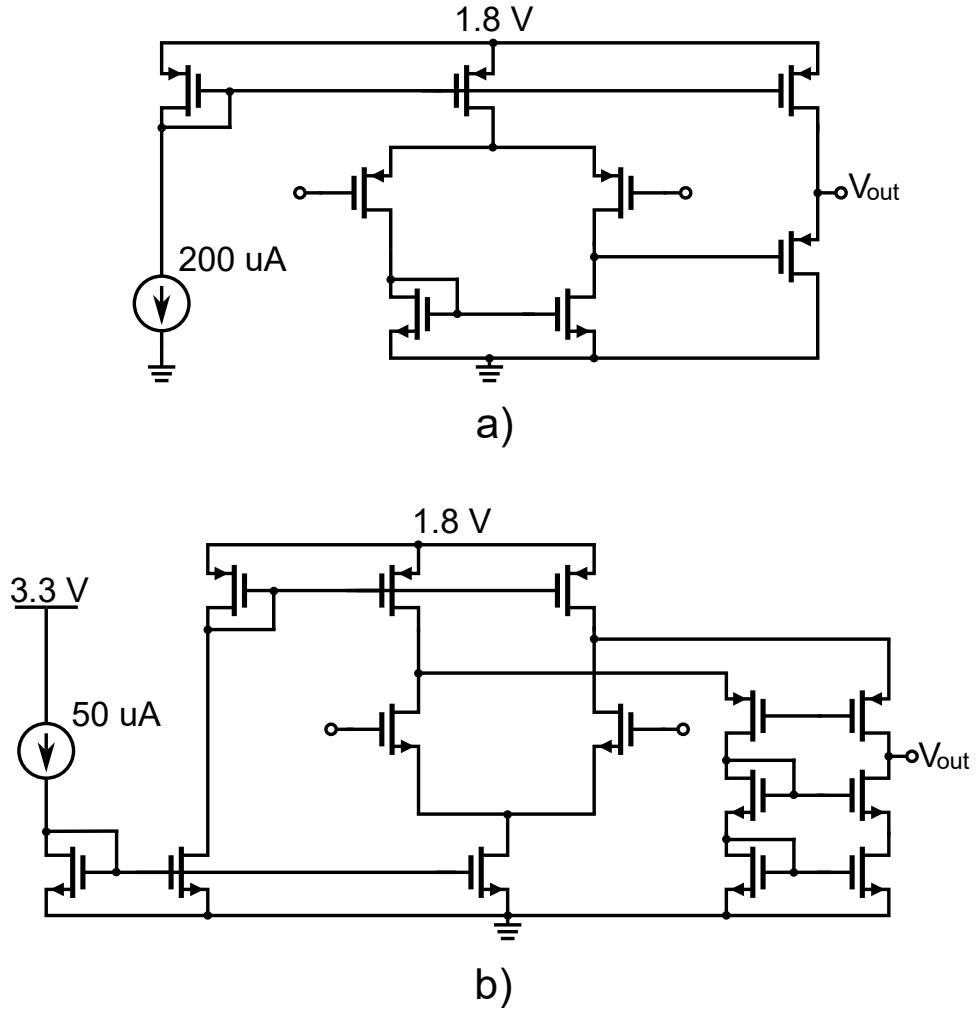

Figure 6: Schematic of two-stage solution: (a) PMOS differential pair followed by a level shifter, (b) Folded cascode Op-Amp with an NMOS input pair. [2]

The gain of the two-stage LNA can be adjusted by configuring the capacitance C_3, as shown in Fig. 5. The operational amplifier used in the first stage consists of a PMOS differential pair followed by a level shifter (Fig. 6a), while the second stage is implemented as a folded cascode operational amplifier with an NMOS input pair (Fig. 6b). The first stage accounts for the majority of the noise contribution in the signal chain, as the noise from the second stage is attenuated by the sufficiently high gain provided by the first stage. Moreover, within the frequency range considered in this work, the thermal noise of the MOSFETs can be made dominant with respect to 1/f noise contributions by carefully selecting the amplifier configuration and optimizing the transistor sizing.

An alternative is presented in [12], where, instead of using two amplifiers, a single amplifiers is employed, thereby reducing power consumption (Fig. 7) The archi-

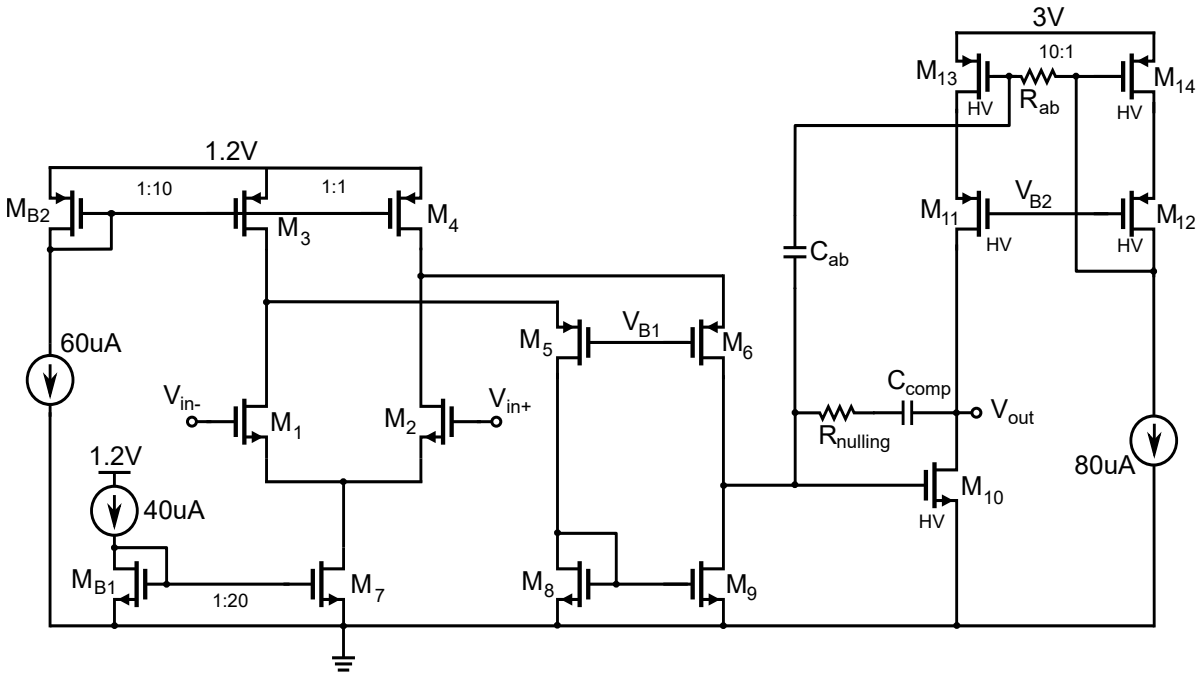

Figure 7: Folded cascode input stage followed by Class-AB output stage. [12]

tecture consists of a folded cascode amplifier followed by a Class AB output stage, implemented using high-voltage transistors. This design choice is particularly advantageous as it enables a high gain, a good frequency response, low distortion, and high power efficiency. The adoption of the Class AB stage further enhances energy efficiency, making this configuration particularly suitable for battery-powered portable systems. Moreover, it allows for a wide signal dynamic range (output swing) and a reduction in distortion for high-amplitude signals, thereby improving the quality of ultrasonic imaging. The LNA gain is determined by the capacitive feedback. The input-referred noise was obtained by integrating the power spectral density over the PMUT bandwidth, assuming that the gain of the folded cascode stage is significantly higher than that of the Class AB stage. Consequently, the folded cascode can be considered the dominant noise-contributing stage, leading to an approximate input noise given by:

$$v_n \approx \sqrt{\int_{BW} v_{eq,in}^2 \, df} \approx \sqrt{\int_{BW} \left(v_{n1}^2 + \frac{g_{m3}^2 v_{n2}^2}{g_{m1}^2} + \frac{g_{m8}^2 V_{n5}^2}{g_{m1}^2} \right) df}$$

$$\approx \left(\sqrt{\frac{4k_b T\gamma}{g_{m1}} (BW)} \right) \left(1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m8}}{g_{m1}} \right) \tag{2.3}$$

where k_b represent Boltzmann's constant, T denotes the absolute temperature and γ is the excess channel thermal noise coefficient. Given that the signal bandwidth for ultrasound applications typically exceeds several megahertz, the dominant noise contribution arises from thermal noise. The low-frequency flicker noise is neglected in the calculations. To minimize the input noise, it is possible to maximize the input transconductance g_{m1} and reduce the bandwidth. However, it is crucial to find a trade-off between these parameters, ad a high transconductance may lead to increased power consumption, while an excessively narrow bandwidth could limit the amplifier's frequency response, ultimately affecting the overall system performance.

2.3 Fully-Differential Amplifier

A fully differential Amplifier (Fig.8) provides enhanced noise rejection improved linearity, and a wider dynamic range compared to single-ended amplifiers. This configuration is particularly advantageous for weak and high-frequency signals, such as those generated by ultrasound transducers. A fully differential amplifier processes differential signals, meaning it operates with two inputs and two outputs:

- Differential input: V_{in+} and V_{in-};

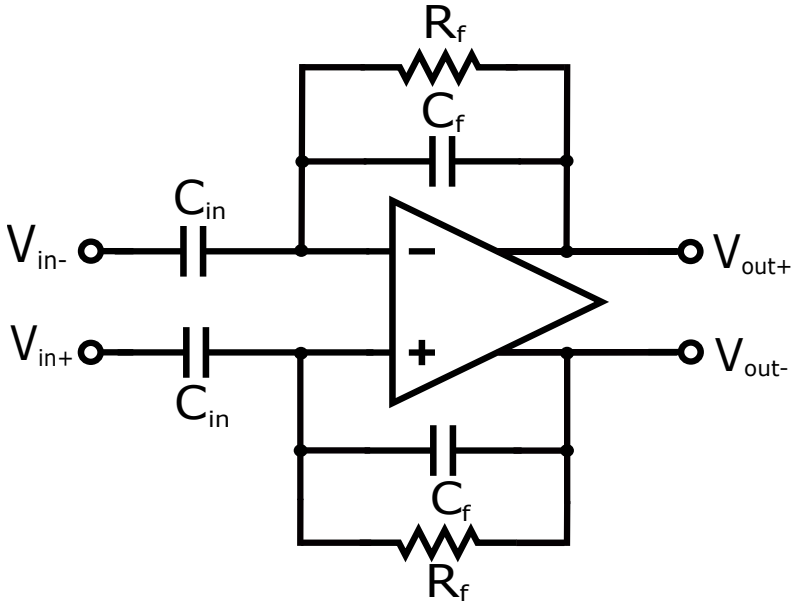

Figure 8: Fully-Differential Amplifier.

- Differential output: V_{out+} and V_{out-};
- Common-mode voltage (CM): the average of the two output voltages, which must be regulated through a Common-mode Feedback (CMFB) circuit to stabilize the operating point.

The adoption of a fully differential architecture offers several beneficts, including:

- High common-mode noise rejection (high CMRR): power supply noise, environmental interference, and crosstalk from other circuits are effectively suppressed. This is particularly crucial in ultrasound imaging, where common-mode noise can degrade the signal-to-noise ratio (SNR);
- Improved linearity and reduced harmonic distortion: second-order harmonic distortion (HD2) is significantly minimized, which is essential for preventing artifacts in ultrasound images;
- Greater dynamic range(wider output swing): given the same supply voltage (V_{DD}), a differential amplifier provides twice the dynamic range compared to a single-ended configuration;
- Better immunity to offset variations: the use of differential feedback and a Common-Mode Feedback (CMFB) circuit helps maintain symmetry between the two branches of the amplifier, improving overall stability;
- Compatibility with pipeline ADCs and digital circuits: many high-speed analog-to-digital converters (ADCs) require differential inputs. A fully differential LNA eliminates the need for additional conversion stages, simplifying system integration.

However, using a fully differential amplifier also presents some challenges:

- Increased circuit complexity: a fully differential amplifier requires a more intricate biasing network than a single-ended configuration, as well as a balanced pair of transistors and symmetric components to ensure optimal operation;
- Higher power consumption: in general, a fully differential amplifier draws more current than a single-ended counterpart, as it powers two active branches instead of one. This can be a significant drawback in battery-powered portable systems, where energy efficiency is a critical parameter;

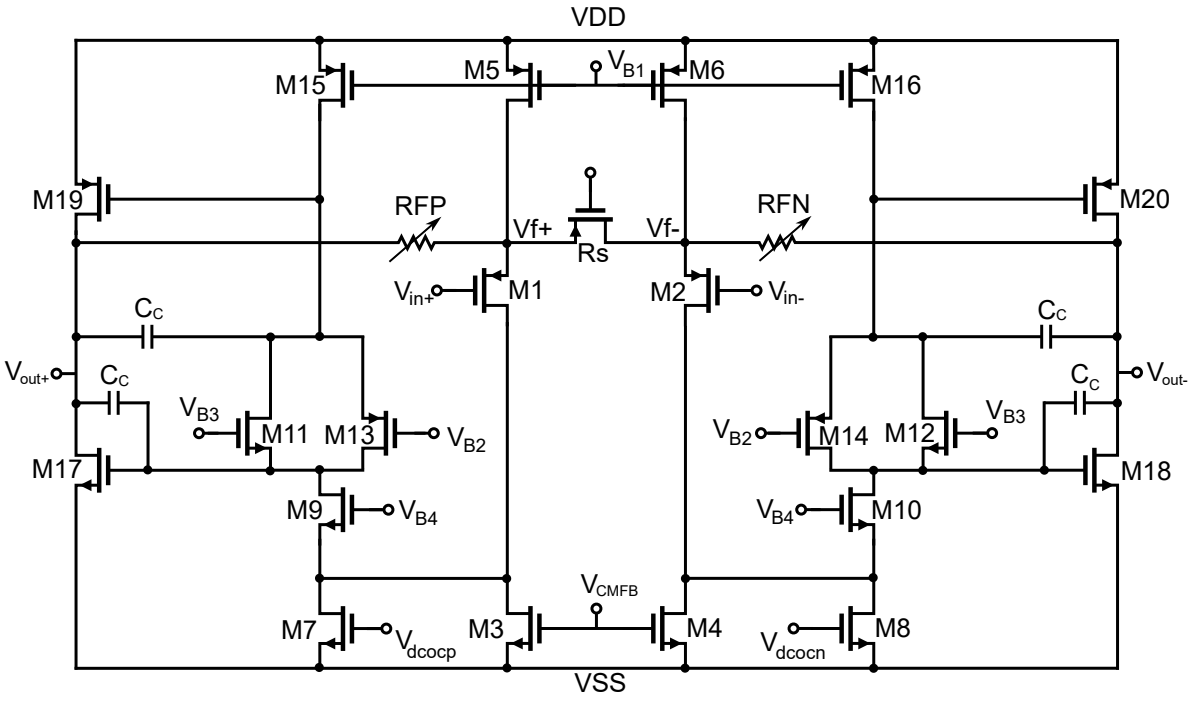

Figure 9: Fully-Differential Amplifier: first stage is a common gate common source (CGCS) circuit with source resistance feedback followed by Class-AB stage. [13]

- More complex PCB layout design: to maintain symmetry between the two branches of the differential signal, a more meticulous PCB design is required;
- Potential mismatch issues: Any discrepancies between the two branches can introduce voltage offsets and degrade overall circuit performance.

The structure presented in [13] employs a fully differential amplifier with feedback resistances RFP and RFN. The fist stage consist of a common-gate common-source (CGCS) circuit with source resistance feedback (Fig. 9), ensuring a sufficiently high open-loop gain. The transistors in the input pair of the common-source amplifier can be regarded as a combination of a voltage amplifier, which amplifies the input signal, and a current amplifier, which amplifies the feedback signal, as illustrated in the figure. Furthermore, the common-gate amplifier in the CGCS stage enhances the difference between the input and feedback signals. The second stage is a class AB amplifier, which serves as an output stage to improve the overall linearity of the system. The voltage gain A_v of the fully differential amplifier is determined by the ratio of the feedback resistances to the source resistance R_s. The open-loop gain is primarly provided by the CGCS amplifier in the first stage,

while the contribution from the second-stage class-AB amplifier remains relatively low. As a result, the noise generated by the first stage is the dominant component in the system's overall noise performance. In cases where the output stage noise can be neglected, the Input-Referred Noise (IRN) of the LNA or PGA can be approximated by the following expression:

$$\overline{v_{in,eq}^2} \approx 2(\frac{1}{g_{m1}})^2[4k_bT\gamma(g_{m1}+g_{m3}) + \frac{K_f}{C_{OX}WL}\frac{1}{f}(g_{m1}^2+g_{m3}^2)] \tag{2.4}$$

where K_f represent the flicker noise coefficient, C_{OX} is the gate-oxide capacitance per unit area, f denotes the flicker noise frequency, W and L correspond to the MOSFET's width and length, respectively, while g_{m1} and g_{m3} denote the transconductances of transistor M_1 and M_3, respectively. From equation 2.4, it can be observed that achieving low noise requires a high g_{m1}. However, increasing g_{m1} leads to a higher gain-bandwidth product (GBW). which is essential for the amplifier given the bandwidth requirements for high-frequency ultrasound signals. Furthermore, g_{m1} is directly related to the DC current, resulting in increased power consumption. Consequently, the LNA implemented with a fully differential amplifier exhibits a relatively high power consumption, primarily attributed to the CMFB circuit and the necessity of duplicating the passive network. This may exceed the specified design constraints for power consumption.

2.4 Inverter-based Amplifier

Inverter-based amplifiers employ CMOS inverters as gain stages, as an alternative to traditional operational amplifiers based on differential pairs (Fig. 10). This architectural choice offers significant advantages in terms of energy efficiency and chip area reduction, owing to the simplicity of the circuit. However, this configuration also presents certain limitations, including a lower gain compared to multi-stage operational amplifiers and higher harmonic distortion, primarily due to the absence of strong negative feedback. This latter aspect is particularly critical in ultrasound imaging applications, where signal quality is of utmost importance. Additionally, the biasing stability is sensitive to variations in the manufacturing process, supply voltage, and temperature (PVT), necessitating compensation strategies to ensure reliable operation. The use of an inverter-based Low-Noise

Amplifier (LNA) represents a promising solution for ultrasound receivers, as it enables power efficiency optimization and enhanced chip integration. However, the design of these amplifiers poses significant challenges, particularly in terms of bias stabilization, gain control, and robustness against PVT variations. To enhance circuit performance, a fully differential topology can be adopted, offering a higher Common-Mode Rejection Ratio (CMRR) compared to single-ended configurations, thereby improving immunity to common-mode interference. In this context, the inclusion of a Common-Mode Feedback (CMFB) circuit is essential for stabilizing the output common-mode voltage, ultimately enhancing the overall CMRR and ensuring a higher-quality amplified signal. The Input-Referred Noise (IRN), whose minimization is crucial for achieving high system sensitivity and accurate amplification of low-amplitude ultrasonic signals, is derived as follows:

$$V_{n,inv}^2 = \frac{8k_bT\gamma}{g_{m1}+g_{m3}}\left(1+\frac{g_{m5}}{g_{m1}+g_{m5}}\right) \tag{2.5}$$

Since the signal bandwidth for ultrasound applications typically exceeds several MHz, the dominant noise contribution comes from thermal noise. Low-frequency flicker noise is neglected in the calculation. To minimize the input-referred noise, M_5 can be carefully sized to reduce its noise contribution while maximizing the input transistors.

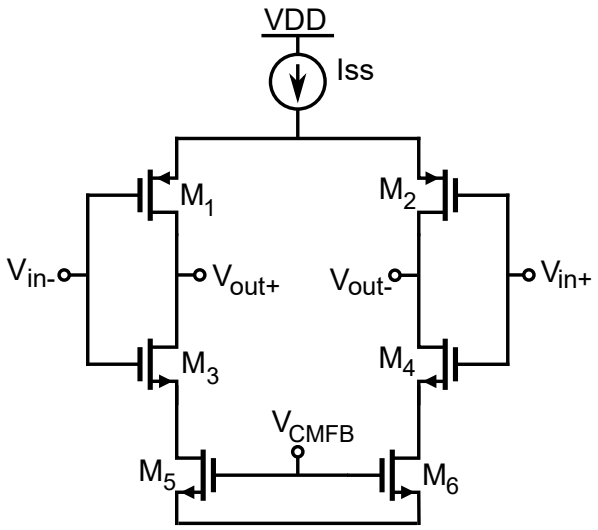

Figure 10: Fully-Differential inverter-based Amplifier. [14]

Chapter 3

LNA Design

In this chapter, the design of the low-noise amplifier (LNA) will be analyzed, with a particular focus on the single-ended configuration. This choice is driven by the need to optimize both power consumption and area, which are critical factors in the design of integrated circuits for high-performance applications.
Subsequently, the design of an inverter-based LNA will be developed and evaluated to assess its behavior concerning the project requirements. Finally, a comparison between the different configurations will be conducted to determine which one best meets the design specifications and delivers the highest overall performance.

3.1 Single-ended Voltage LNA

The most suitable solution for the single-ended amplifier is the use of a non-inverting configuration, combined with a capacitive feedback network (Fig. 11). This section presents a detailed analysis of the operation and characteristics of capacitive feedback, highlighting its advantages in terms of gain, frequency response, and overall noise performance of the system.

3.1.1 Capacitive Feedback

For this project, the optimal choice is to adopt a capacitive feedback instead of a resistive one, in order to avoid additional noise, in compliance with the design specifications. However, a feedback resistor has been introduced to close the feedback loop in DC. Since the resistor introduces thermal noise with a power spectral

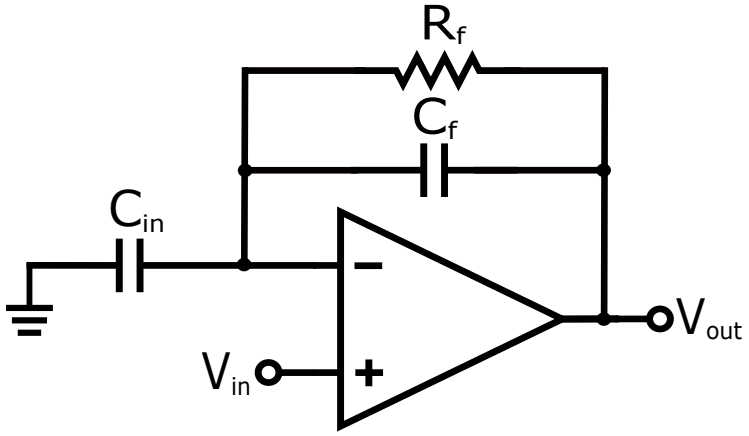

Figure 11: Single-Ended Non-Inverting Amplifier.

density of $4k_B$TR, its contribution to the total noise depends not only on its resistance value but also on the bandwidth over which this noise is integrated. By increasing the resistance, the associated RC time constant becomes larger, thus reducing the bandwidth and limiting the amount of thermal noise integrated at the output. Therefore, using a high resistance value helps to minimize the total noise contribution, although it results in increased area consumption. To make the parasitic capacitance of the input MOS transistor negligible, a feedback capacitance of C_f = 7pF has been selected. Increasing this value excessively would lead to unnecessary current consumption required for charging. According to the bandwidth specifications (see Table 2.1), the first pole of the transfer function must be lower than 100 kHz:

$$f_{p1} = \frac{1}{2\pi C_f R_f} < 100kHz$$

$$R_f > \frac{1}{2\pi C_f f_{p1}} \approx 227k\Omega \tag{3.1}$$

A capacitance of C_{in} = 32.2pF was also selected in order to achieve a gain of 5.6 (15 dB). The use of capacitive feedback offers several advantages, such as a reduction in thermal noise compared to its resistive counterpart; however, it also introduces some significant design challenges, including:

- Slew Rate and Capacitive Loading: the feedback capacitors must be charged and discharged rapidly, especially at the high frequencies required for ultrasound imaging. This increases the required slew rate and may lead to higher current consumption in the transistors to ensure fast response. Furthermore, if the transistors are not properly sized, the circuit may fail to track rapid

signal variations, thereby limiting the usable bandwidth;

- Potential Instability and Nonlinear Effects: the combination of feedback capacitance and parasitic impedances can introduce unwanted poles and zeros, affecting the stability of the amplifier. In addition, MOS capacitors may exhibit voltage-dependent capacitance, introducing nonlinear distortion that could degrade the quality of the amplified signal;

- Lack of DC Stabilization: a purely capacitive feedback does not provide a DC path, making it difficult to establish the amplifier's operating point. In particular, the design goal is to center the output at 1.25 V while biasing the gates of the input transistors at 0.9 V, in order to ensure an appropriate operating point for all transistors in the first stage.

One way to set a DC gain value is to use a resistor triangle as a feedback network, as shown in the Figure 12. By calculating the DC gain, we obtain the following expression

$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_{f1}}{R_{DC}} = 1.389$$

Obtaining:

$$R_{DC} = 2.57 R_{f1} \tag{3.2}$$

Let us now return to the single R_f branch to size the resistors in such a way that the low-frequency pole is placed below 100 kHz, thus obtaining an equivalent feed-

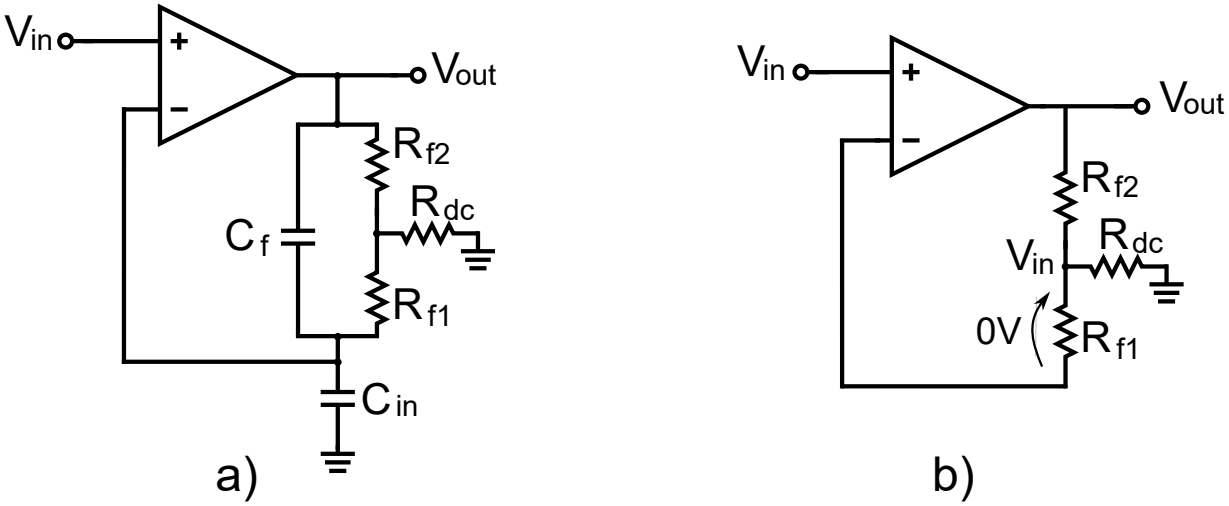

Figure 12: a) Closed-Loop configuration with T-Resistance feedback, b) Closed-loop configuration in DC since the capacitance in DC are short circuit. [12]

back resistance. The equivalence can be determined through the following calculations.

$$R_f = R_{f2} + R_{f1} || R_{DC} \tag{3.3}$$

From Eq. 3.1 to place the pole below 100kHz, R_f must be greater than 227kΩ. By arbitrarily setting $R_{f1} = R_{f2}$ and using Eq. 3.2, the DC gain can be set

$$R_f = R_{f1}(1 + 0.7) > 227k\Omega$$

$$R_{f1} = R_{f2} > 134k\Omega$$

Since a higher feedback resistance generates less noise, R_{f1}=R_{f2}=200kΩ and R_{DC}=514kΩ were selected. The equivalent R_f is therefore 344kΩ, and the low-frequency pole is located at 66 kHz. Obtaining a transfer function as follows:

$$\frac{V_{out}}{V_{in}}(s) = \left(1 + \frac{R_{f2}}{R_{dc}}\right) \frac{1 + s\left(C_f \frac{R_{dc}R_{f2}}{R_{dc}+R_{f2}} + C_{in}\frac{R_{dc}R_{f1}}{R_{dc}+R_{f1}}\right)}{1 + sC_f R_{f2}} \tag{3.4}$$

Regarding the choice of the type of capacitor to use, there are essentially two options in the employed technology: P-sub/N-well capacitors or Metal-Oxide-Metal (MOM) capacitors. The P-sub/N-well capacitor is based on the junction between the N-well and the P-SUB substrate. Its characteristics are as follows:

- High capacitance density (pF/mm^2): it allows for a relatively high capacitance per unit area;
- Compact layout: being integrated into the substrate structure, it saves space;
- Easy to implement in standard CMOS process: it does not require additional layers or masks, making it compatible with low-cost processes;
- Voltage dependence: being a PN junction, the capacitance varies with the applied voltage, which can introduce non-linearity;
- Low precision: the variation with voltage makes it difficult to achieve precise and stable values.

In contrast, regarding MOM capacitors, they are structured on a series of interdigitated fingers between multiple metallic layers, separated by a thin dielectric layer

(such as $Si0_2$). They function as an array of parallel capacitors between the metals. Their characteristics are as follows:

- High linearity: its capacitance is practically independent of the applied voltage;
- Low losses: it has significantly better insulation compared to P-SUB/N-well capacitors;
- Lower capacitance density compared to P-SUB/N-well;
- Scalability: it can be fabricated with multiple metal layers to increase capacitance;
- Technology dependence: capacitance per unit area is highly dependent on the manufacturing processes.

To ensure high linearity of the circuit, the implementation of Metal-Oxide-Metal (MOM) capacitors has been adopted. This design choice is based on the proven reliability and stability of MOM capacitors compared to other integrated solutions, particularly in their behavior under varying signals and at high operating frequencies, making them particularly suitable for use in high-performance analog circuits, such as those required in ultrasound imaging systems.
At this stage of the work, the amplifier will be implemented in order to experimentally evaluate its performance. In particular, a detailed analysis of the frequency response will be conducted, with the aim of verifying its consistency with theoretical predictions and project specifications.

3.1.2 Folded Cascode + Class-AB stage

The topology used to implement the amplifier is a folded cascode with class AB output stage. The proposed circuit is shown in Figure 13. The choice of a Folded-Cascode architecture is motivated by its high output impedance, which facilitates efficient signal transfer to the second Class-AB stage. This configuration ensures optimal interfacing between the two stages and contributes to noise reduction—an essential requirement when amplifying weak signals, as typically encountered in ultrasound imaging applications.

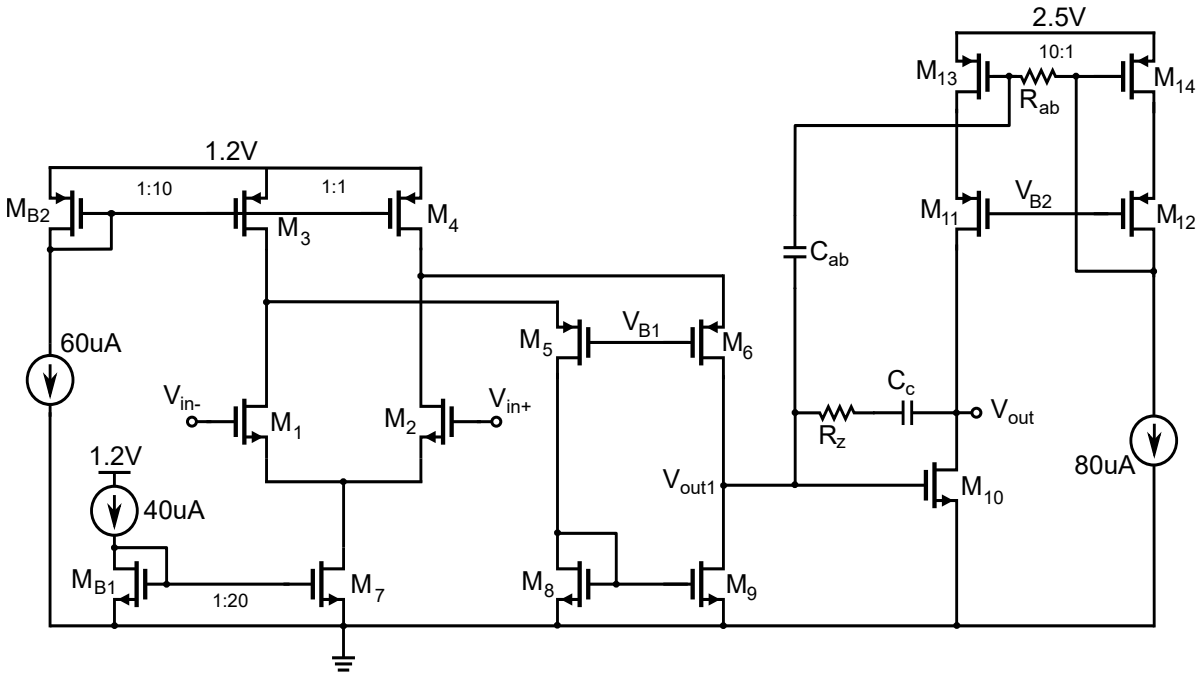

Figure 13: Schematic diagram of single-ended LNA. [12]

Another advantage of this topology lies in the possibility of decoupling the biasing of the input and output branches. This allows for the optimization of the input transconductance, maximizing it to reduce the overall noise and to fine-tune the output impedance. As a result, the circuit benefits from improved stability and reduced interference.

To limit power consumption, the MOS transistors in the first stage are designed to operate with a reduced supply voltage of 1.2 V. However, to accommodate the requirement of a 1 V peak-to-peak output swing centered at 1.25 V, the second stage operates from a higher supply voltage of 2.5 V, ensuring sufficient voltage headroom for proper transistor operation.

The Class-AB output stage is designed so that both the PMOS and NMOS devices operate in signal amplification mode. Specifically, the gate of the PMOS can follow the signal variations thanks to the capacitive coupling C_{ab} with the NMOS gate. During a positive slew rate, when the PMOS is required to supply increased current, the output voltage rises, causing a decrease in the gate voltage of the NMOS, and consequently, in the gate voltage of the PMOS as well. This mechanism holds true as long as the capacitor C_{ab} behaves as a short circuit at the signal frequency. To ensure this condition is met, C_{ab} and its associated resistor R_{ab} must be properly sized so that the resulting pole is located at least one decade below the minimun

signal frequency, which is 1MHz[12].

With regard to the open-loop gain, it must be sufficiently high in order to ensure greater accuracy of the closed-loop gain. The closed-loop gain of a feedback amplifier is given by:

$$A_{cl} = \frac{A_{ol}}{1 + A_{ol}\beta} \tag{3.5}$$

Where A_{ol} denotes the open-loop gain and β represents the feedback factor. When A_{ol} is sufficiently high, the closed-loop gaincA_{cl} becomes largely independent of variations in A_{ol} and is instead determined almost exclusively by the passive components of the feedback network.

Regarding bandwidth considerations, the goal is to amplify signals with frequencies up to at least 10 MHz. Consequently, the amplifier's bandwidth should extend at least one decade beyond the signal frequency, i.e., up to 100 MHz.

In terms of phase margin, a minimum value of 60° under typical operating conditions is desired to ensure system stability and prevent oscillations. A sufficient phase margin also improves the transient response, reducing overshoot and ringing in the impulse response.

When capacitive feedback is employed, the high-frequency behavior of the amplifier is significantly influenced by both the feedback and parasitic capacitances. This may lead to a reduction in the effective phase margin; therefore, designing for an initial phase margin of at least 60° provides a safety margin to ensure stability under real-world conditions, which may deviate from idealized simulation assumptions.

3.1.3 Frequency Response and Compensation

The small-signal equivalent circuit of the two-stage LNA (Fig. 13) can be represented by a simplified diagram, as shown in Fig. 14. Each stage is represented by a

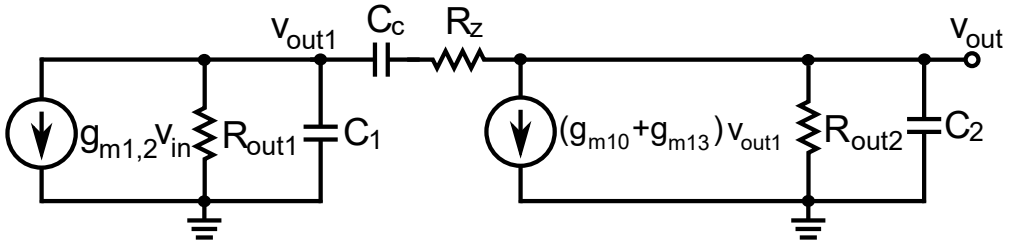

Figure 14: Small signal equivalent circuit of a the LNA.

voltage-controlled current soruce, with an output resistance and a load capacitance connected in parallel. The DC gain is given by the product of the gains A_1 and A_2:

$$A_v|_{DC} = A_1 A_2 = g_{m1,2} R_{out1} \left(g_{m10} + g_{m13}\right) R_{out2} \tag{3.6}$$

The two RC networks introduce two poles, with their respective angular frequencies given by:

$$\omega_{p1} = \frac{1}{\tau_1} \approx \frac{1}{C_c \left(g_{m10} + g_{m13}\right) R_{out2} R_{out1}} \tag{3.7}$$

$$\omega_{p2} = \frac{1}{\tau_2} \approx \frac{\left(g_{m10} + g_{m13}\right) C_c}{C_1 C_2 + \left(C_1 + C_2\right) C_c} \tag{3.8}$$

and a zero located at

$$\omega_z \approx \frac{1}{C_c \left(\frac{1}{g_{m10} + g_{m13}} - R_z\right)} \tag{3.9}$$

We know that the output resistances of the two stages are given by the parallel connection of the r_{ds}. The load capacitances result from the parasitic elements of the transistors used and, possibly, from the capacitance that charges the output. By neglecting the effect of the capacitances C_c and R_z, the two poles introduced by the two RC networks would be relatively close to each other, potentially leading the system to instability (Fig. 15). Since the circuit does not exhibit a dominant pole, it was necessary to introduce a compensation network. By using the

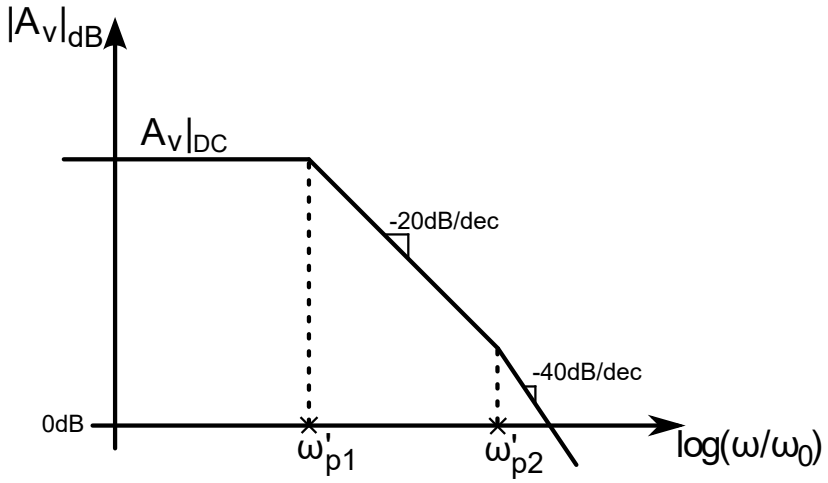

Figure 15: Bode plot of the amplifier without compensation network: the Bode plot highlights the instability of the system in the absence of a compensation network. The two poles introduced by the folded cascode input stage and the class-AB output stage are located at relatively close frequencies.

compensation capacitance C_c and the resistance R_z, it was possible to shift the first pole toward lower frequencies and, simultaneously, move the second pole toward higher frequencies, thereby improving the stability of the system. Furthermore, the resistance R_z prevents the zero introduced by the compensation capacitance from being located in the right half of the s-plane. If this zero were to be close to the unity gain frequency (ω_T), it could significantly alter the frequency response in the region around the 0 dB crossover, thereby degrading the stability conditions in terms of phase margin. Through the introduction of the compensation network, the frequency response of the amplifier can be described by the following transfer function:

$$\frac{v_{out}}{v_{in}} = A_v|_{DC} \frac{1 + s\frac{1}{C_c}\left(\frac{1}{g_{m10}+g_{m13}} - R_z\right)}{\left(1 + s\frac{1}{(g_{m10}+g_{m13})R_{out2}R_{out1}C_c}\right)\left(1 + s\frac{(g_{m10}+g_{m13})C_c}{C_1C_2+(C_1+C_2)C_c}\right)} \tag{3.10}$$

This expression allows for an accurate modeling of the circuit's dynamic behavior, highlighting the presence of two complex poles and one zero, the position of which directly depends on the compensation parameters adopted. Figure 16 illustrates the resulting frequency response, clearly showing the presence of the zero and the two

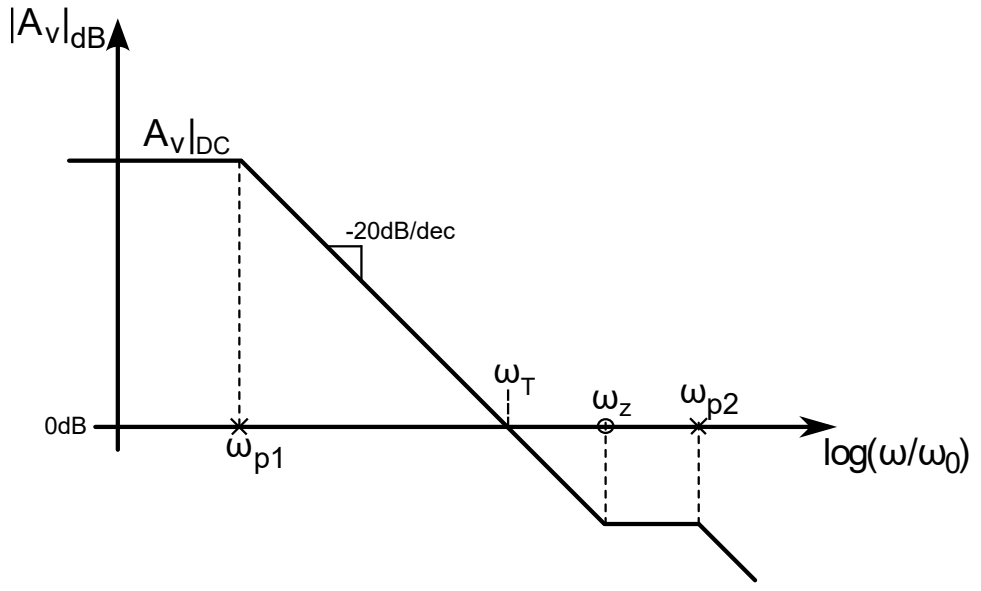

Figure 16: Frequency response of the amplifier with compensation network: the plot highlights the presence of a zero and two complex poles introduced by the compensation network, which contribute to stabilizing the dynamic behavior of the circuit.

complex poles. In this way, the stability of the amplifier can be ensured over the entire range of operating frequencies.
Before performing the Fourier transform of the output signal, it is necessary to understand the relationship between second-order harmonic distortion (HD2) and third-order harmonic distortion (HD3) in order to achieve the desired values.

3.1.4 Harmonic Distortions

Harmonic distortions are an undesirable effect that occurs in nonlinear electronic circuits, such as amplifiers. In particular, second-order harmonic distortion (HD2) and third-order harmonic distortion (HD3) are two of the main components of the total distortion in a system. HD2 arises when the amplifier circuit introduces a spurious component at twice the frequency of the input signal. This phenomenon is primarily caused by asymmetries in the circuit's behavior, such as an asymmetry in the characteristics of the active device, such as transistors.
Third-order harmonic distortion (HD3) can become evident when the output signal assumes an approximately triangular shape. This typically occurs when the amplifier operates in slew-rate limiting mode, i.e., when the rate of change of the output signal exceeds the maximum dynamic speed the circuit can sustain. Under these conditions, the ideal sinusoid is distorted, adopting a sharper, triangular waveform, which is characterized by the predominant presence of odd harmonics. Among

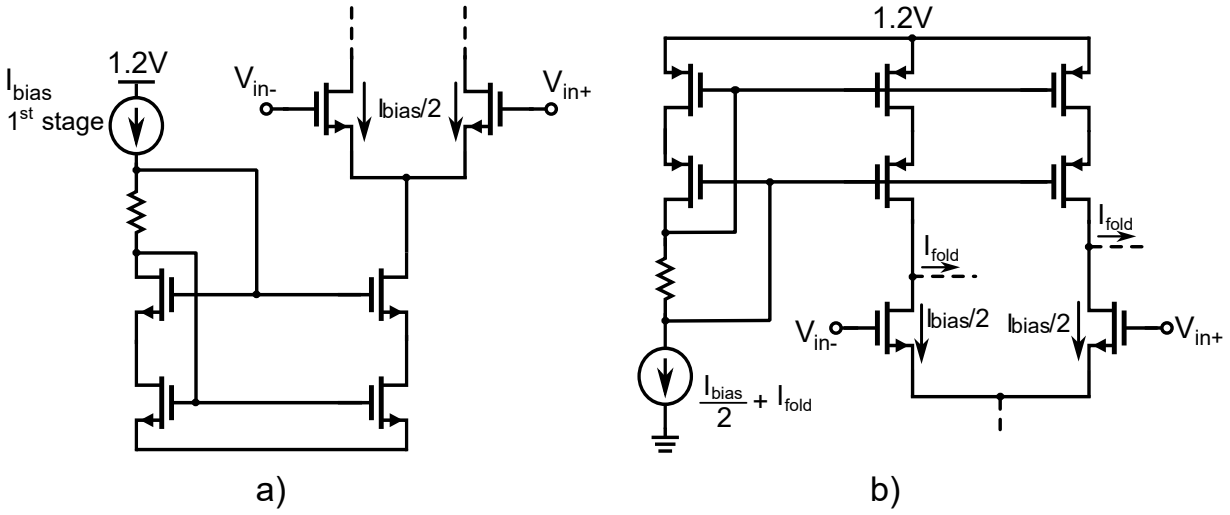

Figure 17: a) High compliance current mirror of the first stage tail generator, b)High compliance current mirror of the first stage head generator. [12]

these, the third harmonic (HD3) is particularly significant, as it represents the first nonlinear component generated by the cubic nonlinear symmetries present in the system.

To achieve harmonic distortions that meet the specifications, the idea is to reduce the effect of channel voltage modulation in the current generators in order to increase their channel resistance, particularly for the tail generator of the first stage and that of the second stage. Increasing their length alone is insufficient and also worsens the phase margin, as parasitic capacitances increase. The cascode considered in the first stage is shown in Figure 17. In the cascode of the first-stage tail current generator (Fig. 17a), there is an increase in HD2, which reduces the loss of gain caused by a low tail resistance. However, this results in a deterioration of HD2 due to the fact that the gate of the MOS of the tail can capacitively couple with the signal from the source of the input MOS (via C_{gd}). Furthermore, if the bias node is not low-impedance, it suffers signal modulations, further degrading linearity. On the other hand, implementing a cascode in the tail current generator does not yield improvements, as it results in a voltage V_{DS} that is too low for the upper current-generation MOS transistors.

However, implementing a cascode in the current generator of the second stage (as shown in Fig. 18) significantly reduces HD2, due to the stabilization of the V_{DS} of the current-generating transistor, thereby improving its linearity.

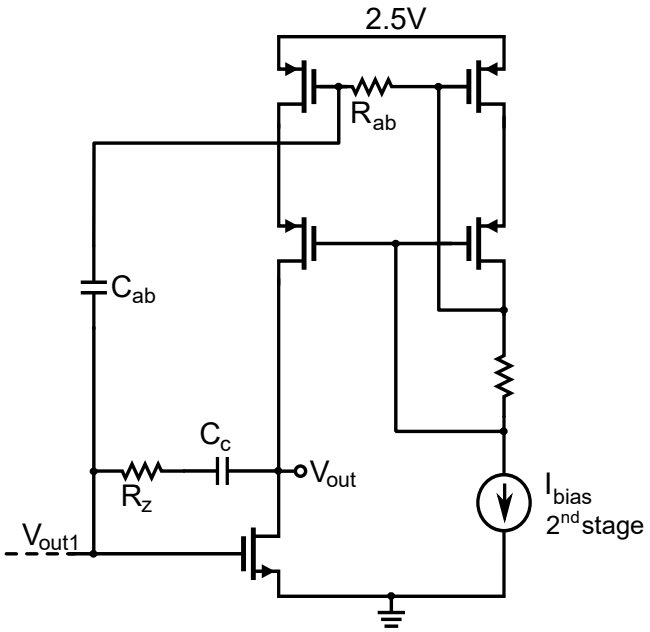

Figure 18: High compliance current mirror of the second stage. [12]

In conclusion, the use of the cascode is advantageous only for the second stage. This is consistent with the fact that, in this stage, a higher supply voltage is available, whereas in the first stage, it was necessary to significantly increase the W/L ratio of the current mirror to accommodate such a low supply voltage.
At this stage, the design of the inverter-based LNA will be carried out, analyzing its behavior in detail and evaluating its performance through circuit-level simulations. The objective is to assess whether this architecture can meet the gain, bandwidth, power consumption, and linearity requirements demanded by ultrasound imaging applications.

3.2 Fully-Differential Inverter-Based LNA

Another possible implementation of the LNA is the fully-differential inverter-based topology. A fully differential inverter-based amplifier can be implemented by replacing the PMOS input pair of a generic common-source amplifier, shown in Fig. 19a, with the inverter input pairs illustrated in Fig. 19b. This approach leverages both active transistors to maximize transconductance and achieve improved area and power efficiency. For the circuit to function correctly as an amplifier, it is

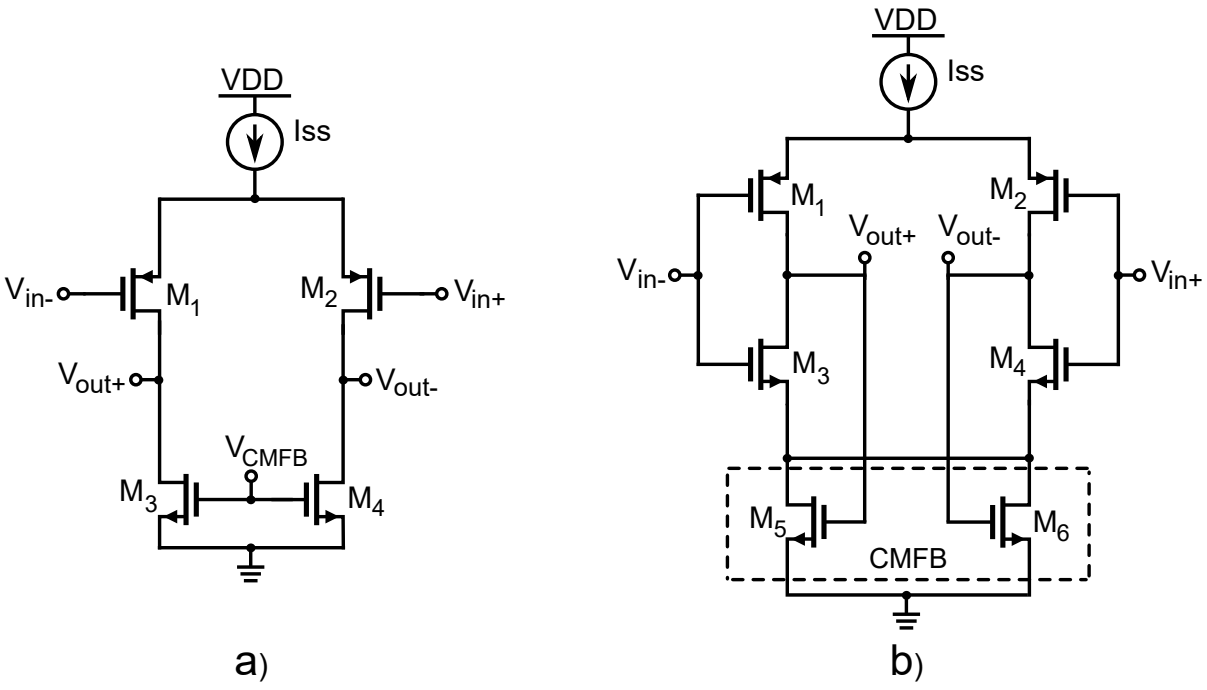

Figure 19: a) Common-Source Differential Amplifier, b)Inverter-Based Differential Amplifier. [14]

essential that transistors M1, M2, M3, and M4 operate in the saturation region, a necessary condition to ensure proper amplification. The differential output voltages, V_{out+} and V_{out-}, are fed back to the gates of transistors M5 and M6, which serve as common-mode voltage stabilizers. Specifically, M5 and M6 operate in the linear region, behaving as voltage-controlled resistors, thus enabling the detection and regulation of the common-mode component present at the circuit output [14]. If the transistors are perfectly matched, the open-loop gain is given by:

$$A_v|_{DC} = \frac{V_{out}}{V_{in}} = 2\left(g_{m1} + g_{m3}\right)\left(r_{ds1} \parallel r_{ds3}\right) \tag{3.11}$$

According to Eq. 2.5, in order to achieve a low input-referred noise (IRN), it is necessary to maximize the input transconductance. One effective way to accomplish this is by increasing the bias current I_{SS}, thereby enhancing the transconductance and, as a result, improving the gain-bandwidth product (GBW). However, increasing the bias current may also lead to a reduction in the output resistance, potentially degrading the open-loop gain. Therefore, a trade-off must be carefully established among GBW, IRN, and gain. With this design approach, a gain of approximately 49 dB was achieved, along with a GBW of 300 MHz and a phase margin of 70°.
A gain of 49 dB (corresponding to a linear gain of approximately 280) is relatively high for a single-stage amplifier. Nevertheless, in applications such as ultrasonic imaging, where the input signals are typically very weak, a higher overall gain or improved accuracy may be required to ensure an adequate signal-to-noise ratio.
To further increase the open-loop gain, a cascode configuration was introduced, as shown in Fig. 20, by incorporating transistors M_7 - M_{10}. This design choice increases the output impedance of the circuit, thereby enhancing the overall gain performance:

$$A_v|_{DC} = 2(g_{m1} + g_{m3})\left(r_{ds1} g_{m9} r_{ds9} || r_{ds3} g_{m7} r_{ds7}\right) \tag{3.12}$$

However, an additional critical issue to consider is the common-mode swing. Since the two input transistors share the same biasing node, the common-mode voltage can limit the proper operation of the circuit. Specifically, transient analysis reveals that, when large input signals are present, the output signal is not amplified correctly, leading to saturation or clipping issues.
To mitigate this effect, it is possible to reduce the common-mode swing by separat-

ing the gates of the input transistors and biasing them individually with two distinct voltages, V_{Nb} and V_{Pb}, applied through the resistors R_b. Moreover, to guarantee an adequate voltage headroom and support a larger output dynamic range, the circuit operates from a 2.5 V supply voltage. This choice allows the MOS transistors to remain in the saturation region even for large output swings, thereby preserving the linearity and amplification capability required for ultrasound imaging applications. This solution improves the linearity of the circuit and ensures an adequate dynamic range of the output signal, even in the presence of large input signals. By separating the gates of the input transistors and biasing them with two distinct potentials, it became necessary to divide the input capacitors and the feedback capacitors into

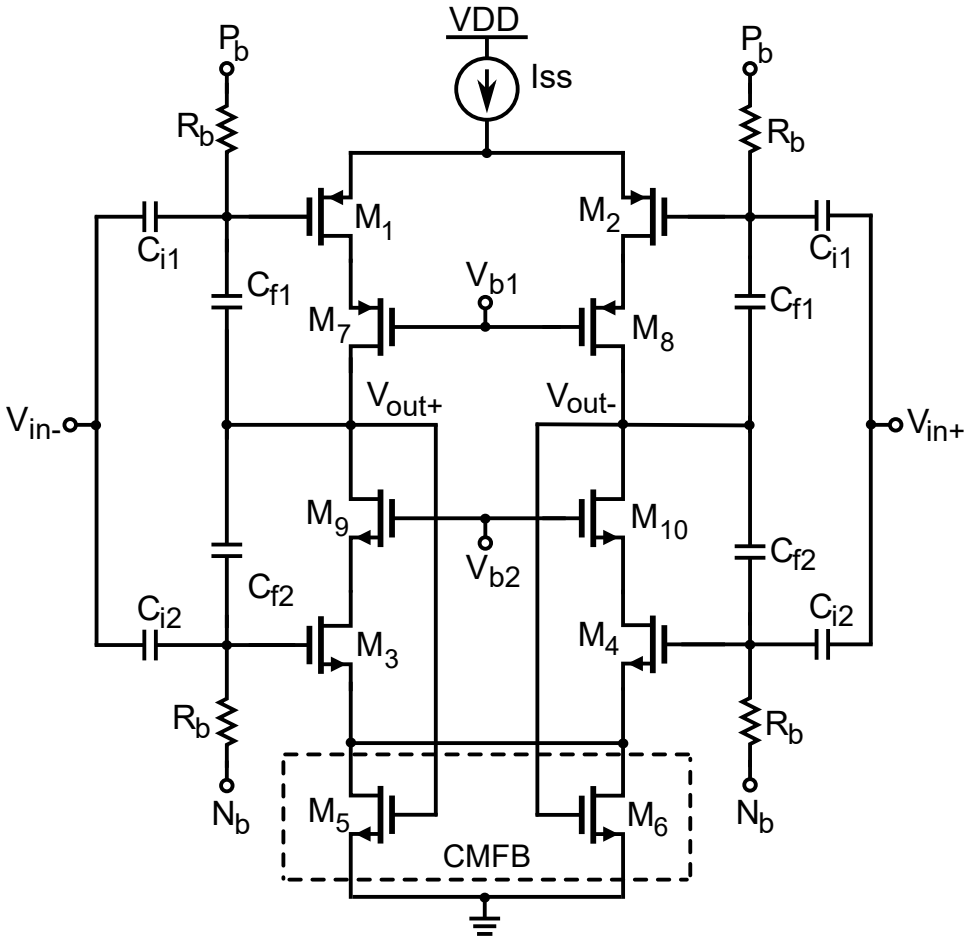

Figure 20: Schematic of a Fully-Differential inverter-based LNA in closed-loop configuration, with separated gate polarization and additional transistors. [14]

two identical pairs. In this way, the mid-band gain can be expressed as:

$$A_M = \frac{1}{2}\left(\frac{C_{i1}}{C_{f1}} + \frac{C_{i2}}{C_{f2}}\right) = \frac{Ci}{C_f} \tag{3.13}$$

Considering

$$\frac{C_{i1}}{C_{f1}} = \frac{C_{i2}}{C_{f2}} = \frac{Ci}{C_f}$$

In order to maintain the circuit's input impedance unchanged, it is necessary to halve the input capacitors of each branch, as well as the feedback capacitors, compared to the original configuration. This adjustment helps preserve the overall area occupied by the capacitors [15].
Under these conditions, the transfer function of the circuit, considering the effect of the bias resistance R_b, can be expressed as:

$$\frac{V_{out}}{V_{in}}(s) = \frac{C_i}{C_f}\frac{sC_iR_b}{1+sC_iR_b} \tag{3.14}$$

The obtained expression highlights the presence of a zero at the origin and a real pole at s = $-\frac{1}{C_iR_b}$, due to the presence of the bias resistance R_b. At low frequencies, the transfer function increases linearly with frequency (high-pass behavior), and then stabilizes at a constant value determined by the ratio between C_i and C_f, which represents the mid-band gain. However, at higher frequencies, an additional pole may appear, generated by parasitic capacitances or by the intrinsic limitations of the active devices. The presence of this second pole alters the circuit's response, resulting in a band-pass behavior. This effect imposes a limitation on the amplifier's effective bandwidth and may degrade its response to high-frequency ultrasound signals. The next chapter will present and discuss the simulations performed, along with the obtained results.

Chapter 4

Simulation Results

This section presents the simulation results related to the design and optimization of the proposed LNA architectures. All simulations were conducted using Cadence Virtuoso, an advanced electronic design automation (EDA) platform widely adopted for the analysis and verification of analog and mixed-signal integrated circuits. The technology used for circuit implementation is a 40 nm CMOS process, chosen for its excellent trade-off between performance, power consumption, and integration density.

The transistor sizing was primarily carried out by adjusting the geometric parameters of length (L) and width (W). No strict constraints were imposed on the multiplicity (M) or the number of fingers, in order to allow greater flexibility during the performance tuning phase. It is important to note that, although not strictly constrained, these parameters were carefully considered during the design process, as they significantly affect factors such as device matching, parasitic capacitances, channel resistance, linearity, and overall layout area.

The simulations performed include several fundamental analyses aimed at validating the overall performance of the system. Specifically:

- DC analysis: performed to determine and verify the correct biasing points of the transistors in each proposed configuration;
- AC analysis: conducted to evaluate the amplifier's frequency response, with particular attention to the passband and phase margin, across a frequency range that includes and extends beyond the operational bandwidth typical of PMUTs (Piezoelectric Micromachined Ultrasonic Transducers);

- Transient analysis: carried out to observe the LNA's dynamic response to sinusoidal input signals and to verify time-domain stability. This type of simulation is particularly useful for emulating the system's behavior when receiving signals from a PMUT, where the wave amplitude and phase vary depending on the target distance and the propagation medium characteristics. These simulations thus allow for assessing the amplifier's suitability for ultrasound imaging applications under realistic operating conditions;
- Spectral analysis: performed to analyze the harmonic content of the output signal and to quantify harmonic distortions (HD2, HD3). This analysis is crucial for evaluating the integrity of the amplified signal and the impact of circuit nonlinearities on overall system performance;
- Noise analysis: conducted to estimate both the equivalent output noise and the input-referred noise (IRN). The latter represents a critical metric for evaluating the amplifier's sensitivity, particularly in ultrasound imaging applications, where the received signals are extremely weak.

In the following sections, the results obtained from the simulation analyses described above will be presented and discussed in detail, with particular focus on the parameters most relevant to the performance evaluation of the designed LNA circuits.

4.1 Simulation Results of the Single-Ended LNA

This section presents the simulation results for the single-ended LNA architecture. The main performance aspects, including DC operating point, frequency response, transient behavior, harmonic distortion, and noise performance, are analyzed in detail in the following subsections.

4.1.1 DC analysis

Regarding the DC analysis, the optimal operating point of the circuit is achieved when all the transistors operate in the saturation region. By analyzing the input common-mode constraints and the output swing, it is observed that the input common-mode voltage can reach relatively high values without compromising the

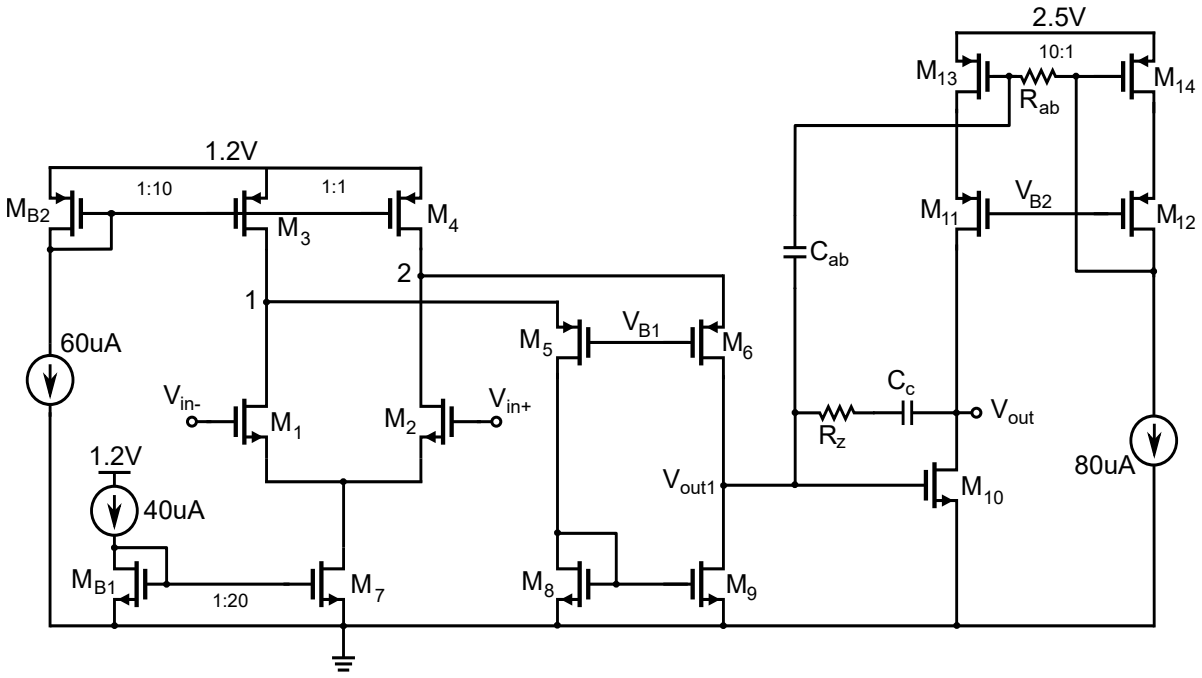

Figure 21: Schematic of the single-ended LNA.

correct operation of the circuit. This is made possible by the bias voltage V_{B1}, which sets the potential at nodes 1 and 2 (Fig. 21) to a sufficiently high level, ensuring that the input transistors M_1 and M_2 remain in saturation even for elevated input common-mode levels. The lower limit for the input common-mode voltage is instead determined by the condition under which transistor M_7 exits saturation and enters the triode region. As for the output swing, it is governed by the proper operation of the Class-AB output stage, composed of transistors M_{13} and M_{11}. The bias voltage V_{B2} must be set such that M_{13} remains in the saturation region. In this way, the maximum positive swing is determined by the sum of the saturation voltages of M_{13} and M_{11}. Conversely, the lower swing limit is set by the minimum voltage that keeps M_{10} in saturation; below this threshold, M_{10} would enter the triode region.

4.1.2 Frequency Analisys

To characterize the amplifier's frequency response and assess its stability, both an AC small-signal analysis and a Stability (STB) analysis were carried out using Cadence Virtuoso. The frequency range adopted for the AC analysis spanned from 1 Hz to 1 GHz, thereby extensively covering the amplifier's operational bandwidth

for PMUT-based applications and ensuring a detailed description of its frequency behavior.

To evaluate the stability of the feedback system, an STB analysis was employed. This analysis allows for the extraction of the open-loop gain, or loop gain, defined as

$$A_{loop} = A_{ol}\beta$$

This quantity represents the overall gain along the feedback path and is critical for determining the gain margin and phase margin, which are key indicators of the stability of a closed-loop system. The analysis was performed by inserting an ideal voltage source (V_{DC}) between the inverting input of the amplifier and the feedback node, as shown in Fig. 22. The voltage source is configured with a DC component of 0 V and an AC magnitude of 1, so as not to disturb the DC biasing point while allowing the injection of a sinusoidal AC signal for analysis.

V_{DC} was directly used as the probe point for the STB analysis, without the need to insert an additional iprobe element. This approach allows:

- Non-invasive analysis of the loop gain, without physically breaking the feedback loop;
- Differential AC signal injection;
- Extraction of the Bode plot for the loop gain ($A_{ol}\beta$) and its corresponding phase.

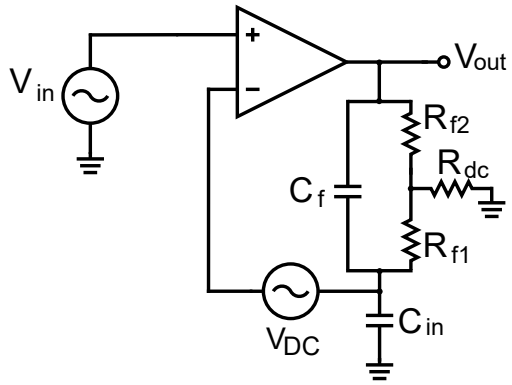

Figure 22: Schematic representation of the amplifier configuration used for loop gain analysis. The ideal voltage source V_{DC}, with DC = 0 V and AC = 1, is inserted between the inverting input and the feedback network. This setup allows performing STB analysis to extract the loop gain ($A_{ol}\beta$) and evaluate the stability of the closed-loop system.

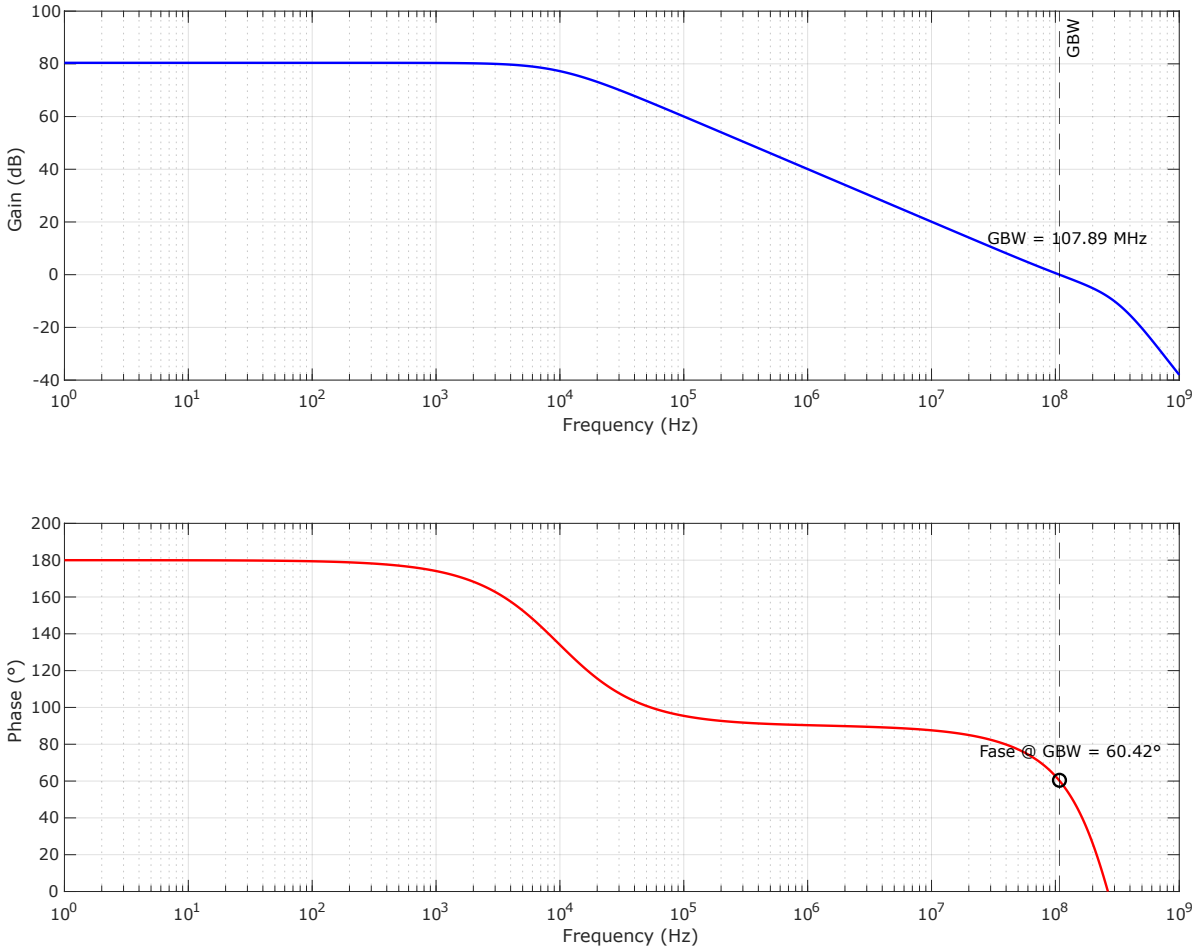

Figure 23: Frequency response of the Open-Loop single-ended amplifier.

The results obtained from the STB analysis reveal the open-loop frequency behavior of the feedback system, showing an initial gain of 80 dB, a gain-bandwidth product (GBW) of 107.89 MHz, and a phase margin of 60.42°, as illustrated in Fig. 23. These values indicate that the system is stable under the considered operating conditions.

After verifying the stability of the system, the closed-loop frequency response of the amplifier was analyzed. For this purpose, the ideal voltage source was removed, thus closing the feedback loop, and a sinusoidal input signal was applied to observe the output behavior. The results obtained are consistent with those predicted by Eq. 3.4 (Fig. 24): a DC gain of 2.85 dB (corresponding to a linear gain of 1.389), the presence of one zero and one pole, a midband gain of approximately 15 dB, and a -3 dB bandwidth of 248.66 MHz, all in agreement with the design specifications listed in Table 2.1. The next step involves the transient analysis, to evaluate the amplifier's behavior when subjected to a sinusoidal input signal, and,

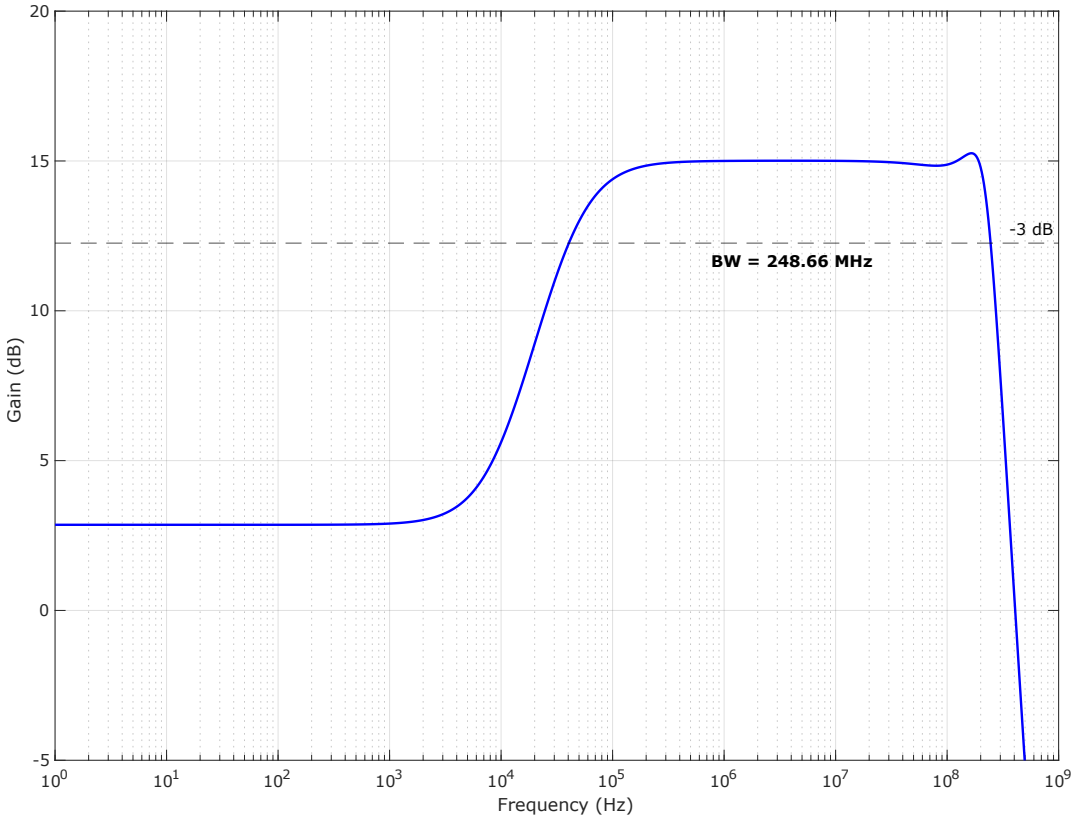

Figure 24: Frequency response of the Closed-Loop single-ended amplifier.

subsequently, the spectral analysis to assess its harmonic distortion.

4.1.3 Transient analisys

To evaluate the dynamic behavior of the amplifier and assess its linearity and response to sinusoidal inputs, a transient simulation was performed in Cadence Virtuoso. The transient analysis allows observation of the circuit's time-domain behavior, providing fundamental information regarding:

- The dynamic response to input signals;
- The distortion of the amplified signal;
- Steady-state stability;
- The fidelity of the output waveform relative to the input.

The simulation was configured by applying a sinusoidal input signal with a moderate amplitude, representative of a typical operating condition where the PMUT

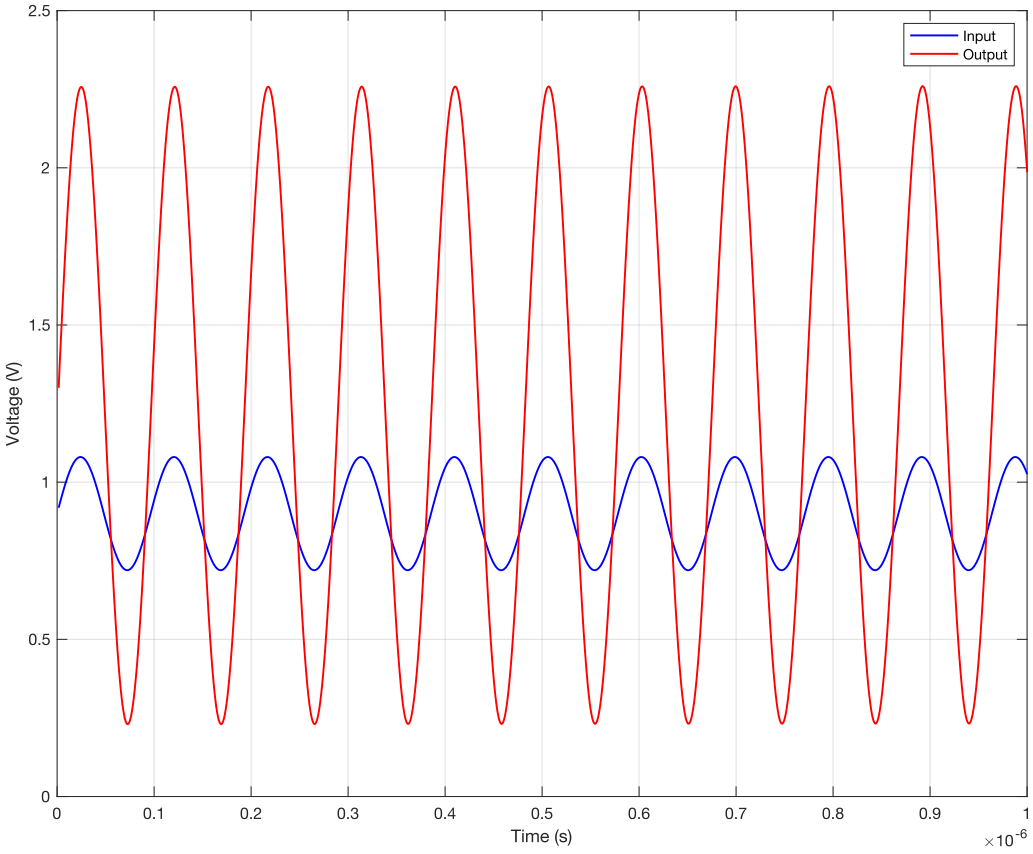

Figure 25: Transient simulation showing the input signal V_{in} and the output signal V_{out}. The amplifier exhibits a clean sinusoidal output centered at 1.25 V with an amplitude of approximately 2 V_{pp}, matching the input frequency of 5 MHz.

is positioned close to the target and generates a relatively stronger echo compared to more distant scenarios. Specifically:

- Input signal V_{in}: sinusoid centered at 0.9 V, 360 mV_{pp} amplitude, 5 MHz frequency;
- Simulation time: 20 μs, sufficient to observe several steady-state periods and identify any transient anomalies;
- Operating conditions: nominal supply voltage, nominal bias settings, no intentional injection of noise or disturbances.

The signals V_{in} and V_{out} were captured simultaneously, as shown in Fig. 25. From the transient simulation results, the following observations can be made:

- The output signal V_{out} maintains a clean sinusoidal shape, consistent with the input, with no evident signs of clipping, compression, or saturation;

- The measured amplitude gain between V_{in} and V_{out} matches the expected design value: the output is centered around 1.25 V with a peak-to-peak amplitude of approximately 2 V_{pp};
- The output frequency perfectly matches the input frequency (5 MHz), confirming that the amplifier performs linear amplification without altering the fundamental frequency.

The transient simulation confirms that the amplifier operates correctly in the linear regime, providing adequate amplification of the sinusoidal input without exhibiting saturation, clipping, or instability. The quality of the output waveform suggests faithful amplification with no macroscopic distortion, laying a solid foundation for the subsequent analyses of harmonic distortion and noise performance, which will be discussed in the following sections.
After confirming the correct dynamic operation through transient analysis, the next step is to assess the harmonic distortion performance for a detailed evaluation of the amplifier's linearity.

4.1.4 Spectral analysis and harmonic distortion

Following the transient analysis, the amplifier's linearity was evaluated through the analysis of harmonic distortion. This evaluation is based on observing the output waveform and identifying any deviations from an ideal sinusoid, which suggest the presence of undesired harmonic components.
To quantify these distortions, a discrete Fourier transform of the output signal was performed, implemented via the Fast Fourier Transform (FFT) tool integrated within the Cadence environment. This technique allows the signal to be transformed from the time domain into the frequency domain, making the spectral components of the signal readily visible.
However, the use of FFT introduces some limitations due to the finite nature of the analyzed signal. When the number of captured signal periods is not an integer, artificial discontinuities are introduced at the time window edges, leading to spectral leakage. This phenomenon can result in an overestimation of harmonic components or a loss of spectral resolution.
To mitigate such effects, a windowing function was applied prior to performing the FFT. In particular, a Hanning window was adopted, due to its favorable trade-

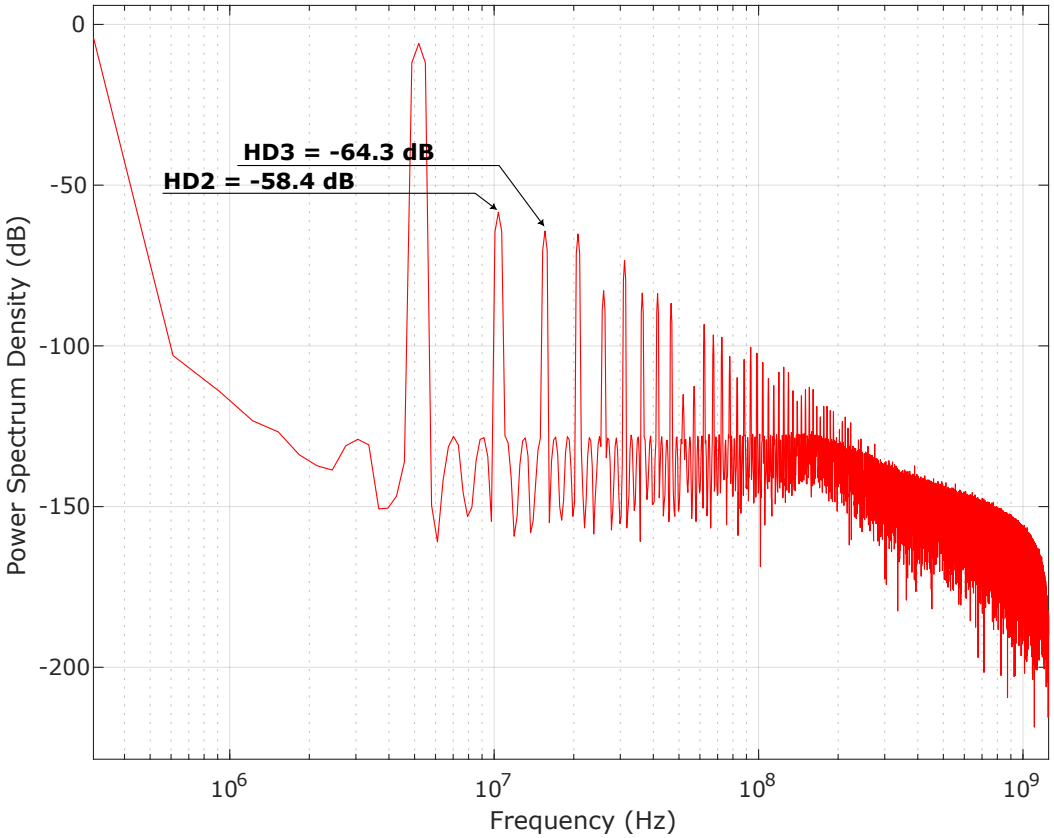

Figure 26: Output frequency spectrum obtained through Fast Fourier Transform (FFT) analysis. The plot highlights the fundamental component at 5 MHz, along with the second- and third-order harmonics at 10 MHz and 15 MHz, respectively, both exhibiting significantly lower amplitudes compared to the fundamental. This analysis allows for the evaluation of harmonic distortion introduced by the amplifier and confirms the good linearity of the designed circuit.

off between frequency resolution and sidelobe attenuation, making it effective for most practical cases. Windowing reduces the amplitude of discontinuities at the sequence edges, thus avoiding the spreading of spectral energy across adjacent frequencies and improving the readability of the harmonic content.

The analysis was performed considering 17 periods of the signal, with a sampling frequency of 2.5 GHz and using 8192 samples. The resulting spectrum is shown in Fig. 26. Clearly observable are:

- The fundamental component at 5 MHz with an amplitude of -5.9 dB;
- The second harmonic at -58.44 dB;
- The third harmonic at -64.28 dB.

From these results, the following metrics were extracted:

- Second-order harmonic distortion (HD2): 52.53 dB;
- Third-order harmonic distortion (HD3): 58.37 dB;
- Total harmonic distortion (THD): -50.73 dB.

These results demonstrate that the designed circuit exhibits excellent linearity, with harmonic distortions well below the acceptable threshold for ultrasound imaging applications, fully meeting the design specifications summarized in Table 2.1.
After completing the characterization of harmonic distortions, it is now essential to analyze the amplifier's noise performance. Noise represents a fundamental limit to the overall system sensitivity, especially in ultrasound imaging applications, where the received signals are extremely weak. The following analysis focuses on evaluating the equivalent input and output noise of the amplifier, in order to verify compliance with the design specifications and ensure high-quality signal acquisition.

4.1.5 Noise analysis

Noise analysis plays a crucial role in evaluating the performance of a low-noise amplifier (LNA), as the noise introduced by the circuit adds to the useful signal, reducing the signal-to-noise ratio (SNR) and consequently degrading the quality of the images acquired in the ultrasound imaging system..
To assess the noise contribution of the amplifier, a noise simulation was performed in the Cadence environment, configured to provide both the output-referred noise spectral density and the input-referred noise spectral density. The latter is of particular interest, as it allows the entire noise contribution of the circuit to be expressed as if it were directly present at the system input, enabling a direct comparison with the signal level generated by the PMUT.
The simulation was carried out over a frequency range from 1 Hz to 1 GHz. To obtain the input-referred noise curve, the output noise was normalized by the frequency-dependent gain according to the relation:

$$v_{n,in}(f) = \frac{v_{n,out}(f)}{A_v(f)}$$

where:

- $v_{n,out}(f)$ is the output noise spectral density [nV/$\sqrt{Hz}$];
- $A_v(f)$ is the amplifier gain at frequency f;
- $v_{n,in}(f)$ is the input-referred noise spectral density.

This transformation enables the evaluation of the circuit noise as if it were present directly at the input and represents a fundamental metric for comparing the LNA with other designs or target specifications. Figure 27 and Fig. 28 show the input-referred noise and the equivalent output noise spectra, respectively. Both curves exhibit the expected behavior for a CMOS amplifier:

- At low frequencies, an increase in noise with a 1/f trend, typical of flicker noise, is observed;
- Above 100 kHz, both curves stabilize, showing a white noise floor due to thermal noise.

The minimum value in the white noise region is approximately 2.5 nV/$\sqrt{Hz}$, located around the frequency of interest (3 MHz), which is a key metric for evaluating the circuit's sensitivity. This value is consistent with expectations for an LNA

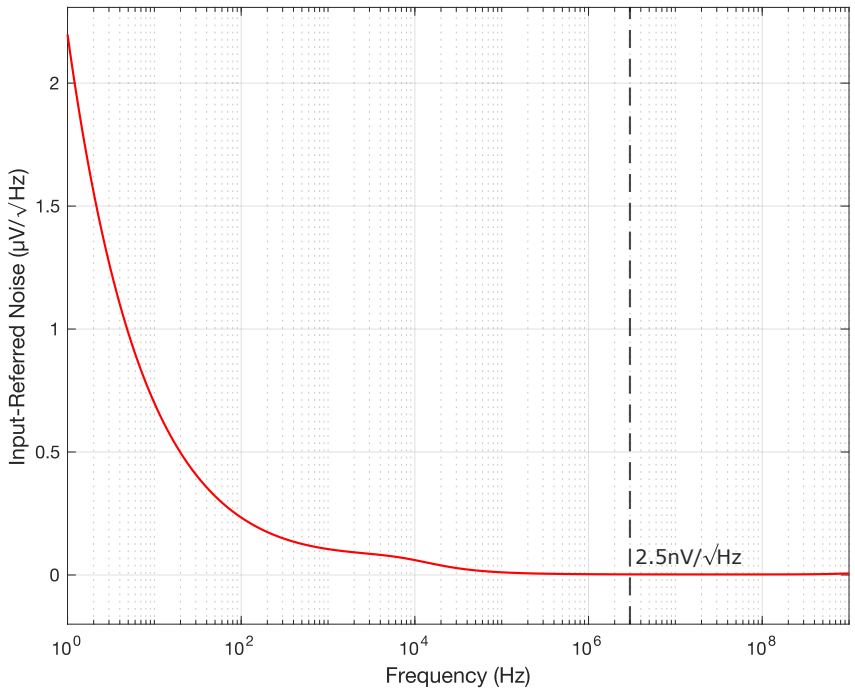

Figure 27: Input-referred noise spectral density of the designed LNA. The curve shows a clear 1/f noise behavior at low frequencies, followed by a flat thermal noise floor at higher frequencies.

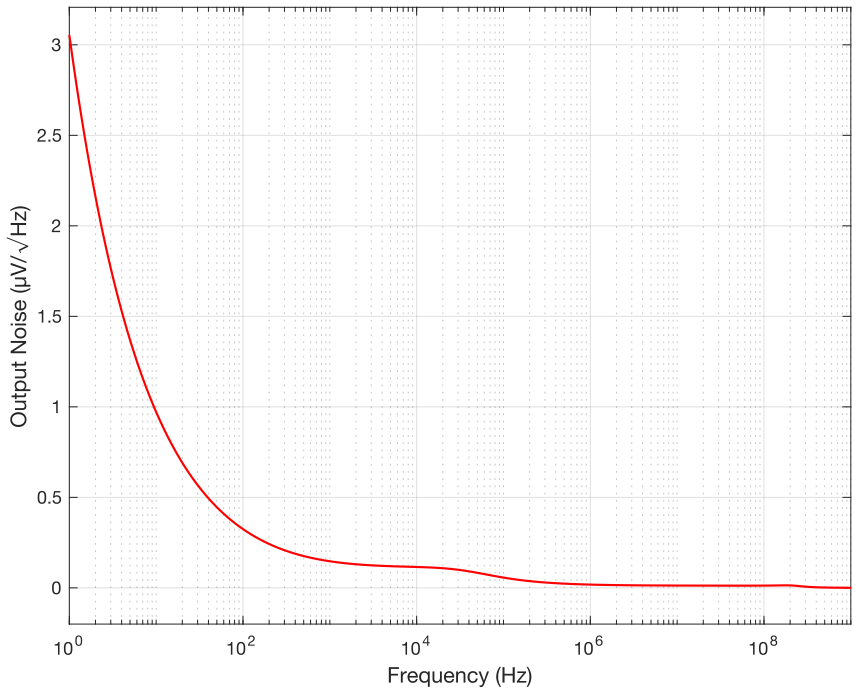

Figure 28: Equivalent output noise spectral density of the LNA. The graph highlights the same two region observed in the input-referred noise: low-frequency flicker noise and high-frequency white noise.

optimized in CMOS technology.
Achieving low noise spectral densities was made possible through careful design choices, including:

- the use of input transistors with high transconductance;
- careful selection of the bias point to maximize linearity and SNR;
- minimization of bias and feedback resistances.

The comparison between the two graphs confirms the consistency between the output noise and the input-referred noise, obtained by dividing the former by the gain as a function of frequency. The good agreement between the curves demonstrates the proper design of the feedback loop and the stability of the gain across the useful bandwidth.
The minimum input-referred noise value is fully compliant with the project specifications reported in Table 2.1. Thus, the analysis demonstrates that the designed amplifier not only ensures high linearity (as discussed in previous sections) but also achieves excellent noise performance, which is critical for high-precision medical

imaging applications. With the noise analysis of the previous design completed, attention is now directed toward a fully differential inverter-based LNA, whose schematic, biasing considerations, and dynamic performance will be thoroughly analyzed.

4.2 Simulation Result of the Inverter-Based Fully-Differrential LNA

The simulation results of the inverter-based fully differential LNA are discussed in this section. The analysis starts from the DC operating conditions to ensure correct device biasing, and then proceeds to characterize the circuit's frequency response, transient behavior, linearity, and noise performance.

4.2.1 DC analysis

Figure 29 shows the schematic of the proposed fully differential inverter-based LNA. As observed from the DC analysis, the optimal operating point is achieved when all transistors operate in the saturation region, except for M_5 and M_6, which are biased in the triode region and form an integral part of the common-mode feedback (CMFB) circuit. Operating in triode, these transistors behave as common-mode controlled resistances and provide a feedback path that helps stabilize the output common-mode level. This simple approach eliminates the need for a dedicated error amplifier by exploiting the direct connection between the output nodes and the gates to naturally close the feedback loop.

When analyzing the lower limit of the output swing, the output voltage can drop sufficiently to drive transistors M_9 and M_{10} into the triode region. Their transition is controlled by the bias voltage V_{B2}, which sets their operating point. Ideally, V_{B2} should be set as low as possible to maximize the downward swing. However, excessively lowering V_{B2} reduces the available common-mode input range, as a high common-mode voltage could push transistors M_3 and M_4 out of saturation.

Similarly, the upper limit of the output swing is constrained by the bias voltage V_{B1}, which controls the operating point of transistors M_7 and M_8. A V_{B1} value that is too low may drive these devices into the triode region, thereby limiting the maximum swing. Conversely, an excessively high V_{B1} value may restrict the allowable

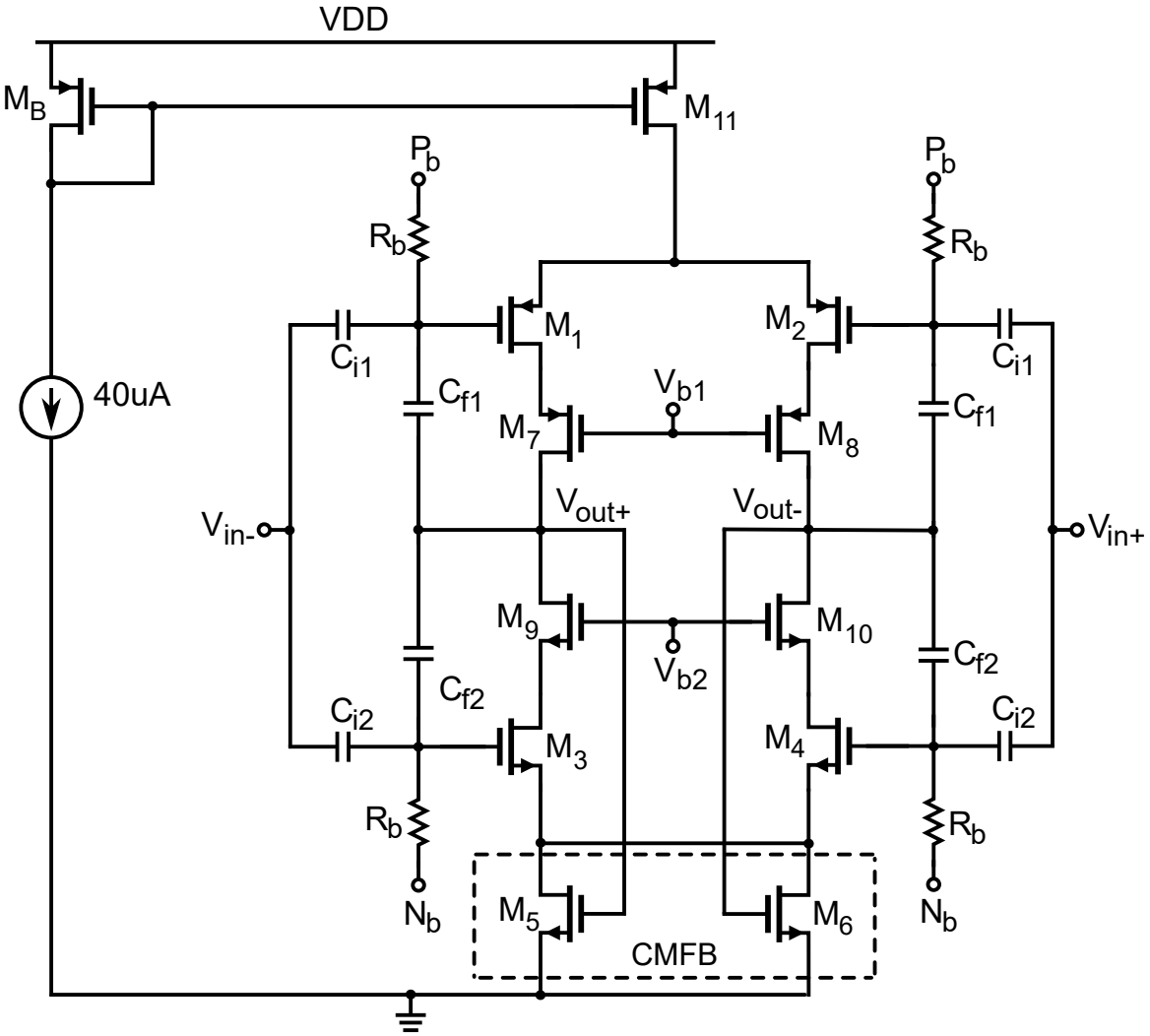

Figure 29: Schematic of the fully differential inverter-based LNA [14].

operating range of transistors M_1 and M_2, pushing them toward the triode region as well.

After verifying the correct biasing of all devices and analyzing the dynamic swing constraints, the dynamic characterization of the circuit is performed through frequency response analysis. This analysis is essential to assess key performance parameters such as bandwidth, gain, and stability, which are fundamental for validating the design.

4.2.2 Frequency analysis

As previously described for the single-ended amplifier, an AC analysis was also carried out for the fully differential LNA, both in open-loop and closed-loop con-

figurations, over a frequency range spanning from 1 Hz to 1 GHz. In this inverter-based architecture, the gates of the input NMOS and PMOS transistors were structurally separated to enhance the available output swing. This design choice, made early in the development phase, enables an improved maximum swing without affecting the correct DC biasing.

During the open-loop AC analysis, a small-signal differential excitation was applied across the four separate input terminals, while maintaining the DC bias levels unchanged. This approach allowed linearization of the amplifier's response around the operating point without introducing any bias variations. The obtained results, shown in Fig. 30, exhibit a low-frequency gain of 65 dB, a gain-bandwidth product (GBW) of 178.8 MHz, and a phase margin of 60.24°. These values highlight a stable dynamic response and improved performance compared to the previously analyzed single-ended architecture, featuring an extended bandwidth while maintaining an adequate stability margin.

After completing the open-loop analysis, the closed-loop frequency response of

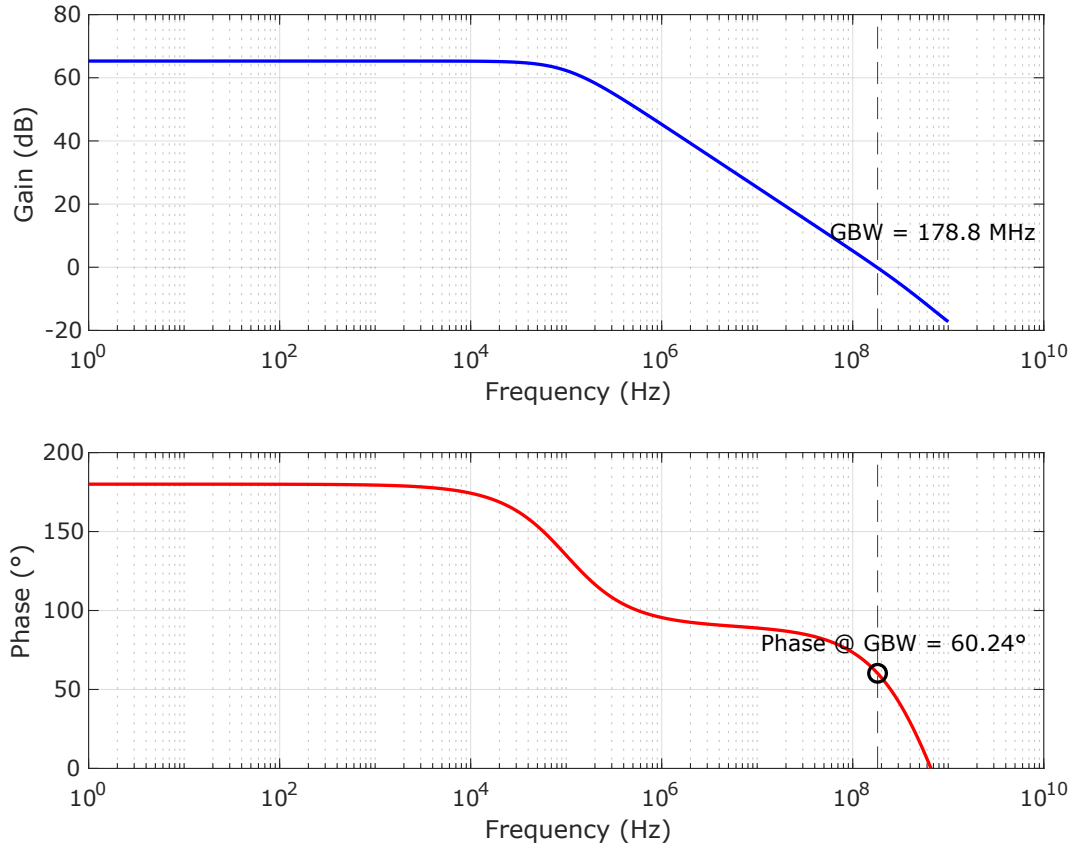

Figure 30: Open-loop frequency response of the fully differential inverter-based LNA.

the amplifier was characterized. Upon restoring the capacitive feedback network, a small differential AC signal was applied while keeping the DC biasing unchanged. The results, reported in Fig. 31, confirm the expected theoretical behavior described by Eq. 3.14: the circuit exhibits a band-pass response with an in-band differential gain of approximately 21 dB and a -3 dB bandwidth of 37 MHz. Compared to the single-ended version, the fully differential configuration shows a reduced bandwidth; however, the achieved value remains fully compliant with the design specifications summarized in Table 2.1. Based on these findings, the transient analysis will now be conducted to verify the circuit's dynamic linearity, followed by the spectral analysis aimed at evaluating the harmonic distortion introduced by the amplifier.

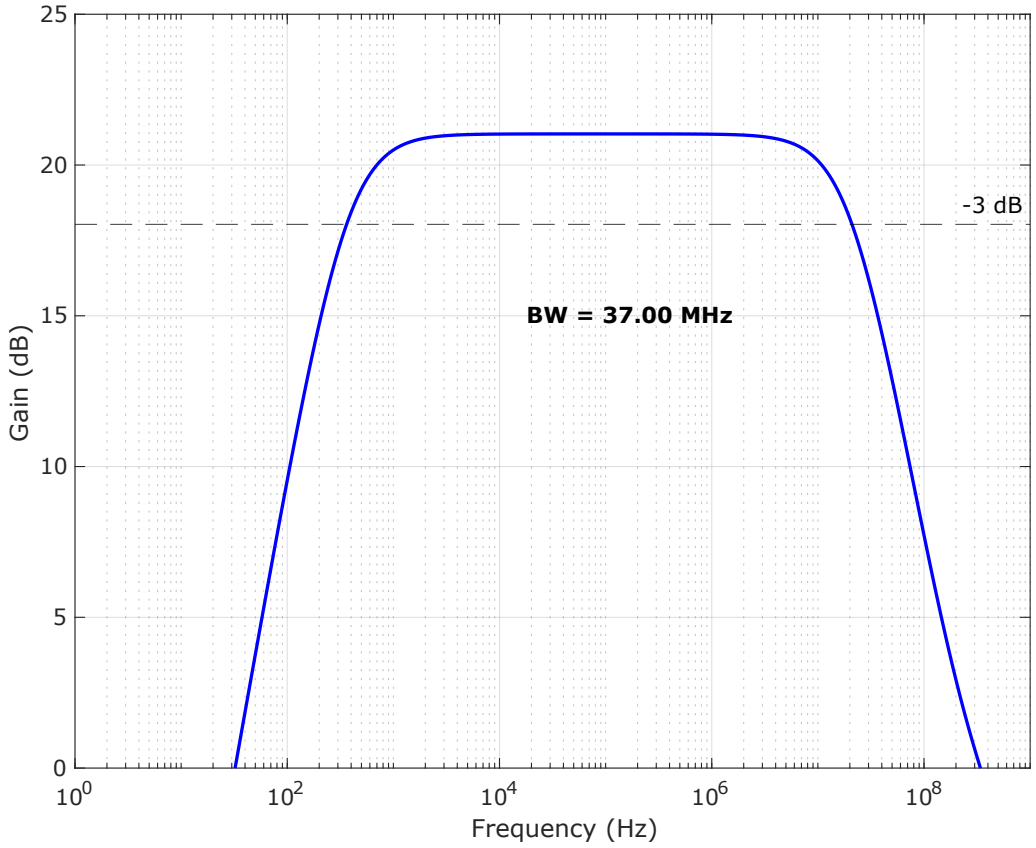

Figure 31: Closed-loop frequency response of the fully differential inverter-based LNA.

4.2.3 Transient analysis

To verify the dynamic behavior of the fully differential amplifier, a transient simulation was performed in the Cadence environment. The objective of the simulation is to validate the linearity, the symmetry between the two differential branches, and the quality of the sinusoidal signal amplification under dynamic conditions.
Compared to the single-ended configuration, two key design improvements were introduced in the fully differential inverter-based architecture. First, the gates of the PMOS and NMOS transistors in each inverter branch were physically separated, enabling independent DC biasing through the voltages P_b and N_b. This design choice allows for a finer adjustment of the operating point, maximizing the output swing and preventing clipping or saturation loss in either device.
Second, to enable such gate separation without compromising the dynamic response, the input and feedback capacitors (C_i e C_f) were divided into two separate components (C_{i1}, C_{i2} e C_{f1}, C_{f2}), thereby preserving the overall frequency response of the circuit. The circuit was stimulated with a differential sinusoidal input signal with the following characteristics:

- V_{in+}: sinusoid centered at 1.25 V, 360 $\mathrm{mV_{pp}}$ amplitude, 5 MHz frequency;
- V_{in-}: complementary sinusoid, 180° out of phase with V_{in+};
- Simulation duration: 20 μs.

Since the amplifier employs capacitive feedback, the circuit's response depends exclusively on the differential component of the input signal, making the absolute common-mode value irrelevant for amplification purposes. The output common-mode level is stabilized by the common-mode feedback (CMFB) circuit, ensuring proper dynamic balancing between the two branches. Figure 32 shows the differential waveforms for the input V_{in+} - V_{in-} and output V_{out+} - V_{out-} signals. The results demonstrate a clean, balanced, and expected dynamic behavior. The output exhibits a symmetric differential sinusoidal waveform, free from clipping or compression, with the output frequency matching the input frequency (5 MHz).
In conclusion, the transient analysis confirms the correct dynamic operation of the fully differential amplifier, highlighting a high waveform quality and a linear, symmetric behavior between the two branches. The introduced structural modifications (gate separation and capacitor splitting) prove effective in maximizing the

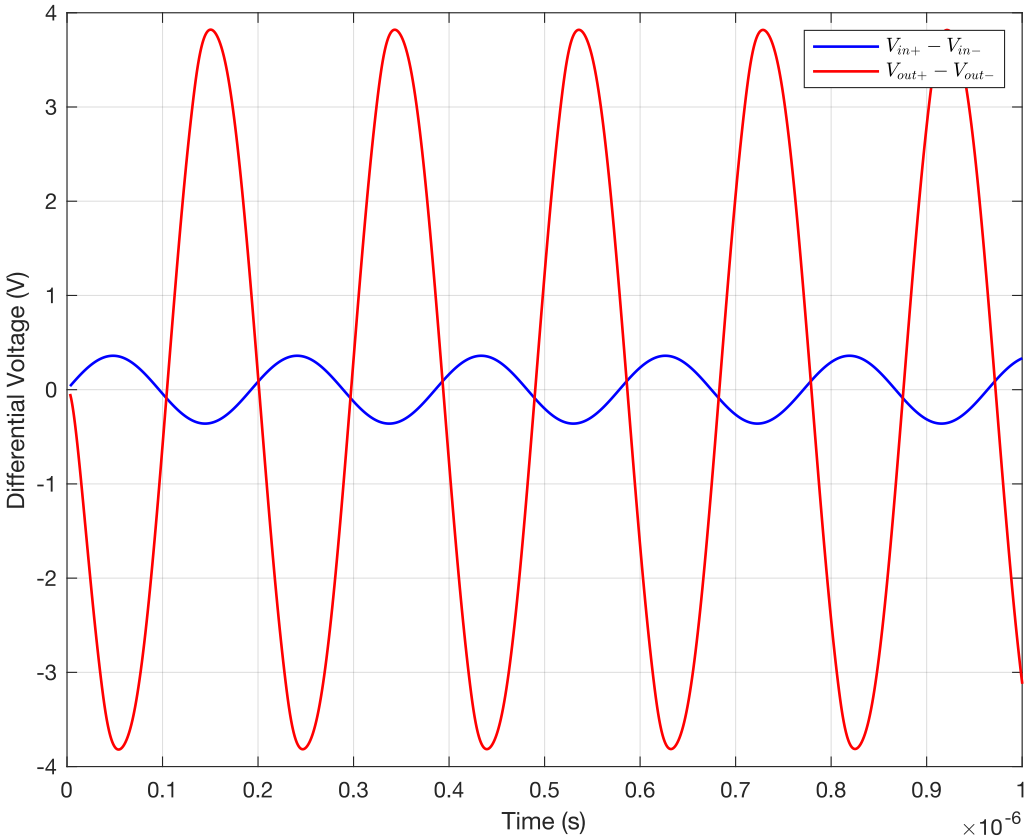

Figure 32: Transient simulation of the fully-differential inverter-based LNA. The differential input V_{in+} - V_{in-}, and output V_{out+} - V_{out-} waveforms are shown, confirming the linear and balanced dynamic behavior of the amplifier.

output swing without degrading the frequency performance, thus providing a solid foundation for the subsequent linearity and harmonic distortion analyses.

4.2.4 Spectral analysis and harmonic distortion

Following the transient analysis, a spectral characterization of the fully differential amplifier was conducted to assess the dynamic linearity and quantify the harmonic distortions introduced. The analysis was carried out using the same approach adopted for the single-ended configuration, namely by applying the Fast Fourier Transform (FFT) to the differential output signal V_{out+} - V_{out-} obtained from the transient simulation.

To ensure comparability of the results, the simulation parameters were kept unchanged: Hanning windowing, acquisition of 17 periods, a sampling frequency of 2.5 GHz, and a total of 8192 samples. The resulting output spectrum, shown in Fig. 33, clearly highlights:

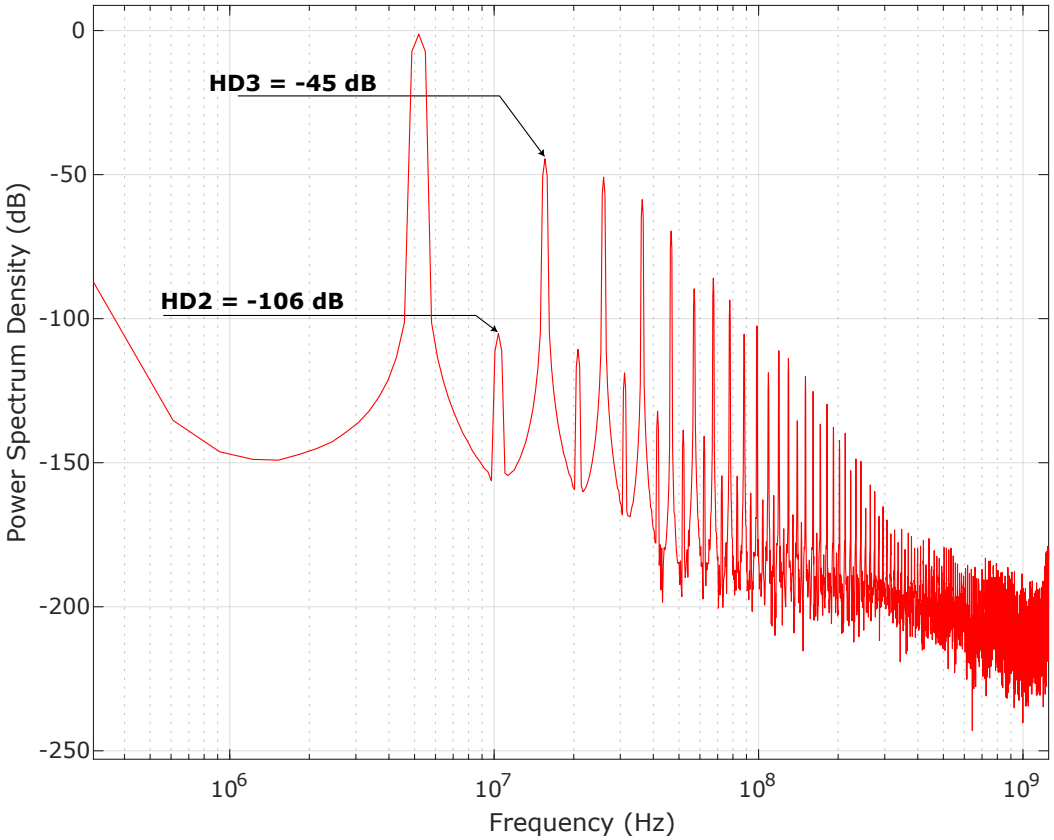

Figure 33: Output frequency spectrum of the fully differential inverter-based LNA, obtained through Fast Fourier Transform (FFT) of the differential signal V_{out+} - V_{out-}. The plot highlights the fundamental component at 5 MHz, along with the second- and third-order harmonics.

- The fundamental component at 5 MHz with an amplitude of approximately -1 dB;
- The second harmonic at 10 MHz with an amplitude of approximately -106 dB;
- The third harmonic at 15 MHz with an amplitude of approximately -45 dB.

From these measurements, the following distortion figures are obtained:

- Second-order harmonic distortion (HD2): 105 dB;
- Third-order harmonic distortion (HD3): 44 dB;
- Total harmonic distortion (THD): approximately -42.2 dB.

It is important to note that, although a fully differential architecture is theoretically immune to even-order distortions, the presence of a residual second harmonic

(-106 dB) can be attributed to practical imperfections in the symmetry between the two differential branches, such as device mismatches or layout asymmetries. Nevertheless, the high ratio between the fundamental and the second harmonic, approximately 105 dB, confirms the excellent linearity and dynamic balance achieved by the amplifier. Having consolidated the harmonic characterization, the analysis now proceeds with the evaluation of the noise performance of the fully differential amplifier.

4.2.5 Noise analysis

Following the harmonic distortion analysis, the noise performance of the fully differential amplifier was evaluated. The analysis was carried out using the same approach adopted for the single-ended configuration, through noise simulations in the Cadence environment.
Both the input-referred noise spectral density and the equivalent output noise spectral density were extracted over a frequency range from 1 Hz to 1 GHz. The normalization methodology between output noise and frequency-dependent gain was maintained unchanged, enabling a direct comparison with the results previously obtained. The obtained curves, shown in Fig.34 and Fig.35, exhibit the expected behavior:

- A low-frequency region dominated by flicker noise (1/f);
- A white noise floor beyond 100 kHz, attributed to thermal noise.

The minimum value of the input-referred noise spectral density is approximately 3.96 nV/$\sqrt{Hz}$ within the band of interest. Although slightly higher than that observed in the single-ended configuration, this value fully complies with the design specifications and meets the sensitivity requirements for ultrasound imaging applications. The comparison between output noise and input-referred noise further confirms the accuracy of the gain model and the dynamic stability of the circuit. The achievement of low noise spectral densities results from the combined effect of a balanced differential architecture, the use of high-transconductance input transistors, and the optimization of the biasing points.

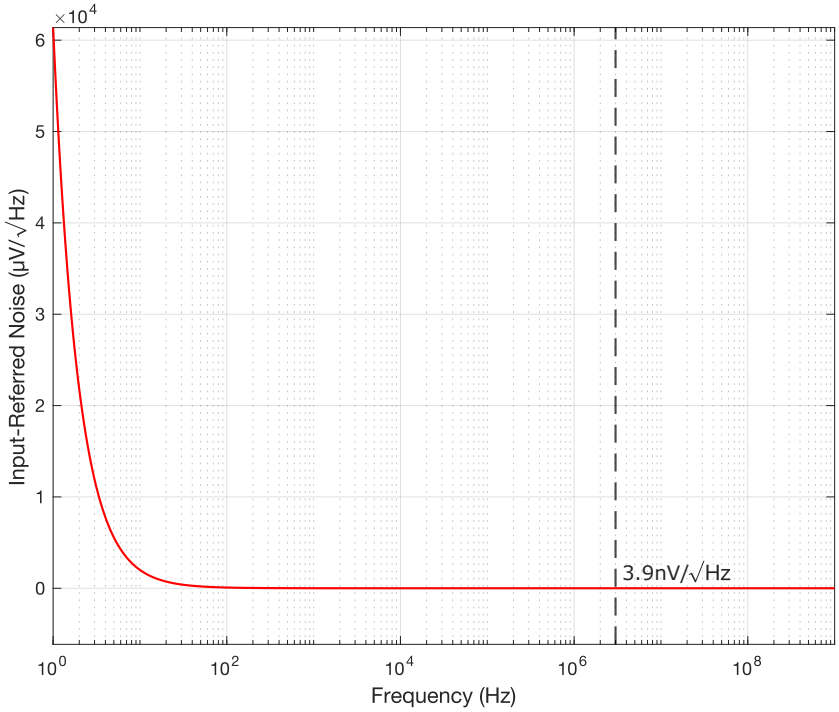

Figure 34: Input-referred noise spectral density of the fully differential inverter-based LNA. The curve exhibits typical 1/f behavior at low frequencies and a white noise floor at higher frequencies.

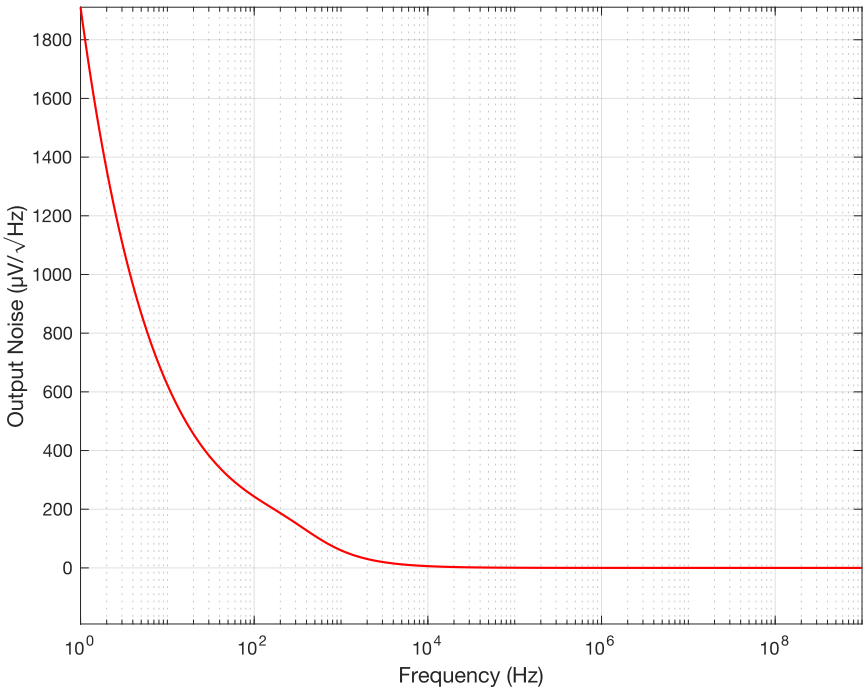

Figure 35: Equivalent output noise spectral density of the fully differential inverter-based LNA, highlighting the expected flicker noise and thermal noise regions.

4.3 Comparative Analysis

During the design process of low-noise amplifiers (LNAs) for ultrasound imaging applications, two distinct architectures were developed and analyzed: a single-ended LNA based on a folded cascode core followed by a class-AB output stage, and a fully differential LNA employing an inverter-based topology.
The first solution (folded cascode + class AB) ensures high gain, wide output dynamic range, and good linearity, thanks to the high output impedance and voltage headroom typical of cascode structures. The second solution (inverter-based fully differential) is optimized for simplicity, reduced area occupation, and low power consumption, leveraging the high transconductance efficiency (g_m/I_D) characteristic of inverter stages.
It should be noted, however, that although the fully differential structure theoretically provides improved common-mode noise rejection, in this design the benefit is somewhat limited due to the simplicity of the common-mode feedback circuit and the architectural compromises made to maximize output swing.
This section presents a comparative analysis between the two designs, highlighting the key performance parameters obtained through simulation. The comparison focuses on aspects such as gain, bandwidth, harmonic distortion, noise performance, power consumption, and circuit complexity, providing a comprehensive evaluation of the architectural trade-offs.
Table 4.1 provides a summary comparison of the main performance metrics achieved by the two architectures: the single-ended folded-cascode amplifier with class-AB output buffer, and the inverter-based fully differential amplifier.
First, it can be observed that the folded-cascode architecture achieves a significantly higher low-frequency gain (80 dB) compared to the inverter-based solution (65 dB), as expected due to the higher output resistance of the folded-cascode topology.
Similarly, the gain bandwidth product (GBW) is higher for the inverter-based amplifier (178.8 MHz versus 107.8 MHz), owing to the lower impedance at internal nodes and reduced parasitic capacitances. However, analyzing the usable bandwidth (-3 dB cutoff), an opposite trend is noted: the folded-cascode amplifier exhibits a -3 dB bandwidth of 248.6 MHz, significantly wider than the 37 MHz achieved by the inverter-based design. This result can be attributed to differences in feedback loop implementation and the impact of parasitic capacitances in the

Parameter	Folded-Cascode+ClassAB (Single-ended)	Inverter-Based (Fully-Differential)
Low-Frequency Gain (Open-loop)	80 dB	65 dB
Gain Bandwidth (GBW)	107.8 MHz	178.8 MHz
Bandwidth (-3dB cutoff)	248.6 MHz	37 MHz
HD2 (Harmonic Distortion 2nd Order)	52.5 dB	105 dB
HD3 (Harmonic Distortion 3rd Order)	58.3 dB	44dB
THD (Total Harmonic Distortion)	-50.7 dB	-42.2 dB
Input-Referred Noise (IRN)	2.5 nV/$\sqrt{Hz}$	3.9 nV/$\sqrt{Hz}$
Power consumption	3.85 mW	2.09 mW

Table 4.1: Summary of key performance metrics for the designed LNAs: Folded-Cascode+ClassAB (single-ended) and Inverter-Based (fully differential).

fully differential structure.

Regarding linearity performance, the inverter-based amplifier shows excellent suppression of the second harmonic (HD2), achieving 105 dB compared to 52.5 dB in the folded-cascode design. This improvement is attributed to the natural common-mode rejection provided by the fully differential configuration. Conversely, the folded-cascode architecture performs better in terms of third-order harmonic distortion (HD3), achieving 58.3 dB compared to 44 dB for the inverter-based amplifier, and also exhibits a lower total harmonic distortion (THD) of -50.7 dB versus -42.2 dB.

From a noise perspective, the folded-cascode amplifier achieves superior performance, with an input-referred noise of 2.5 nV/$\sqrt{Hz}$, lower than the 3.9 nV/$\sqrt{Hz}$ measured in the inverter-based design. This outcome can be partially explained by the lower efficiency of the inverter-based architecture in suppressing common-mode noise. Finally, in terms of power consumption, the inverter-based amplifier proves more efficient, consuming 2.09 mW compared to 3.85 mW for the folded-

cascode design, making it more suitable for applications with stringent energy constraints.
In order to objectively compare the overall performance of the two amplifiers, a specific Figure of Merit (FoM) was introduced, simultaneously accounting for both noise contribution and power consumption.
The adopted FoM is defined as the product of the input-referred noise (IRN) and the square root of the power consumption, namely:

$$FoM = IRN * \sqrt{P_{cons}}$$

where:

- IRN is the input-referred noise expressed in nV/$\sqrt{Hz}$;
- P_{cons} is the power consumption expressed in Watts.

This definition is particularly appropriate in the context of amplifiers intended for ultrasound imaging applications, where it is essential to maximize sensitivity while minimizing energy consumption. A lower FoM value indicates better performance, corresponding to an amplifier with both low noise and low power consumption.
Calculating the FoM for the two architectures yields:

$$FoM_{Folded-Cascode+ClassAB} = 2.5nV/\sqrt{Hz} * \sqrt{3.85mW} = 0.155\frac{nV\sqrt{W}}{\sqrt{Hz}}$$

$$FoM_{Inverter-Based} = 3.9nV/\sqrt{Hz} * \sqrt{2.09mW} = 0.178\frac{nV\sqrt{W}}{\sqrt{Hz}}$$

The results show that, although the inverter-based amplifier consumes less power, the folded-cascode+classAB design achieves a lower FoM, thus offering a globally more efficient noise-power trade-off.
In conclusion, the folded-cascode+classAB amplifier emerges as the preferable choice when noise performance and overall efficiency are prioritized, despite its higher power consumption and greater circuit complexity. Conversely, the inverter-based fully differential design is more suitable for applications where minimizing power consumption and silicon area is critical, at the cost of slightly degraded noise and linearity performance. The selection between the two architectures ultimately depends on the specific requirements and constraints of the intended ultrasound imaging application.

Chapter 5

Conclusion

This thesis presented the design, optimization, and simulation of two low-noise amplifier (LNA) architectures intended for ultrasound imaging applications: a single-ended LNA based on a folded-cascode topology with a class-AB output stage, and a fully-differential inverter-based LNA. The main design objectives focused on achieving low input-referred noise, high linearity, wide bandwidth, and low power consumption, addressing the demanding requirements of modern medical ultrasound systems. Extensive simulations were performed using Cadence Virtuoso, covering DC analysis, AC frequency response characterization, transient behavior evaluation, spectral analysis of harmonic distortion, and noise performance assessment.

Both architectures successfully met the target specifications, demonstrating the effectiveness of the design strategies adopted. The comparative analysis between the two designs highlighted the inherent trade-offs between noise performance, linearity, bandwidth, power consumption, and circuit complexity. While the fully-differential inverter-based LNA exhibited superior power efficiency and a more compact implementation, the single-ended folded-cascode LNA achieved higher low-frequency gain, better linearity in terms of third-order distortion (HD3), and significantly lower input-referred noise. To enable a fair comparison, a specific figure of merit (FoM) combining input-referred noise and power consumption was introduced, defined as the product of IRN and the square root of P_{cons}, with lower values indicating better performance.

The folded-cascode LNA achieved a lower FoM value (0.155 nV$\sqrt{W}/\sqrt{Hz}$) compared to the inverter-based LNA (0.178 nV$\sqrt{W}/\sqrt{Hz}$), confirming its superior

global efficiency in balancing noise and energy consumption. This outcome highlights the folded-cascode architecture as the preferable choice for applications where maximum sensitivity and signal integrity are critical, even at the cost of higher power consumption and increased circuit complexity.

Looking ahead, several directions can be explored to further develop and extend this work. First, physical layout implementation followed by post-layout simulations should be performed to assess the impact of parasitic effects on key performance metrics such as bandwidth, noise, and linearity. Moreover, beyond the design of the standalone amplifier, future efforts could focus on integrating the LNA into a complete ultrasound receiver front-end.

In particular, incorporating a Time Gain Compensation (TGC) stage would allow dynamic adaptation of the gain profile to compensate for signal attenuation with propagation depth, thereby preserving the signal-to-noise ratio across the imaging field. In addition, a Programmable Gain Amplifier (PGA) could be introduced after the LNA to fine-tune the amplification dynamically, depending on imaging modes or patient-specific conditions. The development of an integrated LNA–TGC–PGA analog front-end would represent a significant step toward realizing highly integrated, low-power, and high-performance ultrasound imaging systems, suitable not only for conventional clinical applications but also for emerging portable and wearable ultrasound devices.

In conclusion, the work presented in this thesis provides a solid foundation for the development of next-generation analog front-end solutions for ultrasound imaging, combining high sensitivity, low power operation, and scalability toward full system integration.

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